

Description

Title of Invention: NON-VOLATILE SEMICONDUCTOR STORAGE DEVICE

Technical Field

[0001] The present invention relates to a non-volatile semiconductor memory device.

Background Art

[0002] In a conventional memory cell disclosed in Japanese Patent Laid-Open No. 2011-129816 (Patent Literature 1), a memory gate structure is disposed between two select gate structures (refer to FIG. 15 in Patent Literature 1). This memory cell includes a drain region connected with a bit line, and a source region connected with a source line. A select gate structure, a memory gate structure, and another select gate structure are disposed in this order on a well between the drain and source regions. In the memory cell thus configured, the memory gate structure includes a charge storage layer. Data is programmed by injecting charge into the charge storage layer and erased by removing the charge inside the charge storage layer.

[0003] FIG. 9 is a schematic view illustrating an exemplary circuit configuration of a conventional non-volatile semiconductor memory device 100. In this case, the non-volatile semiconductor memory device 100 includes, for example, a plurality of memory cells 102a, 102b, 102c, 102d, 102e, 102f, 102g, and 102h arranged in a matrix of rows and columns. Memory cell formation parts 101a, 101b, 101c, and 101d are provided for respective pairs of the memory cells 102a, 102b, 102c, 102d, 102e, 102f, 102g, and 102h arranged in the row direction.

[0004] In the non-volatile semiconductor memory device 100, one bit line BL1 (BL2) is shared by the memory cells 102a, 102c, 102e, and 102g (102b, 102d, 102f, and 102h), which are arranged in the column direction among the memory cells 102a, 102b, 102c, 102d, 102e, 102f, 102g, and 102h. A bit voltage is evenly applied to each of the bit lines BL1 and BL2. In the non-volatile semiconductor memory device 100, for example, the memory cell formation parts 101a, 101b, 101c, and 101d share respective memory gate lines MGL1, MGL2, MGL3, and MGL4 and respective drain side select gate lines DGL1, DGL2, DGL3, and DGL4. A predetermined voltage is applied to each of the memory gate lines MGL1, MGL2, MGL3, and MGL4 and each of the drain side select gate lines DGL1, DGL2, DGL3, and DGL4.

[0005] In the non-volatile semiconductor memory device 100, one source side select gate line SGL and one source line SL are shared by all memory cells 102a, 102b, 102c, 102d, 102e, 102f, 102g, and 102h. A predetermined source gate voltage is applied to the source side select gate line SGL, and a predetermined source voltage is applied to the source line SL.

[0006] The memory cells 102a, 102b, 102c, 102d, 102e, 102f, 102g, and 102h have identical configurations. For example, the memory cell 102a includes a memory gate electrode MG connected with a memory gate line MGL1, a drain side select gate electrode DG connected with a drain side select gate line DGL1, and a source side select gate electrode SG connected with the source side select gate line SGL. The memory cells 102a, 102b, 102c, 102d, 102e, 102f, 102g, and 102h each becomes a data programmed state when charge is injected into a charge storage layer EC by a quantum tunneling effect caused by a voltage difference between the memory gate electrode MG and a channel layer.

[0007] At a data reading operation to read, for example, data programmed to the memory cell 102a on the first row and the first column in the conventional non-volatile semiconductor memory device 100, a reading voltage of 1.5 V is applied to the bit line BL1 connected with the memory cell (hereinafter also referred to as a data reading cell) 102a from which data is to be read, whereas a non-reading voltage of 0 V is applied to the bit line BL2 connected with the memory cells 102b, 102d, 102f, and 102h from which no data is to be read.

[0008] Simultaneously, in the non-volatile semiconductor memory device 100, a voltage of 0 V is applied to the memory gate line MGL1, MGL2, MGL3, MGL4, a voltage of 1.5 V is applied to the source side select gate line SGL, and a voltage of 0 V is applied to the source line SL.

Simultaneously, in the non-volatile semiconductor memory device 100, a reading gate voltage of 1.5 V is applied to the drain side select gate line DGL1 connected with the data reading cell 102a, whereas a non-reading gate voltage of 0 V is applied to the drain side select gate lines DGL2, DGL3, and DGL4 connected with the memory cells 102c, 102d, 102e, 102f, 102g, and 102h from which no data is to be read.

[0009] Accordingly, in the data reading cell 102a, the well directly below the drain side select gate electrode DG connected with the bit line BL1 becomes a conductive state, whereas the well directly below the memory gate electrode MG is a non-conductive state when charge is stored in the charge storage layer EC (data is programmed). Accordingly, electrical connection between the source line SL and the bit line BL1 is blocked to maintain intactly the reading voltage of 1.5 V applied to the bit line BL1.

[0010] When no charge is stored in the charge storage layer EC of the data reading cell 102a (when no data is

programmed), the well directly below the memory gate electrode MG is in a conductive state, the source line SL at 0 V and the bit line BL1 at 1.5 V are electrically connected with each other through the data reading cell 102a, and the reading voltage of 1.5 V applied to the bit line BL1 decreases due to the source line SL at 0 V accordingly.

[0011] Simultaneously, in the other memory cells 102c, 102e, and 102g sharing the bit line BL1 with the data reading cell 102a, the well directly below the drain side select gate electrode DG becomes a non-conductive state due to voltage differences between the respective drain side select gate lines DGL2, DGL3, and DGL4 and the bit line BL1, and has no influence on the reading voltage of 1.5 V applied to the bit line BL1. Accordingly, the non-volatile semiconductor memory device 100 can detect whether charge is stored in the charge storage layer EC of the data reading cell 102a by detecting whether the reading voltage applied to the bit line BL1 has changed.

[0012] The following describes, for example, a planar layout of the memory cell formation part 101a among the memory cell formation parts 101a, 101b, 101c, and 101d provided in the non-volatile semiconductor memory device 100 thus configured. The planar layout of the memory cell formation part 101a is, for example, a planar layout as illustrated in FIG. 10. FIG. 10 is a schematic view illustrating an exemplary planar layout of the memory cell formation part 101a when viewed from above a semiconductor substrate. The following describes the memory cell formation part 101a in which the three memory cells 102a, 102b, and 102c are provided.

[0013] In this case, the memory cell formation part 101a includes a memory cell region ER3 in which the memory cells 102a, 102b, and 102c are disposed. A select gate contact region ER6 is disposed at one end of the memory

cell region ER3, and another select gate contact region ER7 is disposed at the other end of the memory cell region ER3. A physical disconnection region ER1 (ER5) is disposed at an end of the select gate contact region ER6 (ER7) through an electrical disconnection region ER2 (ER4).

[0014] In this case, the memory cell formation part 101a includes the strip-shaped memory gate electrode MG extending across the physical disconnection region ER1, the electrical disconnection region ER2, the select gate contact region ER6, the memory cell region ER3, the select gate contact region ER7, the electrical disconnection region ER4, and the physical disconnection region ER5. A memory gate contact MGC is provided on the memory gate electrode MG in, for example, the physical disconnection regions ER1 and ER5.

[0015] The memory cell region ER3 includes a well W having a predetermined shape and disposed on a surface of the semiconductor substrate. For example, the memory gate electrode MG intersects strip-shaped memory disposition regions W1, W2, and W3 of the well W. The memory disposition regions W1, W2, and W3 are each divided into a source region WS and a drain region WD with the memory gate electrode MG interposed therebetween. In the memory cell formation part 101a, the source regions WS of the memory disposition regions W1, W2, and W3 are provided continuously with each other. A predetermined source voltage is evenly applied to each source region WS through a column-shaped source contact SC connected with the source line SL (FIG. 9).

[0016] In the memory cell formation part 101a, the drain regions WD of the memory disposition regions W1, W2, and W3 are separated from each other. Predetermined bit voltages are individually applied from the different bit lines BL1, BL2, ... to the respective drain regions WD

through bit contacts BC provided to the respective drain regions WD.

[0017] In the memory cell region ER3 of the memory cell formation part 101a, a first sidewall 112 of the memory gate electrode MG is disposed in the drain regions WD of the well W, and the drain side select gate electrode DG is disposed along this sidewall 112. A second sidewall 111 of the memory gate electrode MG is disposed in the source regions WS of the well W, and the source side select gate electrode SG is disposed along this sidewall 111. In this case, the drain side select gate electrode DG and the source side select gate electrode SG together with the memory gate electrode MG are shared by the memory cells 102a, 102b, and 102c arranged in the row direction. The drain side select gate electrode DG and the source side select gate electrode SG are insulated from the memory gate electrode MG through a sidewall spacer (not illustrated) made of an insulation material.

[0018] The drain side select gate electrode DG includes a wide select gate contact formation part Ca provided with a drain side select gate contact DGC in the select gate contact region ER6. A predetermined voltage from the drain side select gate line DGL2 (FIG. 9) is applied to the drain side select gate electrode DG through the drain side select gate contact DGC and the select gate contact formation part Ca.

[0019] The source side select gate electrode SG includes a wide select gate contact formation part Cb provided with a source side select gate contact SGC in the select gate contact region ER7. A predetermined voltage from the source side select gate line SGL (FIG. 9) is applied to the source side select gate electrode SG through the source side select gate contact SGC and the select gate contact formation part Cb.

[0020] In addition, the memory gate electrode MG extends to the electrical disconnection regions ER2 and ER4 from the memory cell region ER3, but the drain side select gate electrode DG and the source side select gate electrode SG do not extend to the electrical disconnection regions ER2 and ER4 unlike the memory cell region ER3. Electrical disconnection portions 103a and 103b serving as a p-i-n junction are disposed in place of the drain side select gate electrode DG and the source side select gate electrode SG. The electrical disconnection portions 103a and 103b each includes i-type intrinsic semiconductor layers Ia and Ib, and an opposite-conductivity-type semiconductor layer OC of a conductivity type (in this case, p-type) different from a conductivity type of the drain side select gate electrode DG and the source side select gate electrode SG. The intrinsic semiconductor layers Ia and Ib and the opposite-conductivity-type semiconductor layer OC are arranged along each of the sidewalls 111 and 112 of the memory gate electrode MG in the order of the intrinsic semiconductor layer Ia, the opposite-conductivity-type semiconductor layer OC, and the intrinsic semiconductor layer Ib.

[0021] In this manner, in the electrical disconnection regions ER2 and ER4 of the memory cell formation part 101a, the i-type intrinsic semiconductor layer Ia, the p-type opposite-conductivity-type semiconductor layer OC, and the i-type intrinsic semiconductor layer Ib are arranged in this order from each of the n-type drain side select gate electrode DG and the n-type source side select gate electrode SG. With this configuration, p-i-n junctions are disposed at ends of each of the n-type drain side select gate electrode DG and the n-type source side select gate electrode SG, thereby providing electrical disconnection of the drain side select gate

electrode DG and the source side select gate electrode SG at two places of the corresponding electrical disconnection portions 103a and 103b.

[0022] In the physical disconnection regions ER1 and ER5 at the ends of the electrical disconnection regions ER2 and ER4, no conduction layer made of, for example, a semiconductor material is disposed along the sidewalls 111 and 112 and end walls 113 of the memory gate electrode MG, thereby providing physical disconnection portions 104 in which the drain side select gate electrode DG and the source side select gate electrode SG are not in contact with each other. With this configuration, in the memory cell formation part 101a, the drain side select gate electrode DG and the source side select gate electrode SG are insulated from each other not only through the two electrical disconnection portions 103a and 103b but through the physical disconnection portions 104 in the physical disconnection regions ER1 and ER5. Accordingly, predetermined voltages can be independently applied to the drain side select gate electrode DG and the source side select gate electrode SG.

Citation List

Patent Literature

[0023] Patent Literature 1: Japanese Patent Laid-Open No. 2011-129816

Summary of Invention

Technical Problem

[0024] In the memory cell formation part 101a thus configured, electrical connection between the drain side select gate electrode DG and the source side select gate electrode SG is prevented by each set of two of the electrical disconnection portions 103a and 103b and one

of the physical disconnection portions 104. However, for some reasons, failure potentially occurs to the electrical disconnection portions 103a and 103b and the physical disconnection portions 104 to achieve the electrical connection between the drain side select gate electrode DG and the source side select gate electrode SG in some cases.

[0025] For example, at a data reading operation to read data from the memory cell 102a on the first row and the first column as illustrated in FIG. 9, when a short-circuit defect occurs to the memory cell formation part 101b from which no data is to be read due to the electrical connection between the drain side select gate electrode DG and the source side select gate electrode SG, the drain side select gate line DGL2 at 0 V and the source side select gate line SGL at 1.5 V are electrically connected with each other at the memory cell formation part 101b (illustrated as a wire L in FIG. 9).

[0026] As a result, the voltage of 0 V applied to the drain side select gate line DGL2 increases or the voltage of 1.5 V applied to the source side select gate line SGL shared by all memory cells 102a, 102b, ... decreases in the non-volatile semiconductor memory device 100, and accordingly, a false reading operation potentially occurs due to voltage variation in the drain side select gate line DGL2 and the source side select gate line SGL.

[0027] For this reason, it is desired to provide further measures for preventing the occurrence of the electrical connection between the drain side select gate electrode DG and the source side select gate electrode SG in the non-volatile semiconductor memory device 100, thereby preventing any false reading operation occurring due to voltage variation at a data reading operation as compared to conventional cases.

[0028] The present invention is intended to solve the above-described problem by providing a non-volatile semiconductor memory device capable of preventing any false reading operation occurring due to voltage variation at a data reading operation as compared to conventional cases.

Solution to Problem

[0029] To solve the above-described problem, a non-volatile semiconductor memory device according to claim 1 is a non-volatile semiconductor memory device including a plurality of memory cell formation parts. Each memory cell formation part includes: a first select gate structure including a first select gate electrode on a well of a semiconductor substrate through a first select gate insulating film; a second select gate structure including a second select gate electrode on the well through a second select gate insulating film; a memory gate structure provided between the first select gate structure and the second select gate structure through sidewall spacers and including a lower gate insulating film, a charge storage layer, an upper gate insulating film, and a memory gate electrode stacked on the well in this order; and an extended electrode portion as an extension portion extending from the memory gate electrode in a select gate formation region in which the first select gate structure and the second select gate structure are disposed facing each other. Three or more opposite-conductivity-type semiconductor layers of a conductivity type different from a conductivity type of the first select gate electrode and the second select gate electrode, or three or more intrinsic semiconductor layers are provided on sidewalls of the extended electrode portion.

[0030] A non-volatile semiconductor memory device according to claim 2 is a non-volatile semiconductor memory device including a plurality of memory cell formation parts. Each memory cell formation part includes: a first select gate structure including a first select gate electrode on a well of a semiconductor substrate through a first select gate insulating film; a second select gate structure including a second select gate electrode on the well through a second select gate insulating film; and a memory gate structure provided between the first select gate structure and the second select gate structure through sidewall spacers and including a lower gate insulating film, a charge storage layer, an upper gate insulating film, and a memory gate electrode stacked on the well in this order. An extended electrode portion as an extension portion extending from the memory gate electrode in a select gate formation region connects one memory cell formation part and the other memory cell formation part. The first select gate structure and the second select gate structure are disposed facing each other in the select gate formation region. Three or more opposite-conductivity-type semiconductor layers of a conductivity type different from a conductivity type of the first select gate electrode and the second select gate electrode, or three or more intrinsic semiconductor layers are provided on sidewalls of the extended electrode portion.

Advantageous Effects of Invention

[0031] In the non-volatile semiconductor memory device according to claim 1 of the present invention, the three or more opposite-conductivity-type semiconductor layers, or the three or more intrinsic semiconductor layers for achieving disconnection between the first select gate electrode and the second select gate electrode are

provided along the sidewalls of the extended electrode portion so that the first select gate electrode and the second select gate electrode are disconnected from each other at the increased number of places as compared to conventional cases, thereby preventing any false reading operation occurring due to voltage variation at a data reading operation as compared to conventional cases.

[0032] In the non-volatile semiconductor memory device according to claim 2 of the present invention, the three or more opposite-conductivity-type semiconductor layers, or the three or more intrinsic semiconductor layers for disconnecting electrical connection between the first select gate electrode of a first memory cell formation part and the first select gate electrode or the second select gate electrode of a second memory cell formation part are provided along the sidewalls of the extended electrode portion so that the first select gate electrode of the first memory cell formation part and the first select gate electrode or the second select gate electrode of the second memory cell formation part are disconnected from each other at the increased number of places as compared to conventional cases, thereby preventing any false reading operation occurring due to voltage variation at a data reading operation as compared to conventional cases.

Brief Description of Drawings

[0033] FIG. 1 is a schematic view illustrating a sectional configuration of a memory cell included in a non-volatile semiconductor memory device according to the present invention.

FIG. 2 is a schematic view illustrating a circuit configuration of the non-volatile semiconductor memory device according to the present invention.

FIG. 3 is a table listing voltage values of the non-volatile semiconductor memory device at various operations.

FIG. 4 is a schematic view illustrating a planar layout of a non-volatile semiconductor memory device according to a first embodiment.

FIG. 5 is a schematic view illustrating a planar layout of a non-volatile semiconductor memory device according to a second embodiment.

FIG. 6 is a schematic view illustrating a planar layout of a non-volatile semiconductor memory device according to a third embodiment.

FIG. 7 is a schematic view illustrating a planar layout of a non-volatile semiconductor memory device according to a fourth embodiment.

FIG. 8 is a schematic view illustrating a planar layout of a non-volatile semiconductor memory device according to another embodiment.

FIG. 9 is a schematic view illustrating a circuit configuration of a conventional non-volatile semiconductor memory device.

FIG. 10 is a schematic view illustrating a planar layout of a conventional memory cell formation part.

Description of Embodiments

[0034] Hereinafter, embodiments of the present invention will be described in the following order.

<1. First embodiment>

1-1. Configuration of memory cell

1-2. Circuit configuration of non-volatile semiconductor memory device according to the present invention

1-3. Voltages in non-volatile semiconductor memory device at various operations

1-4. Planar layout of non-volatile semiconductor memory device

1-5. Operations and effects

<2. Planar layout of non-volatile semiconductor memory device according to second embodiment>

<3. Planar layout of non-volatile semiconductor memory device according to third embodiment>

<4. Planar layout of non-volatile semiconductor memory device according to fourth embodiment>

<5. Other embodiments>

<6. Positional relation between electrical and physical disconnection regions>

[0035] (1) First embodiment

(1-1) Configuration of memory cell

The following first describes the configuration of each of memory cells arranged in a matrix of rows and columns in a non-volatile semiconductor memory device according to the present invention. As illustrated in FIG. 1, a memory cell 2a includes a memory gate structure 4a, a drain side select gate structure 5a, and a source side select gate structure 6a disposed on a well W made of, for example, P-type Si. The memory gate structure 4a is included in an N-type transistor structure. The drain side select gate structure 5a is included in an N-type metal-oxide-semiconductor (MOS) transistor structure. The source side select gate structure 6a is included in an N-type MOS transistor structure.

[0036] A drain region WD and a source region WS are spaced at a predetermined distance on a surface of the well W. The drain region WD is disposed at one end of the drain side select gate structure 5a, and the source region WS is disposed at one end of the source side select gate structure 6a. The drain region WD is connected with a bit line BL1, and the source region WS is connected with a source line SL. A low concentration

drain region WDa is disposed adjacent to the drain region WD on the surface of the well W. A sidewall structure SW along a sidewall of the drain side select gate structure 5a is disposed on the low concentration drain region WDa. A low concentration source region WSa is disposed adjacent to the source region WS on the surface of the well W. Another sidewall structure SW along a sidewall of the source side select gate structure 6a is disposed on the low concentration source region WSa.

[0037] The memory gate structure 4a includes a charge storage layer EC on the well W between the low concentration drain region WDa and the low concentration source region WSa through a lower gate insulating film Bo made of an insulation material such as SiO_2 . The charge storage layer EC is made of, for example, silicon nitride (Si_3N_4), silicon oxynitride (SiON), alumina (Al_2O_3), or hafnia (HfO_2). The memory gate structure 4a further includes a memory gate electrode MG on the charge storage layer EC through an upper gate insulating film Tp made of an insulation material. Accordingly, the memory gate structure 4a has a configuration in which the charge storage layer EC is insulated from the well W and the memory gate electrode MG through the lower gate insulating film Bo and the upper gate insulating film Tp.

[0038] In addition to this configuration, a cap film CP made of an insulation material is disposed on the memory gate electrode MG in the memory gate structure 4a. A silicide layer S1 on an upper surface of the drain side select gate structure 5a and a silicide layer S2 on an upper surface of the source side select gate structure 6a are disposed separately from an upper surface of the memory gate electrode MG by the thickness of the cap film CP. With this configuration, no silicide layer is disposed on the upper surface of the memory gate

electrode MG in a region of the memory cell 2a, and the memory gate electrode MG is covered by the cap film CP. [0039] In the present embodiment, the cap film CP has a laminated structure in which an upper cap layer CPb is stacked on a lower cap film CPa. The lower cap film CPa is made of an insulation material such as SiO_2 , and the upper cap layer CPb is made of an insulation material such as SiN which is different from the insulation material of the lower cap film CPa.

[0040] The memory gate electrode MG of the memory gate structure 4a is provided with a wall-shaped first sidewall 11 and a wall-shaped second sidewall 12 disposed facing the first sidewall 11. In the memory gate structure 4a, sidewalls of the lower gate insulating film Bo, the charge storage layer EC, the upper gate insulating film Tp, and the cap film CP are aligned with the first sidewall 11 and the second sidewall 12 of the memory gate electrode MG. The lower gate insulating film Bo, the charge storage layer EC, the upper gate insulating film Tp, and the cap film CP are disposed in a region between the first sidewall 11 and the second sidewall 12 of the memory gate electrode MG.

[0041] In the memory gate structure 4a, a sidewall spacer 28a made of an insulation material is disposed along the second sidewall 12 of the memory gate electrode MG and the sidewalls of the lower gate insulating film Bo, the charge storage layer EC, the upper gate insulating film Tp, and the cap film CP so that the memory gate structure 4a is disposed adjacent to the drain side select gate structure 5a through the sidewall spacer 28a. The sidewall spacer 28a disposed between the memory gate structure 4a and the drain side select gate structure 5a has the thickness enough to insulate the memory gate structure 4a and the drain side select gate structure 5a from each other. The thickness of the sidewall spacer

28a between the memory gate structure 4a and the drain side select gate structure 5a is desirably set in the range of 5 nm to 40 nm inclusive with taken into account breakdown voltage of the sidewall spacer 28a and readout current between the memory gate structure 4a and the drain side select gate structure 5a.

[0042] The drain side select gate structure 5a includes a drain side select gate insulating film 30 on the well W between the sidewall spacer 28a and the drain region WD. The drain side select gate insulating film 30 is made of an insulation material and has the thickness less than or equal to 9 nm, preferably less than or equal to 3 nm. A drain side select gate electrode DG is disposed on the drain side select gate insulating film 30. The silicide layer S1 is disposed on an upper surface of the drain side select gate electrode DG as a second select gate electrode. The silicide layer S1 is connected with a drain side select gate line DGL1 as a second select gate line.

[0043] In the memory gate structure 4a, a sidewall spacer 28b made of an insulation material is disposed along the first sidewall 11 of the memory gate electrode MG and the sidewalls of the lower gate insulating film Bo, the charge storage layer EC, the upper gate insulating film Tp, and the cap film CP. The memory gate structure 4a is disposed adjacent to the source side select gate structure 6a through the sidewall spacer 28b. The sidewall spacer 28b disposed between the memory gate structure 4a and the source side select gate structure 6a has a thickness between 5 nm and 40 nm inclusive same as the thickness of the sidewall spacer 28a, which is enough to insulate the memory gate structure 4a and the source side select gate structure 6a from each other.

[0044] The source side select gate structure 6a includes a source side select gate insulating film 33 on the well

W between the sidewall spacer 28b and the source region WS. The source side select gate insulating film 33 is made of an insulation material and has the thickness less than or equal to 9 nm, preferably less than or equal to 3 nm. A source side select gate electrode SG is disposed on the source side select gate insulating film 33. The silicide layer S2 is disposed on an upper surface of the source side select gate electrode SG as a first select gate electrode. The silicide layer S2 is connected with a source side select gate line SGL as a first select gate line.

[0045] Additionally, in the present embodiment, the source side select gate electrode SG and the drain side select gate electrode DG, which are disposed along the first sidewall 11 and the second sidewall 12 of the memory gate electrode MG through the sidewall spacers 28a and 28b, each has a sidewall shape in which the distance from the memory gate electrode MG increases such that the top portion of the select gate electrode slopes down toward the well W.

[0046] The source side select gate structure 6a and the drain side select gate structure 5a of the memory cell 2a are sidewall-shaped along the respective sidewalls (the first sidewall 11 and the second sidewall 12) of the memory gate structure 4a. With this configuration, the silicide layer S1 on the drain side select gate electrode DG and the silicide layer S2 on the source side select gate electrode SG are spaced from the memory gate electrode MG through the cap film CP on the memory gate electrode MG even when the source side select gate structure 6a and the drain side select gate structure 5a are disposed close to the memory gate structure 4a. Accordingly, short circuit is prevented between the silicide layers S1 and S2 and the memory gate electrode MG.

[0047] (1-2) Circuit configuration of non-volatile semiconductor memory device according to the present invention

The following describes a circuit configuration of the non-volatile semiconductor memory device according to the present invention. As illustrated in FIG. 2, this non-volatile semiconductor memory device 1 includes, for example, a plurality of memory cells 2a, 2b, 2d, 2e, 2g, 2h, 2i, and 2j arranged in the matrix. The memory cells 2b, 2d, 2e, 2g, 2h, 2i, and 2j have configurations identical to the configuration of the memory cell 2a described with reference to FIG. 1, and each includes the memory gate electrode MG connected with a memory gate line MGL, the drain side select gate electrode DG connected with the drain side select gate line DGL1 (DGL2, DGL3, DGL4), and the source side select gate electrode SG connected with the source side select gate line SGL.

[0048] The non-volatile semiconductor memory device 1 includes memory cell formation parts 3a, 3b, 3c, and 3d for the memory cells 2a and 2b, the memory cells 2d and 2e, the memory cells 2g and 2h, and the memory cells 2i and 2j, respectively, arranged in the row direction. A predetermined substrate voltage is applied to the memory cells 2a, 2b, 2d, and 2e through, for example, a substrate voltage line Back.

[0049] In the non-volatile semiconductor memory device 1, the single bit line BL1 (BL2) is shared by the memory cells 2a, 2d, 2g, and 2i (2b, 2e, 2h, and 2j) arranged in the column direction among the memory cells 2a, 2b, 2d, 2e, 2g, 2h, 2i, and 2j. Predetermined bit voltages are evenly applied, through the bit lines BL1 and BL2, to the memory cells 2a, 2d, 2g, and 2i, and the memory cells 2b, 2e, 2h, and 2j, respectively, in the column direction. In addition, the drain side select gate lines DGL1, DGL2, DGL3, and DGL4 are shared by, for example, the memory

cell formation parts 3a, 3b, 3c, and 3d in the non-volatile semiconductor memory device 1. Predetermined voltages are applied to the memory cell formation parts 3a, 3b, 3c, and 3d through the respective drain side select gate lines DGL1, DGL2, DGL3, and DGL4.

[0050] In the non-volatile semiconductor memory device 1, the single memory gate line MGL, the single source side select gate line SGL, and the single source line SL are shared by all memory cells 2a, 2b, 2d, 2e, 2g, 2h, 2i, and 2j. A predetermined memory gate voltage is applied to the memory gate line MGL, a predetermined source gate voltage is applied to the source side select gate line SGL, and a predetermined source voltage is applied to the source line SL.

[0051] (1-3) Voltages in non-volatile semiconductor memory device at various operations

The following describes various operations at the non-volatile semiconductor memory device 1. FIG. 3 is a table listing an exemplary voltage values at each site in the non-volatile semiconductor memory device 1 illustrated in FIG. 2 at a data programming operation ("Prog") to inject charge into the charge storage layer EC of, for example, the memory cell 2a, at a data reading operation ("Read") to detect whether charge is stored in the charge storage layer EC of the memory cell 2a, or at a data erasing operation ("Erase") to remove charge inside the charge storage layer EC of, for example, the memory cell 2a.

[0052] The column "Prog" in FIG. 3 lists voltage values ("select column" and "select row") for injecting charge into the charge storage layer EC of the memory cell 2a, and voltage values ("non-select column" or "non-select row") for injecting no charge into the charge storage layer EC of the memory cell 2a.

[0053] For example, to inject charge into the charge storage layer EC of the memory cell 2a, a charge storage gate voltage of 12 V is applied from the memory gate line MGL to the memory gate electrode MG and a substrate voltage of 0 V is applied to the well W (denoted by "Back" in FIG. 3) as listed in the column "Prog" in FIG. 3. Simultaneously, a gate off voltage of 0 V is applied from the source side select gate line SGL to the source side select gate electrode SG, and a source off voltage of 0 V is applied from the source line SL to the source region WS. Accordingly, the source side select gate structure 6a blocks electrical connection between the source region WS and a channel layer formation carrier region of the memory gate structure 4a, thereby preventing voltage application from the source line SL to the channel layer formation carrier region of the memory gate structure 4a.

[0054] Simultaneously, a drain side select gate voltage of 1.5 V is applied from the drain side select gate line DGL1 to the drain side select gate electrode DG, and a charge storage bit voltage of 0 V is applied to the drain region WD from the bit line BL1. Accordingly, the drain side select gate structure 5a electrically connects the drain region WD and the channel layer formation carrier region of the memory gate structure 4a.

[0055] The electrical connection between the drain region WD and the channel layer formation carrier region of the memory gate structure 4a induces carriers into the channel layer formation carrier region so that the carriers form a channel layer at 0 V, which is same as the charge storage bit voltage, in the surface of the well W. Accordingly, a large voltage difference of 12 V occurs between the memory gate electrode MG of the memory gate structure 4a and the channel layer, and causes a quantum tunneling effect by which charge is injected into

the charge storage layer EC, thereby achieving a data programmed state.

[0056] To prevent charge injection into the charge storage layer EC of the memory cell 2a when a charge storage gate voltage necessary for injecting charge into the charge storage layer EC is applied to the memory gate electrode MG of the memory cell 2a, the source side select gate structure 6a blocks electrical connection between the source region WS and the well W of a region facing the memory gate electrode MG whereas the drain side select gate structure 5a blocks electrical connection between the drain region WD and the well W of the region facing the memory gate electrode MG.

[0057] Thus, in the memory cell 2a to which no data is programmed, a depleted layer is disposed in the channel layer formation carrier region, so that potential at the surface of the well W increases based on the charge storage gate voltage, and a voltage difference between the memory gate electrode MG and the surface of the well W decreases accordingly, thereby preventing charge injection into the charge storage layer EC.

[0058] At a data reading operation specified through the column "Read" in FIG. 3, for example, the bit line BL1 connected with the memory cell 2a, from which data is to be read, is precharged to an exemplary voltage of 1.5 V, and then a voltage of 0 V is applied to the source line SL. In this state, the potential of the bit line BL1, which changes depending on whether current flows through the memory cell 2a, is detected to determine whether charge is stored in the charge storage layer EC of the memory cell 2a. Specifically, when charge is stored in the charge storage layer EC of the memory gate structure 4a (when data is programmed) at data reading from the memory cell 2a, the well W directly below the memory gate structure 4a is in a non-conductive state, blocking

electrical connection between the drain region WD and the source region WS. As a result, the reading voltage of 1.5 V applied to the bit line BL1 connected with the drain region WD is maintained intactly in the memory cell 2a from which data is to be read.

[0059] When no charge is stored in the charge storage layer EC of the memory gate structure 4a (when no data is programmed) at data reading from the memory cell 2a, the well W directly below the memory gate structure 4a is in a conductive state, electrically connecting the drain region WD and the source region WS. As a result, the source line SL at 0 V and the bit line BL1 at 1.5 V are electrically connected with each other through the memory cell 2a. As a result, the reading voltage applied to the bit line BL1 is applied to the source line SL at 0 V in the memory cell 2a from which data is to be read, and the reading voltage of 1.5 V applied to the bit line BL1 decreases accordingly.

[0060] Accordingly, the non-volatile semiconductor memory device 1 enables execution of the data reading operation of determining whether charge is stored in the charge storage layer EC of the memory cell 2a by detecting whether the reading voltage applied to the bit line BL1 has changed. Simultaneously, a non-reading voltage of 0 V is applied to the bit line BL2 connected only with the memory cells 2b, 2e, 2h, and 2j from which no data is to be read.

[0061] At a data erasing operation to remove charge inside the charge storage layer EC of the memory cell 2a ("Erase" in FIG. 3), a memory gate voltage of -12 V is applied from the memory gate line MGL to the memory gate electrode MG so that charge inside the charge storage layer EC is removed toward the well W at 0 V, thereby erasing data.

[0062] (1-4) Planar layout of non-volatile semiconductor memory device

The following describes a planar layout of the non-volatile semiconductor memory device 1 described above. FIG. 4 is a schematic view illustrating the planar layout of the non-volatile semiconductor memory device 1 according to the present invention including a plurality of memory cell formation parts 3a, 3b, 3c, ... disposed on a semiconductor substrate, when viewed from above the semiconductor substrate. The memory cell formation parts 3a, 3b, 3c, ... all have identical configurations, and thus the following description will be made mainly on the memory cell formation part 3a.

[0063] The sectional configuration of the memory cell 2a illustrated in FIG. 1 is a sectional configuration along line A-A' in FIG. 4. Illustration of, for example, the sidewall structures SW and the silicide layers S1 and S2 on the drain side select gate structure 5a and the source side select gate structure 6a in addition to the sidewall spacers 28a and 28b on the sidewalls of the memory gate structure 4a illustrated in FIG. 1 is omitted in FIG. 4. In the present embodiment, the memory cell formation parts 3a, 3b, 3c, ... extend side by side at a predetermined interval in one direction (the row direction in FIG. 4) on the semiconductor substrate.

[0064] In this case, the memory cell formation part 3a includes a select gate formation region ER9 in which the source side select gate electrode SG and the drain side select gate electrode DG face to each other with the memory gate electrode MG interposed therebetween. The select gate formation region ER9 includes a memory cell region ER3 in which the memory cells 2a, 2b, and 2c are arranged in a longitudinal direction of the memory cell formation part 3a, a select gate contact region ER6 provided at one end of the memory cell region ER3, and a

select gate contact region ER7 provided at the other end of the memory cell region ER3.

[0065] In the memory cell formation part 3b (3c), the memory cells 2d, 2e, and 2f (2g, 2h, and 2i) are arranged in the memory cell region ER3 along the longitudinal direction of the memory cell formation part 3b (3c).

Although FIG. 2 only illustrates the memory cell 2a and 2b (2d and 2e, or 2g and 2h) in the memory cell formation part 3a (3b or 3c), FIG. 4 additionally illustrates the memory cell 2c (2f or 2i) on the third column adjacent to the memory cell 2b (2e or 2h) on the second column.

[0066] In the memory cell formation part 3a, the memory gate electrode MG extending in one direction is disposed in the select gate formation region ER9. The memory gate electrode MG in the select gate formation region ER9 includes the first sidewall extending across the select gate formation region ER9, and the second sidewall 12 disposed facing the first sidewall. The source side select gate electrode SG is disposed along the first sidewall 11, and the drain side select gate electrode DG is disposed along the second sidewall 12.

[0067] In the memory cell region ER3, the well W having a predetermined shape is disposed in a surface of the semiconductor substrate. For example, the memory cell formation part 3a intersects strip-shaped memory disposition regions W1, W2, and W3 of the well W. The memory cell 2a (2b or 2c) including the memory gate structure 4a, the drain side select gate structure 5a, and the source side select gate structure 6a are disposed on the memory disposition region W1 (W2 or W3) in the memory cell region ER3 of the memory cell formation part 3a.

[0068] The memory disposition regions W1, W2, and W3 of the well W are each divided into the source region WS and the drain region WD with the memory gate structure 4a

interposed therebetween. The drain regions WD of the memory disposition regions W1, W2, and W3 between the memory cell formation parts 3a and 3b are separated from each other and each includes a column-shaped bit contact BC. The bit contacts BC are connected with the different bit lines BL1, BL2, ... (FIG. 2), and receive predetermined bit voltages from the corresponding bit lines BL1, BL2, ... Accordingly, the drain regions WD in the memory cell formation part 3a receive predetermined bit voltages from the different bit lines BL1, BL2, ... through the bit contacts BC.

[0069] In the present embodiment, since the drain regions WD are shared by the memory cell formation part 3a and the memory cell formation part 3b adjacent thereto, a bit voltage same as that applied to the memory cell 2a (2b or 2c) in the memory cell formation part 3a can be applied to the memory cell 2d (2e or 2f) in the memory cell formation part 3b.

[0070] The source regions WS of the memory disposition regions W1, W2, and W3 are provided continuously with each other, sharing a column-shaped source contact SC provided at a predetermined position. The source contact SC is connected with the source line SL (FIG. 2) to evenly apply, to the source regions WS of the memory disposition regions W1, W2, and W3, a predetermined source voltage applied from the source line SL.

[0071] In the present embodiment, the first sidewall 11 of the memory gate electrode MG is disposed on the source region WS side in the well W in the memory cell formation part 3a. The source side select gate structure 6a is disposed along the first sidewall 11 of the memory gate electrode MG. The second sidewall 12 of the memory gate electrode MG is disposed on the drain region WD side in the well W in the memory cell formation part 3a. The

drain side select gate structure 5a is disposed along the second sidewall 12 of the memory gate electrode MG.

[0072] In the source side select gate structure 6a, the sidewall-shaped source side select gate electrode SG is disposed along the first sidewall 11 of the memory gate structure 4a, and a wide select gate contact formation part Ca integrated with the source side select gate electrode SG is disposed in the select gate contact region ER7.

[0073] The select gate contact formation part Ca includes a mounting portion over the memory gate electrode MG, and a plane portion having a plane surface along the semiconductor substrate. The plane portion is provided with a column-shaped source side select gate contact SGC connected with a source side select gate line (not illustrated). With this configuration, a predetermined voltage is applied from the source side select gate line SGL to the source side select gate electrode SG having a tilted sidewall shape with a small width through the source side select gate contact SGC and the select gate contact formation part Ca.

[0074] In the drain side select gate structure 5a, the sidewall-shaped drain side select gate electrode DG is disposed along the second sidewall 12 of the memory gate structure 4a, and a wide select gate contact formation part Cb integrated with the drain side select gate electrode DG is disposed in the select gate contact region ER6.

[0075] The select gate contact formation part Cb includes a mounting portion over the memory gate electrode MG, and a plane portion having a plane surface along the semiconductor substrate. The plane portion is provided with a column-shaped drain side select gate contact DGC connected with the drain side select gate line DGL1. With this configuration, a predetermined voltage is

applied from the drain side select gate line DGL1 to the drain side select gate electrode DG having a tilted sidewall shape with a small width through the drain side select gate contact DGC and the select gate contact formation part Cb.

[0076] The select gate contact formation parts Ca and Cb provided in the select gate contact regions ER7 and ER6 may each have such various shapes that the select gate contact formation part is provided continuously with the source side select gate electrode SG or the drain side select gate electrode DG, and the source side select gate contact SGC or the drain side select gate contact DGC is formed on the select gate contact formation part. In addition, the select gate contact formation parts Ca and Cb may be disposed at various positions in one or both of the select gate contact regions ER7 and ER6.

[0077] In addition to this configuration, the memory cell formation part 3a includes an electrical disconnection region ER2 (ER4) disposed at an end of the select gate contact region ER6 (ER7), and a physical disconnection region ER1 (ER5) disposed at an end of the electrical disconnection region ER2 (ER4). The electrical disconnection region ER2 (ER4) and the physical disconnection region ER1 (ER5) include an extended electrode portion 15a (15b) as the memory gate electrode MG extending from the select gate formation region ER9.

[0078] In the present embodiment, when viewed from above the semiconductor substrate, the extended electrode portion 15a (15b) is such a C shape that extends from an end of the select gate formation region ER9 to the physical disconnection region ER1 (ER5) through the electrical disconnection region ER2 (ER4) and then turns around in the physical disconnection region ER1 (ER5) before returning to the electrical disconnection region ER2 (ER4).

[0079] The extended electrode portion 15a (15b) includes an extension part 16a extending straight from the memory gate electrode MG in the select gate formation region ER9, an end part 16b having straight shape disposed laterally outside of the extension part 16a, and a connection part 16c connecting the extension part 16a and the end part 16b. The extension part 16a and the end part 16b is disposed in the electrical disconnection region ER2, and the connection part (non-sidewall formation part) 16c as a turning part is disposed in the physical disconnection region ER1.

[0080] In the present embodiment, the extended electrode portion 15a bends to the first sidewall 11 side of the memory gate electrode MG so that the end part 16b is disposed on the first sidewall 11 side, and the extended electrode portion 15b bends to the second sidewall 12 side of the memory gate electrode MG so that the end part 16b is disposed on the second sidewall 12 side.

[0081] The memory gate electrode MG extends as the extended electrode portion 15a (15b) from the select gate formation region ER9 to the electrical disconnection region ER2 (ER4), but the source side select gate electrode SG and the drain side select gate electrode DG do not extend to the electrical disconnection region ER2 (ER4) unlike the select gate formation region ER9. Four electrical disconnection portions 13a, 13b, 13c, and 13d (13e, 13f, 13g, and 13h) are disposed on sidewalls of the extended electrode portion 15a (15b) in place of the source side select gate electrode SG and the drain side select gate electrode DG.

[0082] The electrical disconnection portions 13a, 13b, 13c, and 13d (13e, 13f, 13g, and 13h) all have identical configurations and each includes i-type sidewall-shaped intrinsic semiconductor layers Ia and Ib and a sidewall-shaped opposite-conductivity-type semiconductor layer OC.

The opposite-conductivity-type semiconductor layer OC is disposed between the intrinsic semiconductor layers Ia and Ib. The opposite-conductivity-type semiconductor layer OC is of a conductivity type (in this case, p-type) different from a conductivity type of the source side select gate electrode SG and the drain side select gate electrode DG.

[0083] In the extension part 16a of the extended electrode portion 15a, the electrical disconnection portion 13a is disposed along a first sidewall continuously provided flush with the first sidewall 11 of the memory gate electrode MG, and the electrical disconnection portion 13c is disposed along a second sidewall continuously provided flush with the second sidewall 12 of the memory gate electrode MG. In the memory cell formation part 3a, for example, the electrical disconnection portion 13a provides a p-i-n junction along the first sidewall 11 of the memory gate electrode MG and the sidewall of the extension part 16a from the n-type source side select gate electrode SG as a starting point. Similarly, in the second sidewall 12 side of the memory gate electrode MG of the memory cell formation part 3a, for example, the electrical disconnection portion 13c provides a p-i-n junction along the second sidewall 12 and the sidewall of the extension part 16a from the n-type drain side select gate electrode DG as a starting point.

[0084] In addition, the electrical disconnection portion 13b is disposed on a sidewall facing the extension part 16a at the end part 16b of the extended electrode portion 15a, and the electrical disconnection portion 13d is disposed on a sidewall disposed outside. Accordingly, in the extended electrode portion 15a, the four electrical disconnection portions 13a, 13b, 13d, and 13c are disposed in this order on the sidewalls extending between

the source side select gate electrode SG disposed along the first sidewall 11 of the memory gate electrode MG and the drain side select gate electrode DG disposed along the second sidewall 12 of the memory gate electrode MG. With this configuration, three or more opposite-conductivity-type semiconductor layers and intrinsic semiconductor layers are provided on the sidewalls of the extended electrode portion 15a.

[0085] Accordingly, for example, even when a foreign object adheres to the electrical disconnection portion 13a of the extension part 16a or the connection part 16c to be described later, providing conduction between the source side select gate electrode SG and the electrical disconnection portion 13b of the end part 16b, the electrical disconnection portions 13b and 13d each provides a p-i-n junction along the first sidewall 11 of the memory gate electrode MG and the sidewall of the end part 16b from the n-type source side select gate electrode SG as a starting point.

[0086] In addition to this configuration, in the connection part 16c as a non-sidewall formation part in the physical disconnection region ER1, physical disconnection portions 14a and 14b are disposed on an outer peripheral wall and an inner peripheral wall connecting the sidewalls of the extension part 16a and the sidewalls of the end part 16b. In the physical disconnection portions 14a and 14b, no conduction layer made of, for example, a semiconductor material is provided along the outer and inner peripheral walls of the connection part 16c so that the outer and inner peripheral walls of the connection part 16c are externally exposed. With this configuration, the physical disconnection portions 14a and 14b each provides physical disconnection through a gap between the source side select gate electrode SG and the drain side select

gate electrode DG, thereby achieving a non-conductive state between the source side select gate electrode SG and the drain side select gate electrode DG.

[0087] In the present embodiment, the physical disconnection portion 14a is disposed along the outer peripheral wall of the connection part 16c and provides a non-conductive state between the electrical disconnection portions 13c and 13d through a gap between the electrical disconnection portion 13c disposed on the first sidewall of the extension part 16a and the electrical disconnection portion 13d disposed on the first sidewall of the end part 16b. The physical disconnection portion 14b is disposed along the inner peripheral wall of the connection part 16c and provides a non-conductive state between the electrical disconnection portions 13a and 13b through a gap between the electrical disconnection portion 13a disposed on the second sidewall of the extension part 16a and the electrical disconnection portion 13b disposed on the second sidewall of the end part 16b.

[0088] In this manner, in the extended electrode portion 15a, the electrical disconnection portion 13a, the physical disconnection portion 14b, the electrical disconnection portions 13b and 13d, the physical disconnection portion 14a, and the electrical disconnection portion 13c are disposed in this order on the sidewalls extending between the source side select gate electrode SG disposed along the first sidewall 11 of the memory gate electrode MG and the drain side select gate electrode DG disposed along the second sidewall 12 of the memory gate electrode MG. Accordingly, the extended electrode portion 15a prevents conduction between the source side select gate electrode SG and the drain side select gate electrode DG through the four

electrical disconnection portions 13a, 13b, 13d, and 13c and the two physical disconnection portions 14a and 14b. [0089] Similarly, in the extension part 16a of the extended electrode portion 15b disposed at the other end of the memory cell formation part 3a, the electrical disconnection portion 13e is disposed along a first sidewall continuously provided flush with the first sidewall 11 of the memory gate electrode MG, and the electrical disconnection portion 13g is disposed along a second sidewall continuously provided flush with the second sidewall 12 of the memory gate electrode MG. In the end part 16b of the extended electrode portion 15b, the electrical disconnection portion 13h is disposed on a sidewall facing the extension part 16a, and the electrical disconnection portion 13f is disposed on a sidewall disposed outside.

[0090] Accordingly, in the extended electrode portion 15b, the four electrical disconnection portions 13e, 13f, 13h, and 13g are disposed in this order the sidewalls extending between the source side select gate electrode SG disposed along the first sidewall 11 of the memory gate electrode MG and the drain side select gate electrode DG disposed along the second sidewall 12 of the memory gate electrode MG.

[0091] In addition to this configuration, in the connection part 16c in the physical disconnection region ER5, physical disconnection portions 14c and 14d are disposed on outer and inner peripheral walls connecting the sidewalls of the extension part 16a and the sidewalls of the end part 16b. In the physical disconnection portions 14c and 14d, no conduction layer made of, for example, a semiconductor material is provided on the outer and inner peripheral walls of the connection part 16c so that the outer and inner peripheral walls of the connection part 16c are externally exposed. With this

configuration, the physical disconnection portions 14c and 14d each provides physical disconnection through a gap between the source side select gate electrode SG and the drain side select gate electrode DG, thereby achieving a non-conductive state between the source side select gate electrode SG and the drain side select gate electrode DG.

[0092] In the present embodiment, the physical disconnection portion 14c is disposed along the outer peripheral wall of the connection part 16c and provides a non-conductive state between the electrical disconnection portion 13e disposed on the first sidewall of the extension part 16a and the electrical disconnection portion 13f disposed on the first sidewall of the end part 16b. The physical disconnection portion 14d is disposed along the inner peripheral wall of the connection part 16c and provides a non-conductive state between the electrical disconnection portion 13g disposed on the second sidewall of the extension part 16a and the electrical disconnection portion 13h disposed on the second sidewall of the end part 16b.

[0093] In this manner, in the extended electrode portion 15b provided symmetrically with the extended electrode portion 15a, the electrical disconnection portion 13e, the physical disconnection portion 14c, the electrical disconnection portions 13f and 13h, the physical disconnection portion 14d, and the electrical disconnection portion 13g are disposed in this order on the sidewalls extending between the source side select gate electrode SG disposed along the first sidewall 11 of the memory gate electrode MG and the drain side select gate electrode DG disposed along the second sidewall 12 of the memory gate electrode MG. Accordingly, the extended electrode portion 15b prevents conduction between the source side select gate electrode SG and the

drain side select gate electrode DG through the four electrical disconnection portions 13e, 13f, 13h, and 13g and the two physical disconnection portions 14c and 14d. [0094] Since the memory cell formation part 3b adjacent to the memory cell formation part 3a shares the drain region WD between the memory cell formation part 3b and the memory cell formation part 3a, the second sidewall 12 of the memory gate electrode MG, on which the drain side select gate electrode DG is disposed, is disposed facing the second sidewall 12 of the memory gate electrode MG in the memory cell formation part 3a.

[0095] The memory cell formation part 3b includes an extended electrode portion 15c, the end part 16b of which is disposed on the adjacent memory cell formation part 3a side in the electrical disconnection region ER2 and the physical disconnection region ER1. The memory cell formation part 3b includes an extended electrode portion 15d, the end part 16b of which is disposed on the adjacent memory cell formation part 3c side in the electrical disconnection region ER4 and the physical disconnection region ER5.

[0096] With this Configuration, in a region between the memory cell formation part 3a on the first row and the memory cell formation part 3b on the second column, the end part 16b and the connection part 16c of the extended electrode portion 15c in the memory cell formation part 3b on the second row are disposed in the electrical disconnection region ER2 and the physical disconnection region ER1, and the end part 16b and the connection part 16c of the extended electrode portion 15b in the memory cell formation part 3a on the first row are disposed in the electrical disconnection region ER4 and the physical disconnection region ER5.

[0097] In this manner, in the non-volatile semiconductor memory device 1, the end part 16b of the memory cell

formation part 3a and the end part 16b of the memory cell formation part 3b are disposed side by side in the row direction between the adjacent memory cell formation parts 3a and 3b to avoid area increase due to the two end parts 16b arranged in line in the column direction between the adjacent memory cell formation parts 3a and 3b, thereby achieving downsizing and highly dense integration.

[0098] In the memory cell formation part 3a, the cap film CP is disposed on the memory gate electrode MG in the select gate formation region ER9 and on the extension part 16a and the end part 16b as extension of the memory gate electrode MG in the electrical disconnection regions ER2 and ER4. With this configuration, in the memory cell formation part 3a, the cap film CP prevents salicidation of upper surfaces of the memory gate electrode MG, the extension part 16a, and the end part 16b through a manufacturing process.

[0099] In the physical disconnection regions ER1 and ER5, no cap film CP is disposed on the connection parts 16c as extension of the memory gate electrode MG, and thus the connection parts 16c are externally exposed so that upper surfaces of the connection parts 16c are salicided. A column-shaped memory gate contact MGC is provided on the connection parts 16c for each, through a silicide layer (not illustrated) disposed on each connection part 16c. The memory gate contact MGC is connected with the memory gate line MGL (FIG. 2) to receive a predetermined voltage from the memory gate line MGL. With this configuration, the voltage applied to the memory gate line MGL is applied from the memory gate contact MGC to the memory gate electrode MG in the select gate formation region ER9 through the extended electrode portions 15a and 15b.

[0100] In this manner, in the non-volatile semiconductor memory device 1, the memory gate electrode MG is covered

by the cap film CP in the memory cell region ER3 and the select gate contact regions ER6 and ER7. However, a predetermined voltage can be applied to the memory gate electrode MG covered by the cap film CP in the memory cell region ER3 by applying the predetermined voltage, through the memory gate contact MGC, to the connection parts 16c exposed in the physical disconnection regions ER1 and ER5.

[0101] The non-volatile semiconductor memory device 1 thus configured can be produced through a process of manufacturing a typical complementary MOS (CMOS) involving a deposition process, a resist applying process, an exposure and developing process, an etching process, an impurity injecting process, and a resist peeling process. Thus, the description of a method of manufacturing the non-volatile semiconductor memory device 1 is omitted below.

[0102] (1-5) Operations and effects

With the above-described configuration, the memory cell formation part 3a includes, in the electrical disconnection regions ER2 and ER4 and the physical disconnection regions ER1 and ER5, the extended electrode portions 15a and 15b as extension of the memory gate electrode MG in the select gate formation region ER9 in which the source side select gate structure 6a and the drain side select gate structure 5a are disposed facing each other.

[0103] In the memory cell formation part 3a, the four electrical disconnection portions 13a, 13b, 13d, and 13c (13e, 13f, 13h, and 13g) providing p-i-n junction structures between the source side select gate electrode SG and the drain side select gate electrode DG are provided along the sidewalls of the extended electrode portion 15a (15b).

[0104] In this manner, in the memory cell formation part 3a, the four electrical disconnection portions 13a, 13b, 13d, and 13c (13e, 13f, 13h, and 13g) for achieving disconnection between the source side select gate electrode SG and the drain side select gate electrode DG are provided along the sidewalls of the extended electrode portion 15a (15b). Accordingly, the source side select gate electrode SG and the drain side select gate electrode DG are disconnected from each other at the increased number of places as compared to conventional cases, thereby preventing any false reading operation occurring due to voltage variation at a data reading operation as compared to conventional cases.

[0105] In the memory cell formation part 3a, the physical disconnection portion 14b (14a) to which no sidewall-shaped semiconductor material is provided is provided between electrical disconnection portions 13a and 13b (13b and 13d) disposed along the sidewalls of the extended electrode portion 15a. Accordingly, the physical disconnection portion 14b (14a) prevents contact between the source side select gate electrode SG and the drain side select gate electrode DG, thereby achieving a non-conductive state. In this manner, the memory cell formation part 3a additionally includes the physical disconnection portion 14b (14a) disconnecting the source side select gate electrode SG and the drain side select gate electrode DG in a manner different from that for the electrical disconnection portions 13a, 13b, 13d, and 13c. This configuration achieves more reliable disconnection between the source side select gate electrode SG and the drain side select gate electrode DG than a case in which only the electrical disconnection portions 13a, 13b, 13d, and 13c are provided.

[0106] In addition, in the memory cell formation part 3a, the extended electrode portion 15a (15b) bends at the

physical disconnection region ER1 (ER5) so that the plurality of electrical disconnection portions 13a, 13b, 13d, and 13c (13e, 13f, 13h, and 13g) are disposed in parallel to each other in the electrical disconnection region ER2 (ER4). With this configuration, in the memory cell formation part 3a, increase in a layout region of the memory cell formation part 3a can be prevented in the longitudinal direction even when the electrical disconnection portions 13a, 13b, 13d, and 13c (13e, 13f, 13h, and 13g) are provided in the extended electrode portion 15a (15b).

[0107] (2) Planar layout of non-volatile semiconductor memory device according to second embodiment

In the above-described embodiment, the extended electrode portion 15a (15b) including the four electrical disconnection portions 13a, 13b, 13d, and 13c (13e, 13f, 13h, and 13g) is described as an extended electrode portion including three or more electrical disconnection portions. However, the present invention is not limited thereto. When including three or more electrical disconnection portions, any extended electrode portion may have various kinds of configurations. For example, FIG. 5, in which any part corresponding to that in FIG. 4 is denoted by an identical reference sign, illustrates a planar layout of a non-volatile semiconductor memory device 21 according to a second embodiment having a configuration in which each extended electrode portion 25a (25b) includes six electrical disconnection portions 23a, 23b, 23c, 23f, 23e, and 23d.

[0108] Memory cell formation parts 22a, 23b, 23c, ... all have identical configurations, and thus the following description will be made mainly on the memory cell formation part 22a. Duplicate description of any part corresponding to that in FIG. 4 will be omitted in the following. In the present embodiment, the extended

electrode portion 25a (25b) of the memory cell formation part 22a is E-shaped when viewed from above the semiconductor substrate. The extended electrode portion 25a (25b) extends from the end of the select gate formation region ER9 to the physical disconnection region ER1 (ER5) through the electrical disconnection region ER2 (ER4), and separately bends toward the first sidewall 11 side and the second sidewall 12 side of the memory gate electrode MG from the memory gate electrode MG in the physical disconnection region ER1 (ER5) before returning to the electrical disconnection region ER2 (ER4).

[0109] The extended electrode portion 25a (25b) includes an extension part 26a extending straight from the memory gate electrode MG in the select gate formation region ER9, straight end parts 26b and 26c disposed laterally outside of the extension part 26a, and a connection part (non-sidewall formation part) 26d connecting the extension part 26a and the end parts 26b and 26c. The extension part 26a and the end parts 26b and 26c are disposed in the electrical disconnection region ER2 (ER4), and the connection part 26d as a turning part is disposed in the physical disconnection region ER1 (ER5).

[0110] In the present embodiment, in the extended electrode portion 25a (25b), the end part 26b is disposed on the first sidewall 11 side of the memory gate electrode MG, and the end part 26c is disposed on the second sidewall 12 side of the memory gate electrode MG.

[0111] The memory gate electrode MG extends as the extended electrode portion 25a (25b) from the select gate formation region ER9 to the electrical disconnection region ER2 (ER4), but the source side select gate electrode SG and the drain side select gate electrode DG do not extend to the electrical disconnection region ER2 (ER4) unlike the select gate formation region ER9. The six electrical disconnection portions 23a, 23b, 23c, 23f,

23e, and 23d are each disposed on sidewalls of the extended electrode portion 25a (25b) in place of the source side select gate electrode SG and the drain side select gate electrode DG.

[0112] The electrical disconnection portions 23a, 23b, 23c, 23f, 23e, and 23d all have identical configurations and each includes the i-type sidewall-shaped intrinsic semiconductor layers Ia and Ib and the sidewall-shaped opposite-conductivity-type semiconductor layer OC. The opposite-conductivity-type semiconductor layer OC is disposed between the intrinsic semiconductor layers Ia and Ib. As described above, the opposite-conductivity-type semiconductor layer OC is of a conductivity type (in this case, p-type) different from a conductivity type of the source side select gate electrode SG and the drain side select gate electrode DG.

[0113] In this case, in the extension part 26a of the extended electrode portion 25a (25b), the electrical disconnection portion 23a is disposed along a first sidewall continuously provided flush with the first sidewall 11 of the memory gate electrode MG, and the electrical disconnection portion 23d is disposed along a second sidewall continuously provided flush with the second sidewall 12 of the memory gate electrode MG. In the memory cell formation part 22a, for example, the electrical disconnection portion 23a provides a p-i-n junction along the first sidewall 11 of the memory gate electrode MG and the sidewall of the extension part 26a from the n-type source side select gate electrode SG as a starting point. Similarly, in the second sidewall 12 side of the memory gate electrode MG of the memory cell formation part 22a, for example, the electrical disconnection portion 23d provides a p-i-n junction along the second sidewall 12 and the sidewall of the extension

part 26a from the n-type drain side select gate electrode DG as a starting point.

[0114] In addition, in the end part 26b disposed on the first sidewall 11 side of the memory gate electrode MG, the electrical disconnection portion 23b is disposed on a sidewall facing the extension part 26a, and the electrical disconnection portion 23c is disposed on a sidewall disposed outside. In the end part 26c disposed on the second sidewall 12 side of the memory gate electrode MG, the electrical disconnection portion 23e is disposed on a sidewall facing the extension part 26a, and the electrical disconnection portion 23f is disposed on a sidewall disposed outside.

[0115] Accordingly, in the extended electrode portion 25a (25b), the six the electrical disconnection portions 23a, 23b, 23c, 23f, 23e, and 23d are disposed in this order on the sidewalls extending between the source side select gate electrode SG disposed along the first sidewall 11 of the memory gate electrode MG and the drain side select gate electrode DG disposed along the second sidewall 12 of the memory gate electrode MG. With this configuration, three or more opposite-conductivity-type semiconductor layers and intrinsic semiconductor layers are provided on the sidewalls of the extended electrode portions 25a and 25b.

[0116] Accordingly, for example, even when a foreign object adheres to the electrical disconnection portion 23a of the extension part 26a or the connection part 26d to be described later, providing electrical conduction between the source side select gate electrode SG and the electrical disconnection portion 23b of the end part 26b, the source side select gate electrode SG and the drain side select gate electrode DG are electrically insulated from each other through the p-i-n junctions provided by

the other electrical disconnection portions 23b, 23d, 23f, 23e, and 23d.

[0117] In addition to this configuration, in the connection part 26d as a non-sidewall formation part in the physical disconnection region ER1, a physical disconnection portion 24b is disposed on an inner peripheral wall connecting the first sidewall of the extension part 26a with a sidewall of the end part 26b on the first sidewall 11 side, a physical disconnection portion 24c is disposed on an inner peripheral wall connecting the second sidewall of the extension part 26a with a sidewall of the end part 26c on the second sidewall 12 side, and a physical disconnection portion 24a is disposed on an outer peripheral wall connecting sidewalls of the end parts 26b and 26c.

[0118] In the physical disconnection portions 24a, 24b, and 24c, no conduction layer made of, for example, a semiconductor material is provided along outer and inner peripheral walls of the connection part 26d so that the outer and inner peripheral walls of the connection part 26d are externally exposed. With this configuration, the physical disconnection portions 24a, 24b, and 24c each provides physical disconnection through a gap between the source side select gate electrode SG and the drain side select gate electrode DG, thereby achieving a non-conductive state between the source side select gate electrode SG and the drain side select gate electrode DG.

[0119] In the present embodiment, the first physical disconnection portion 24a is disposed along the outer peripheral wall of the connection part 26d provided continuously with the sidewalls of the end parts 26b and 26c, and provides a non-conductive state between the electrical disconnection portions 23c and 23f through a gap between the electrical disconnection portion 23c disposed on a sidewall of the end part 26b and the

electrical disconnection portion 23f disposed on a sidewall of the end part 26c. The second physical disconnection portion 24b is disposed along the inner peripheral wall of the connection part 26d provided continuously with the sidewalls of the extension part 26a and the end part 26b, and provides a non-conductive state between the electrical disconnection portions 23a and 23b through a gap between the electrical disconnection portion 23a disposed on a sidewall of the extension part 26a and the electrical disconnection portion 23b disposed on a sidewall of the end part 26b. In addition, the third physical disconnection portion 24c is disposed along the inner peripheral wall of the connection part 26d provided continuously with the sidewalls of the extension part 26a and the end part 26c, and provides a non-conductive state between the electrical disconnection portions 23d and 23e through a gap between the electrical disconnection portion 23d disposed on a sidewall of the extension part 26a and the electrical disconnection portion 23e disposed on a sidewall of the end part 26c. [0120] In this manner, in the extended electrode portion 25a (25b), the electrical disconnection portion 23a, the physical disconnection portion 24b, electrical disconnection portions 23b and 23c, the physical disconnection portion 24a, electrical disconnection portions 23f and 23e, the physical disconnection portion 24c and the electrical disconnection portion 23d are disposed in this order on the sidewalls extending between the source side select gate electrode SG disposed along the first sidewall 11 of the memory gate electrode MG and the drain side select gate electrode DG disposed along the second sidewall 12 of the memory gate electrode MG. Accordingly, the extended electrode portion 15a prevents conduction between the source side select gate electrode SG and the drain side select gate electrode DG through

the six the electrical disconnection portions 23a, 23b, 23c, 23f, 23e, and 23d and the three physical disconnection portions 24b, 24a, and 24c.

[0121] With the above-described configuration, in the memory cell formation part 22a, the six the electrical disconnection portions 23a, 23b, 23c, 23f, 23e, and 23d for achieving disconnection between the source side select gate electrode SG and the drain side select gate electrode DG are provided along the sidewalls of the extended electrode portion 25a (25b). Accordingly, the source side select gate electrode SG and the drain side select gate electrode DG are disconnected from each other at the increased number of places as compared to conventional cases, thereby preventing any false reading operation occurring due to voltage variation at a data reading operation as compared to conventional cases.

[0122] In the memory cell formation part 22a, the physical disconnection portions 24b, 24a, and 24c to which no sidewall-shaped semiconductor material is provided are provided between the electrical disconnection portions 23a and 23b, between the electrical disconnection portions 23c and 23f, and between the electrical disconnection portions 23e and 23d, which are disposed along the sidewalls of the extended electrode portion 25a (25b), so that the three physical disconnection portions 24b, 24a, and 24c prevent contact between the source side select gate electrode SG and the drain side select gate electrode DG, thereby achieving a non-conductive state. In this manner, the memory cell formation part 22a additionally includes the physical disconnection portions 24b, 24a, and 24c, which disconnect the source side select gate electrode SG and the drain side select gate electrode DG in a manner different from that for the electrical disconnection portions 23a, 23b, 23c, 23f, 23e, and 23d. This

configuration achieves more reliable disconnection between the source side select gate electrode SG and the drain side select gate electrode DG than a case in which only the electrical disconnection portions 23a, 23b, 23c, 23f, 23e, and 23d are provided.

[0123] In the memory cell formation part 22a, the extended electrode portion 25a (25b) bends at the physical disconnection region ER1 (ER5) so that the plurality of electrical disconnection portions 23a, 23b, 23c, 23f, 23e, and 23d are all disposed in parallel to each other in the electrical disconnection region ER2 (ER4). With this configuration, increase in a layout region of the memory cell formation part 22a can be prevented in the longitudinal direction.

[0124] (3) Planar layout of non-volatile semiconductor memory device according to third embodiment

In the non-volatile semiconductor memory device 1 according to the above-described embodiments, the extended electrode portions 15a and 15b are provided as parts of the memory cell formation parts 3a, 3b, and 3c and independent between the memory cell formation parts 3a, 3b, and 3c. However, the present invention is not limited thereto. For example, as illustrated in FIG. 6, in which any part corresponding to that in FIG. 4 is denoted by an identical reference sign, a non-volatile semiconductor memory device 31 may include extended electrode portions 35a and 35b separately from memory cell formation parts 32a, 32b, 32c, ... so that the memory cell formation parts 32a, 32b, 32c, ... are provided continuously with each other through the extended electrode portions 35a and 35b.

[0125] In this case, the memory cell formation part 32a (32b or 32c) includes the select gate formation region ER9 in which the source side select gate structure 6a (6b or 6c) and the drain side select gate structure 5a (5b or

5c) are disposed facing each other with the memory gate structure 4a (4b or 4c) interposed therebetween. In the memory gate structures 4a, 4b, and 4c of the respective memory cell formation parts 32a, 32b, and 32c, the memory gate electrode MG extending in the row direction is provided in the select gate formation region ER9, and the cap film CP is disposed on the memory gate electrode MG.

[0126] In the present embodiment, the drain region WD disposed on the well W is shared by the memory cell formation part 32a on the first row and the memory cell formation part 32b on the second row adjacent to the memory cell formation part 32a on the first row.

Accordingly, an identical bit voltage is applied, through the drain region WD, to the memory cell 2a (2b or 2c) in the memory cell formation part 32a on the first row and the memory cell 2d (2e or 2f) in the memory cell formation part 32b on the second row. In this manner, since the memory cell formation part 32b on the second row adjacent to the memory cell formation part 32a on the first row shares the drain region WD disposed between the memory cell formation part 32b and the memory cell formation part 32a on the first row, the second sidewall 12 of the memory gate electrode MG, on which the drain side select gate electrode DG is disposed, is disposed facing the second sidewall 12 of the memory gate electrode MG in the memory cell formation part 32a on the first row.

[0127] In addition to this configuration, the memory gate electrode MG disposed in each of the memory cell formation parts 32a, 32b, 32c, ... extends to the electrical disconnection region ER2 (ER4) and the physical disconnection region ER1 (ER5) from the select gate formation region ER9, forming the extended electrode portions 35a and 35b in the electrical disconnection region ER2 (ER4) and the physical disconnection region

ER1 (ER5). In the present embodiment, the extended electrode portions 35a and 35b each has a comb teeth shape when viewed from above the semiconductor substrate, and include an extension part 36a as straight extension of the memory gate electrode MG in each of the memory cell formation parts 32a, 32b, 32c, ..., and a straight end part 36b disposed laterally outside of the extension part 36a. The extension part 36a and the end part 36b are alternately arranged along the column direction in which the memory cell formation parts 32a, 32b, 32c, ... are arranged. The extension part 36a and the end part 36b are disposed in the electrical disconnection regions ER2 and ER4 and continuously provided through connection parts (non-sidewall formation parts) 36c disposed in the physical disconnection regions ER1 and ER5.

[0128] The following description of the extended electrode portions 35a and 35b will be made mainly on the memory cell formation part 32b on the second row. The second sidewall 12 of the memory gate electrode MG, on which the drain side select gate electrode DG is disposed, in the memory cell formation part 32b on the second row is provided continuously with the second sidewall 12 of the memory gate electrode MG, on which the drain side select gate electrode is disposed, in the adjacent memory cell formation part 32b on the first row, through inner sidewalls of the extended electrode portions 35a and 35b.

[0129] In the present embodiment, four electrical disconnection portions 33a, 33b, 33c, and 33d are disposed in this order along sidewalls of the extended electrode portions 35a and 35b between the second sidewall 12 of the memory gate electrode MG in the memory cell formation part 32b on the second row and the second sidewall 12 of the memory gate electrode MG in the memory cell formation part 32a on the first row. In the extended electrode portions 35a and 35b, the electrical

disconnection portion 33a is disposed along a sidewall of the extension part 36a disposed flush with the second sidewall 12 of the memory gate electrode MG in the memory cell formation part 32b on the second row, and the electrical disconnection portion 33d is disposed along a sidewall of the extension part 36a disposed flush with the second sidewall 12 of the memory gate electrode MG in the memory cell formation part 32a on the first row.

[0130] In the end part 36b of each of the extended electrode portions 35a and 35b extending in the row direction between the memory cell formation part 32a on the first column and the memory cell formation part 32b on the second column, the electrical disconnection portion 33c is disposed along a sidewall disposed on the memory cell formation part 32a side on the first row, and the electrical disconnection portion 33b is disposed along a sidewall disposed on the memory cell formation part 32b side on the second row. In this manner, the four electrical disconnection portions 33a, 33b, 33c, and 33d are disposed in this order along sidewalls of each of the extended electrode portions 35a and 35b connecting the second sidewall 12 of the memory gate electrode MG in the memory cell formation part 32b on the second row with the second sidewall 12 of the memory gate electrode MG in the memory cell formation part 32a on the first row.

With this configuration, three or more opposite-conductivity-type semiconductor layers and intrinsic semiconductor layers are provided on the sidewalls of the extended electrode portions 35a and 35b.

[0131] In addition to this configuration, the physical disconnection portion 34c is disposed on, for example, an inner peripheral wall of the connection part 36c in the physical disconnection region ER1, which connects a sidewall of the extension part 36a provided continuously with the memory cell formation part 32b on the second row

with a sidewall of the end part 36b between the memory cell formation part 32b on the second row and the memory cell formation part 32a on the first row. The physical disconnection portion 34b is disposed on, for example, an inner peripheral wall of the connection part 36c in the physical disconnection region ER1, which connects a sidewall of the extension part 36a provided continuously with the memory cell formation part 32a on the first row with a sidewall of the end part 36b between the memory cell formation part 32a on the first row and the memory cell formation part 32b on the second row.

[0132] In the physical disconnection portions 34b and 34c, no conduction layer made of, for example, a semiconductor material is provided along the inner peripheral wall of the connection part 36c so that the inner peripheral wall of the connection part 36c is externally exposed. With this configuration, the physical disconnection portions 34b and 34c each provides physical disconnection through a gap between the drain side select gate electrode DG in the memory cell formation part 32a on the first row and the drain side select gate electrode DG in the memory cell formation part 32b on the second row, thereby achieving a non-conductive state between the drain side select gate electrode DG in the memory cell formation part 32a on the first row and the drain side select gate electrode DG in the memory cell formation part 32b on the second row.

[0133] In this manner, in the extended electrode portions 35a and 35b, the electrical disconnection portion 33a, the physical disconnection portion 34c, the electrical disconnection portions 33b and 33c, the physical disconnection portion 34b, and the electrical disconnection portion 33d are disposed in this order on sidewalls between the drain side select gate electrode DG in the memory cell formation part 32b on the second row

and the drain side select gate electrode DG in the memory cell formation part 32a on the first row. Accordingly, the extended electrode portions 35a and 35b prevent conduction between the drain side select gate electrode DG in the memory cell formation part 32a on the first row and the drain side select gate electrode DG in the memory cell formation part 32b on the second row through the four electrical disconnection portions 33a, 33b, 33c, and 33d and the two physical disconnection portions 34b and 34c.

[0134] In the extended electrode portions 35a and 35b, the end parts 36b extend from the connection parts 36c, respectively, in the physical disconnection regions ER1 and ER5 to the electrical disconnection regions ER2 and ER4, and are disposed in the region between the memory cell formation parts 32a and 32b adjacent to each other. This configuration prevents increase of the electrical disconnection regions ER2 and ER4 in the longitudinal directions of the memory cell formation parts 32a and 32b by an amount corresponding to the end parts 36b.

[0135] The source region WS disposed on the well W is shared by the memory cell formation part 32b on the second row and the memory cell formation part 32c on the third row adjacent to the memory cell formation part 32b on the second row. Accordingly, an identical source voltage is applied to the memory cells 2d, 2e, and 2f in the memory cell formation part 32b on the second row and the memory cells 2g, 2h, and 2i in the memory cell formation part 32c on the third row. In this manner, since the memory cell formation part 32b on the second row adjacent to the memory cell formation part 32c on the third row shares the source region WS between the memory cell formation part 32b and the memory cell formation part 32c on the third row, the first sidewall 11 of the memory gate electrode MG, on which the source side select

gate electrode SG is disposed, is disposed facing the first sidewall 11 of the memory gate electrode MG in the memory cell formation part 32c on the third row.

[0136] With this configuration, the first sidewall 11 of the memory gate electrode MG, on which the source side select gate electrode SG is disposed, in the memory cell formation part 32b on the second row is provided continuously, through inner sidewalls of the extended electrode portions 35a and 35b, with the first sidewall 11 of the memory gate electrode MG, on which the source side select gate electrode SG is disposed, in the adjacent memory cell formation part 32c on the third row.

[0137] In the present embodiment, four electrical disconnection portions 33e, 33f, 33g, and 33h are disposed in this order along sidewalls each of the extended electrode portions 35a and 35b between the first sidewall 11 of the memory gate electrode MG in the memory cell formation part 32b on the second row and the first sidewall 11 of the memory gate electrode MG in the memory cell formation part 32c on the third row. In each of the extended electrode portions 35a and 35b, the electrical disconnection portion 33e is disposed along a sidewall of the extension part 36a disposed flush with the first sidewall 11 of the memory gate electrode MG in the memory cell formation part 32b on the second row, and the electrical disconnection portion 33h is disposed along a sidewall of the extension part 36a disposed flush with the first sidewall 11 of the memory gate electrode MG in the memory cell formation part 32c on the third row.

[0138] In the end part 36b of each of the extended electrode portions 35a and 35b extending in the row direction between the memory cell formation part 32b on the second column and the memory cell formation part 32c on the third column, the electrical disconnection portion 33f is disposed along a sidewall disposed on the memory

cell formation part 32b side on the second row, and the electrical disconnection portion 33g is disposed along a sidewall disposed on the memory cell formation part 32c side on the third row. In this manner, the four electrical disconnection portions 33e, 33f, 33g, and 33h are disposed in this order along sidewalls of the extended electrode portions 35a and 35b connecting the first sidewall 11 of the memory gate electrode MG in the memory cell formation part 32b on the second row with the first sidewall 11 of the memory gate electrode MG in the memory cell formation part 32c on the third row.

[0139] In addition to this configuration, in the connection part 36c in the physical disconnection region ER1, for example, the physical disconnection portion 34e is disposed on an inner peripheral wall connecting a sidewall of the extension part 36a provided continuously with the memory cell formation part 32b on the second row with a sidewall of the end part 36b between the memory cell formation part 32b on the second row and the memory cell formation part 32c on the third row. Similarly, in the connection part 36c in the physical disconnection region ER1, for example, the physical disconnection portion 34d is disposed on an inner peripheral wall connecting a sidewall of the extension part 36a provided continuously with the memory cell formation part 32c on the third row with a sidewall of the end part 36b between the memory cell formation part 32c on the third row and the memory cell formation part 32b on the second row.

[0140] In the physical disconnection portions 34e and 34d, no conduction layer made of, for example, a semiconductor material is provided along the inner peripheral wall of the connection part 36c so that the inner peripheral wall of the connection part 36c is externally exposed. With this configuration, the physical disconnection portions 34e and 34d each provides physical disconnection through

a gap between the source side select gate electrode SG in the memory cell formation part 32b on the second row and the source side select gate electrode SG in the memory cell formation part 32c on the third row, thereby achieving a non-conductive state between the source side select gate electrode SG in the memory cell formation part 32b on the second row and the source side select gate electrode SG in the memory cell formation part 32c on the third row.

[0141] In this manner, the electrical disconnection portion 33e, the physical disconnection portion 34e, the electrical disconnection portions 33f and 33g, the physical disconnection portion 34d, and the electrical disconnection portion 33h are disposed in this order on sidewalls of the extended electrode portions 35a and 35b between the source side select gate electrode SG in the memory cell formation part 32b on the second row and the source side select gate electrode SG in the memory cell formation part 32c on the third row. Accordingly, the extended electrode portions 35a and 35b prevent conduction between the source side select gate electrode SG in the memory cell formation part 32b on the second row and the source side select gate electrode SG in the memory cell formation part 32c on the third row through the four electrical disconnection portions 33e, 33f, 33g, and 33h and the two physical disconnection portions 34e and 34d.

[0142] In the non-volatile semiconductor memory device 31, the cap film CP is disposed on the memory gate electrodes MG in the memory cell formation parts 32a, 32b, 32c, ..., the extension parts 36a as extension of the memory gate electrode MG in the electrical disconnection regions ER2 and ER4, and the end parts 36b in the electrical disconnection regions ER2 and ER4. The cap film CP prevents salicidation of upper surfaces of the memory

gate electrode MG, the extension part 36a, and the end part 36b through a manufacturing process. In the physical disconnection regions ER1 and ER5, no cap film CP is disposed on the connection parts 36c as extension of the memory gate electrode MG, and thus the connection parts 36c are externally exposed so that upper surfaces of the connection parts 36c are salicided. The column-shaped memory gate contact MGC is provided on the connection parts 36c for each, through a silicide layer (not illustrated) disposed on each connection part 36c. [0143] With the above-described configuration, in the non-volatile semiconductor memory device 31, the four electrical disconnection portions 33a, 33b, 33c, and 33d for achieving disconnection between the drain side select gate electrode DG the memory cell formation parts 32a and 32b adjacent to each other are provided along first sidewalls of the extended electrode portions 35a and 35b. Accordingly, the drain side select gate electrodes DG are disconnected from each other at the increased number of places as compared to conventional cases, thereby preventing any false reading operation occurring due to voltage variation at a data reading operation as compared to conventional cases.

[0144] In the non-volatile semiconductor memory device 31, the four electrical disconnection portions 33e, 33f, 33g, and 33h for achieving disconnection between the source side select gate electrodes SG of the memory cell formation parts 32b and 32c adjacent to each other are provided along second sidewalls of the extended electrode portions 35a and 35b. Accordingly, the source side select gate electrodes SG are disconnected from each other at the increased number of places as compared to conventional cases, thereby preventing any false reading operation occurring due to voltage variation at a data reading operation as compared to conventional cases.

[0145] For example, in the region between the memory cell formation parts 32a and 32b adjacent to each other, the physical disconnection portions 34c and 34b, to which no sidewall-shaped semiconductor material is provided, are provided between the electrical disconnection portions 33a and 33b and between electrical disconnection portions 33c and 33d, which are disposed along sidewalls of the extended electrode portions 35a and 35b, so that the two physical disconnection portions 34c and 34b prevent contact between the drain side select gate electrodes DG, thereby achieving a non-conductive state. In this manner, the region between the memory cell formation parts 32a and 32b additionally includes the physical disconnection portions 34c and 34b, which disconnect the drain side select gate electrodes DG in a manner different from that for the electrical disconnection portions 33a, 33b, 33c, and 33d. This configuration achieves more reliable disconnection between the drain side select gate electrodes DG than a case in which only the electrical disconnection portions 33a, 33b, 33c, and 33d are provided. Similarly, the region between the memory cell formation parts 32b and 32c adjacent to each other additionally includes the physical disconnection portions 34e and 34d, which disconnect the source side select gate electrode SG in a manner different from that for the electrical disconnection portions 33e, 33f, 33g, and 33h. This configuration achieves more reliable disconnection between the source side select gate electrode SG than a case in which only the electrical disconnection portions 33e, 33f, 33g, and 33h are provided.

[0146] In addition, the extended electrode portion 35a (35b) turns around in the physical disconnection region ER1 (ER5) toward the electrical disconnection region ER2 (ER4) and provides the end part 36b between the memory cell formation parts 32a and 32b adjacent to each other.

With the extension part 36a and the end part 36b disposed in the electrical disconnection region ER2 (ER4), the plurality of electrical disconnection portions 23a, 23b, 23c, 23f, 23e, and 23d are all disposed in parallel to each other in the electrical disconnection region ER2 (ER4). Accordingly, increase of the electrical disconnection region ER2 (ER4) can be prevented in the longitudinal direction of the memory cell formation part 32a due to the end part 36b in the non-volatile semiconductor memory device 31, thereby achieving downsizing and highly dense integration.

[0147]In the non-volatile semiconductor memory device 31, for example, when a foreign object remains along a sidewall of the extended electrode portion 35a provided continuously with the first sidewall 11 of each memory gate electrode MG between the memory cell formation parts 32b and 32c adjacent to each other due to manufacturing defect, the source side select gate electrodes SG in the memory cell formation parts 32b and 32c adjacent to each other can be electrically connected with each other. In this case, since an identical voltage is applied to each source side select gate electrode SG in the non-volatile semiconductor memory device 31 at data reading operation, voltage variation can be prevented in the source side select gate electrodes SG and the drain side select gate electrodes DG due to short-circuit defect at data reading operation even when the source side select gate electrodes SG in the memory cell formation parts 32b and 32c are electrically connected with each other.

[0148]In the non-volatile semiconductor memory device 31, for example, when a foreign object remains along a sidewall of the extended electrode portion 35a provided continuously with the second sidewall 12 of each memory gate electrode MG between the memory cell formation parts 32a and 32b adjacent to each other due to manufacturing

defect, the drain side select gate electrodes DG in the memory cell formation parts 32a and 32b adjacent to each other can be electrically connected with each other. In this case, in the non-volatile semiconductor memory device 31, since the drain side select gate electrodes DG of the same kind to which an identical voltage is likely to be applied at data reading operation can be electrically connected with each other, the probability of generation of voltage variation in the drain side select gate electrodes DG at data reading operation can be reduced.

[0149] (4) Planar layout of non-volatile semiconductor memory device according to fourth embodiment

In the non-volatile semiconductor memory device 31 according to the above-described third embodiment, the memory cell formation parts 32a, 32b, 32c, ... are provided continuously with each other in the physical disconnection regions ER1 and ER5, but the present invention is not limited thereto. As illustrated in FIG. 7, in which any part corresponding to that in FIG. 4 is denoted by an identical reference sign, a non-volatile semiconductor memory device 41 may include connection regions ER10 and ER11 provided separately from the physical disconnection regions ER1 and ER5 so that memory cell formation parts 42a and 42b adjacent to each other are provided continuously with each other in the connection regions ER10 and ER11.

[0150] In this case, the memory cell formation part 42a (42b) includes the select gate formation region ER9 in which the source side select gate structure 6a (6b) and the drain side select gate structure 5a (5b) are disposed facing each other with the memory gate structure 4a (4b) interposed therebetween. The memory gate structures 4a and 4b are each provided with the straight memory gate electrode MG extending in the row direction in the memory

cell formation parts 42a and 42b in the select gate formation region ER9, and the cap film CP is disposed on the memory gate electrode MG.

[0151] In addition to this configuration, the non-volatile semiconductor memory device 41 includes the connection regions ER10 and ER11 adjacent to the select gate formation region ER9, and the physical disconnection region ER1 (ER5) at an end of the connection region ER10 (ER11) through the electrical disconnection region ER2 (ER4). In this case, the memory gate electrode MG extends as an extended electrode portion 45a (45b) in the connection region ER10 (ER11), the electrical disconnection region ER2 (ER4), and the physical disconnection region ER1 (ER5).

[0152] The source region WS disposed on the well W is shared by the memory cell formation parts 42a and 42b adjacent to each other so that an identical source voltage is applied from the source region WS to the memory cells 2d, 2e, and 2f in the memory cell formation part 42a and the memory cells 2g, 2h, and 2i in the memory cell formation part 42b. The first sidewalls 11 of the memory gate electrodes MG in the memory cell formation parts 42a and 42b adjacent to each other are disposed facing each other, and the sidewall-shaped source side select gate electrodes SG are disposed facing each other along the first sidewalls 11.

[0153] In addition to this configuration, ends of the memory gate electrodes MG in the memory cell formation parts 42a and 42b adjacent to each other are provided continuously with each other through the extended electrode portions 45a and 45b in the connection regions ER10 and ER11. When viewed from above the semiconductor substrate, the extended electrode portions 45a and 45b have E shapes that are reflectively symmetric with respect to the center of each memory cell formation part

in the connection regions ER10 and ER11, the electrical disconnection regions ER2 and ER4, and the physical disconnection regions ER1 and ER5. In this case, the extended electrode portions 45a, 45b include a forked connection part 46a provided in the connection regions ER10, ER11 and connecting the memory gate electrodes MG in the memory cell formation parts 43a and 42b, extension parts 46b and 46f provided in the electrical disconnection regions ER2, ER4 and extending from the forked connection part 46a along the longitudinal directions of the memory gate electrodes MG, an end part 46d provided in the electrical disconnection regions ER2, ER4 and disposed between the extension parts 46b and 46f, and non-sidewall formation parts 46c, 46g, and 46e provided in the physical disconnection regions ER1, ER5 and disposed at leading ends of the extension parts 46b and 46f and the end part 46d.

[0154] In the memory cell formation parts 42a and 42b adjacent to each other, the first sidewall 11 of the memory gate electrode MG in the memory cell formation part 42a and the first sidewall 11 of the memory gate electrode MG in the memory cell formation part 42b are provided continuously with each other through sidewalls 47a of the forked connection parts 46a in the connection regions ER10 and ER11. Sidewall-shaped semiconductor layers 11a are disposed along the sidewalls 47a of the forked connection parts 46a so that the source side select gate electrode SG in the memory cell formation part 42a and the source side select gate electrode SG in the memory cell formation part 42b are provided continuously with each other through the semiconductor layers 11a.

[0155] In each forked connection part 46a, the wide select gate contact formation part Ca provided with the source side select gate contact SGC is disposed at a

predetermined position on the semiconductor layer 11a. The select gate contact formation part Ca includes a mounting portion over the forked connection part 46a and a plane portion having a plane surface along the semiconductor substrate. The plane portion is provided with the column-shaped source side select gate contact SGC connected with a source side select gate line (not illustrated). With this configuration, a predetermined voltage is applied from the source side select gate line SGL to the source side select gate electrode SG having a tilted sidewall shape with a small width through the source side select gate contact SGC and the select gate contact formation part Ca.

[0156] In the present embodiment, the plane portion of the select gate contact formation part Ca is disposed in the select gate contact regions ER6, ER7, and the mounting portion thereof is disposed in the connection regions ER10, ER11. In the above-described embodiment, the select gate contact formation part Ca is provided to the semiconductor layer 11a in the forked connection part 46a, but the present invention is not limited thereto. The select gate contact formation part Ca may be provided to the source side select gate electrode SG in the select gate contact regions ER6, ER7.

[0157] In the forked connection part 46a, sidewall-shaped semiconductor layers 11b are disposed on C-shaped sidewalls 47b and 47c facing the sidewall 47a provided with the select gate contact formation part Ca. The semiconductor layers 11b remains on the C-shaped sidewalls 47b and 47c of the forked connection part 46a at formation of the source side select gate electrodes SG and the drain side select gate electrodes DG of the memory cell formation parts 42a and 42b.

[0158] In addition to this configuration, in each of the memory cell formation parts 42a and 42b, the sidewall-

shaped drain side select gate electrode DG is disposed along the second sidewall 12 facing the first sidewall 11 of the memory gate electrode MG and disposed in the drain region WD side on the well W. For example, the memory cell formation part 42a shares the drain region WD with an adjacent memory cell formation part (not illustrated), and thus a bit voltage same as that applied to the memory cell 2d in the memory cell formation part 42a is also applied to a memory cell in the adjacent memory cell formation part (not illustrated).

[0159] No source side select gate electrode SG nor drain side select gate electrode DG is disposed on sidewalls of the extension parts 46b and 46f and the end part 46d provided in the electrical disconnection region ER2 (ER4). Instead, six electrical disconnection portions 43a, 43b, 43c, 43f, 43e, and 43d are disposed along these sidewalls. The electrical disconnection portions 43a, 43b, 43c, 43f, 43e, and 43d all have identical configurations and each includes the i-type sidewall-shaped intrinsic semiconductor layers Ia and Ib and the sidewall-shaped opposite-conductivity-type semiconductor layer OC. The opposite-conductivity-type semiconductor layer OC is disposed between the intrinsic semiconductor layers Ia and Ib. The opposite-conductivity-type semiconductor layer OC has a conductivity type (in this case, p-type) different from a conductivity type of the source side select gate electrode SG and the drain side select gate electrode DG.

[0160] In the extension part 46b of the extended electrode portion 45a (45b), the electrical disconnection portion 43a is disposed along a first sidewall provided continuously flush with the second sidewall 12 of the memory gate electrode MG in the memory cell formation part 42a, and the electrical disconnection portion 43b is disposed along a second sidewall disposed facing the

first sidewall. In the memory cell formation part 42a, for example, the electrical disconnection portion 43a provides a p-i-n junction along the second sidewall 12 of the memory gate electrode MG and sidewalls of the forked connection part 46a and the extension part 46b from the n-type drain side select gate electrode DG as a starting point.

[0161] In the extension part 46f of the extended electrode portion 45a (45b), the electrical disconnection portion 43f is disposed along a first sidewall provided continuously flush with the second sidewall 12 of the memory gate electrode MG in the memory cell formation part 42b, and the electrical disconnection portion 43e is disposed along a second sidewall disposed facing the first sidewall. In the memory cell formation part 42b, for example, the electrical disconnection portion 43f provides a p-i-n junction along the second sidewall 12 of the memory gate electrode MG and sidewalls of the forked connection part 46a and the extension part 46f from the n-type drain side select gate electrode DG as a starting point.

[0162] The end part 46d of the extended electrode portion 45a (45b) extends straight from the forked connection part 46a in the longitudinal directions of the extension parts 46b and 46f, and is disposed between the extension parts 46b and 46f. In the end part 46d, the electrical disconnection portion 43c is disposed on a sidewall facing the extension part 46b, and the electrical disconnection portion 43d is disposed on a sidewall facing the extension part 46f. Accordingly, the six electrical disconnection portions 43a, 43b, 43c, 43d, 43e, and 43f are disposed in this order on a sidewall of the extended electrode portion 45a (45b) between the drain side select gate electrode DG disposed along the second sidewall 12 of the memory gate electrode MG in the memory

cell formation part 42a and the drain side select gate electrode DG disposed along the second sidewall 12 of the memory gate electrode MG in the memory cell formation part 42b. With this configuration, three or more opposite-conductivity-type semiconductor layers and intrinsic semiconductor layers are provided on sidewalls of the extended electrode portions 45a and 45b.

[0163] Accordingly, for example, the electrical disconnection portion 43c provides a p-i-n junction along a sidewall of the end part 16b even when foreign objects adhere to the electrical disconnection portions 43a and 43b of the extension part 46b and the non-sidewall formation part 46c of the extension part 46b to be described later, providing electrical conduction through the drain side select gate electrode DG, the electrical disconnection portions 43a and 43b, the non-sidewall formation part 46c, the semiconductor layers 11b on the sidewall 47b, and the electrical disconnection portion 43c of the end part 46d in the memory cell formation part 42a due to the foreign objects.

[0164] In addition to this configuration, physical disconnection portions 44a, 44b, and 44c are disposed on sidewalls of the non-sidewall formation parts 46c, 46e, and 46g in the physical disconnection region ER1. In the physical disconnection portions 44a, 44b, and 44c, no conduction layer made of, for example, a semiconductor material is provided along the sidewalls of the non-sidewall formation parts 46c, 46e, and 46g so that the sidewalls of the non-sidewall formation parts 46c, 46e, and 46g are externally exposed. With this configuration, the physical disconnection portions 44a, 44b, and 44c provide physical disconnection through gaps between the drain side select gate electrode DG in the memory cell formation part 42a and the drain side select gate electrode DG in the memory cell formation part 42b,

thereby achieving a non-conductive state between the drain side select gate electrodes DG.

[0165] In this manner, the electrical disconnection portion 43a, the physical disconnection portion 44a, the electrical disconnection portions 43b and 43c, the physical disconnection portion 44b, the electrical disconnection portions 43d and 43e, the physical disconnection portion 44c, and the electrical disconnection portion 43f are disposed in this order on sidewalls of the extended electrode portion 45a (45b) between the drain side select gate electrode DG disposed along the second sidewall 12 of the memory gate electrode MG in the memory cell formation part 42a and the drain side select gate electrode DG disposed along the second sidewall 12 of the memory gate electrode MG in the memory cell formation part 42b. Accordingly, the extended electrode portion 45a (45b) prevents conduction between the drain side select gate electrodes DG through the six electrical disconnection portions 43a, 43b, 43c, 43d, 43e, and 43f, and the three the physical disconnection portions 44a, 44b, and 44c.

[0166] With the above-described configuration, in the non-volatile semiconductor memory device 41, the six electrical disconnection portions 43a, 43b, 43c, 43d, 43e, and 43f for achieving disconnection between the drain side select gate electrode DG in the memory cell formation part 42a and the drain side select gate electrode DG in the memory cell formation part 42b are provided along the sidewalls of the extended electrode portion 45a (45b). Accordingly, the drain side select gate electrodes DG are disconnected from each other at the increased number of places as compared to conventional cases, thereby preventing any false reading operation occurring due to voltage variation at a data reading operation as compared to conventional cases.

[0167] The physical disconnection portions 44a, 44b, and 44c, to which no sidewall-shaped semiconductor material is provided, are provided between the electrical disconnection portions 43a and 43b, between the electrical disconnection portions 43c and 43d, and between the electrical disconnection portions 43e and 43f, which are disposed along the sidewalls of the extended electrode portion 45a (45b), so that the three physical disconnection portions 44a, 44b, and 44c prevent contact between the drain side select gate electrodes DG, thereby achieving a non-conductive state. In this manner, the memory cell formation parts 42a and 42b adjacent to each other each additionally include the physical disconnection portions 44a, 44b, and 44c, which disconnect the drain side select gate electrodes DG in a manner different from that for electrical disconnection portions 43a, 43b, 43c, 43d, 43e, and 43f. This configuration achieves more reliable disconnection between the drain side select gate electrodes DG than a case in which only the electrical disconnection portions 43a, 43b, 43c, 43d, 43e, and 43f are provided.

[0168] In the memory cell formation parts 42a and 42b adjacent to each other in this manner, the extended electrode portion 45a (45b) bends at the physical disconnection region ER1 (ER5) and provides the end part 46d and the extension parts 46b and 46f in the electrical disconnection region ER2 (ER4) so that the plurality of electrical disconnection portions 43a, 43b, 43c, 43d, 43e, and 43f are all disposed in parallel to each other in the electrical disconnection region ER2 (ER4) through the end part 46d and the extension parts 46b and 46f. With this configuration, in the non-volatile semiconductor memory device 41, the end part 46d is not disposed in line with the extension parts 46b and 46f, and accordingly, increase of the electrical disconnection region ER2 (ER4)

can be prevented in the longitudinal directions of the memory cell formation parts 42a and 42b.

[0169] In the non-volatile semiconductor memory device 41, for example, even when foreign objects remain along sidewalls of the extended electrode portions 45a provided continuously with the second sidewalls 12 of the memory gate electrodes MG between the memory cell formation parts 42a and 42b adjacent to each other due to manufacturing defect, the drain side select gate electrodes DG of the memory cell formation parts 42a and 42b adjacent to each other can be electrically connected with each other. In this case, in the non-volatile semiconductor memory device 41, since the drain side select gate electrodes DG of the same kind to which an identical voltage is likely to be applied at data reading operation can be electrically connected with each other, the probability of generation of voltage variation in the drain side select gate electrodes DG at data reading operation can be reduced.

[0170] In the above-described third embodiment, the electrical disconnection portions 43a, 43b, 43c, 43d, 43e, and 43f disconnecting electrical connection between the drain side select gate electrode DG in the memory cell formation part 42a and the drain side select gate electrode DG in the memory cell formation part 42b are applied as electrical disconnection portions disconnecting electrical connection between the first select gate electrode in a memory cell formation part and the first select gate electrode or the second select gate electrode in another memory cell formation part. However, the present invention is not limited thereto. An electrical disconnection portion disconnecting electrical connection between the source side select gate electrode of a memory cell formation part and the source side select gate electrode in another memory cell formation

part may be applied. In this case, those memory cell formation parts have such a configuration that each drain side select gate electrode DG and the corresponding source side select gate electrode SG illustrated in FIG. 7 are interchanged with each other.

[0171] In another embodiment, an electrical disconnection portion disconnecting electrical connection between the drain side select gate electrode in a memory cell formation part and the source side select gate electrode in another memory cell formation part may be applied. In this case, these memory cell formation parts do not share the source region WS but have such a configuration that the drain side select gate electrode DG of the memory cell formation part 42b illustrated in FIG. 7 is replaced with a source side select gate electrode SG.

[0172] (5) Other embodiments

The present invention is not limited to the present embodiments, but various kinds of modifications are possible without departing from the scope of the present invention. For example, various voltage values may be applied to each site. In the above-described first and second embodiments, the first select gate electrode disposed on the first sidewall of a memory gate electrode is the source side select gate electrode SG, but the present invention is not limited thereto. A drain side select gate electrode may be disposed as the first select gate electrode on the first sidewall of a memory gate electrode. In this case, the second select gate electrode disposed on the second sidewall of the memory gate electrode is a source side select gate electrode.

[0173] In the above-described embodiments, the electrical disconnection portions 13a, 13b, 13d, 13c (13e, 13f, 13h, 13g), 23a, 23b, 23c, 23f, 23e, 23d, 33a, 33b, 33c, 33d, 43a, 43b, 43c, 43d, 43e, and 43f, which provide p-i-n junctions, are each provided from the drain side select

gate electrode DG or the source side select gate electrode SG as a starting point, but the present invention is not limited thereto. Electrical disconnection portions for achieving an n-i-n junction structure, a p-i-p junction structure, an n-p-n junction structure, or a p-n-p junction structure may be provided with the drain side select gate electrode DG or the source side select gate electrode SG as a starting point or with electrical disconnection portions alone. Specifically, three or more opposite-conductivity-type semiconductor layers of a conductivity type different from a conductivity type of the first select gate electrode and the second select gate electrode, or three or more intrinsic semiconductor layers are desirably provided on sidewalls of an extended electrode portion extending from a memory gate electrode. In this case, a physical disconnection portion at which no semiconductor layer is disposed on a sidewall of the extended electrode portion is desirably disposed between opposite-conductivity-type semiconductor layers adjacent to each other or intrinsic semiconductor layers adjacent to each other.

[0174] In the above-described first, second, third, and fourth embodiments, the physical disconnection regions ER1, ER5 are provided, but the present invention is not limited thereto. Only the electrical disconnection regions ER2, ER4 may be provided without the physical disconnection regions ER1 and ER5.

[0175] In the above-described embodiments, the extended electrode portions 15a, 15b, 15c, 15d, 25a, 25b, 35a, 35b, 45a, and 45b each has a C shape, an E shape, or a comb teeth shape when viewed from above the semiconductor substrate, but the present invention is not limited thereto. The extended electrode portions may have various kinds of shapes such as an F shape, an H shape, a

J shape, a K shape, an L shape, an M shape, an N shape, a T shape, a U shape, a V shape, a W shape, a Y shape, and a Z shape.

[0176] In the above-described embodiments, the P-type well W is used to provide the memory gate structure 4a included in an N-type transistor structure, the drain side select gate structure 5a included in an N-type MOS transistor structure, and the source side select gate structure 6a included in an N-type MOS transistor structure, but the present invention is not limited thereto. An N-type well may be used to provide a memory gate structure included in a P-type transistor structure, a drain side select gate structure included in a P-type MOS transistor structure, and a source side select gate structure included in a P-type MOS transistor structure. In this case, the polarity of N-type or P-type is inverted in the memory cell 2a described in the above-described embodiments, and thus, for example, voltages applied to a memory gate structure, a drain side select gate structure, a source side select gate structure, a bit line, and a source line change accordingly.

[0177] In the above-described embodiments, for example, in the memory cell 2a, data is programmed by injecting charge into the charge storage layer EC and data is erased by removing charge in the charge storage layer EC, but the present invention is not limited thereto. Contrary to the above configuration, data may be programmed by removing charge in the charge storage layer EC of the memory cell 2a, and data may be erased by injecting charge into the charge storage layer EC.

[0178] In the above-described embodiments, a cap film disposed on the top portion of the memory gate electrode MG is the cap film CP having a laminated structure in which the upper cap layer CPb made of an insulation material, such as SiN, different from the insulation

material of the lower cap film CPa is stacked on the lower cap film CPa, but the present invention is not limited thereto. The cap film may be a single-layer cap film or a cap film having a laminated structure including three or more layers.

[0179] The four electrical disconnection portions 13a, 13b, 13d, and 13c (13e, 13f, 13h, and 13g) are provided to the extended electrode portions 15a, 15b, and 15c, 15d in the above-described first embodiment, the six electrical disconnection portions 23a, 23b, 23c, 23f, 23e, and 23d are provided to the extended electrode portions 25a and 25b in the above-described second embodiment, the four electrical disconnection portions 33a, 33b, 33c, and 33d are provided to the extended electrode portions 35a and 35b in the above-described third embodiment, and the six electrical disconnection portions 43a, 43b, 43c, 43d, 43e, and 43f are provided to the extended electrode portions 45a and 45b in the above-described fourth embodiment, but the present invention is not limited thereto. Three or more electrical disconnection portions only have to be provided at various positions on extended electrode portions. In addition, the number of electrical disconnection portions and the shapes thereof may be different between extended electrode portions on both sides of a memory gate electrode so that the electrical disconnection portions may be asymmetrically disposed with respect to the memory gate electrode.

[0180] (6) Positional relation between electrical and physical disconnection regions

In the above-described first to third embodiments, the electrical disconnection region ER2 (ER4) and the physical disconnection region ER1 (ER5) are provided in this order from the select gate formation region ER9 on each side of the select gate formation region ER9, but the present invention is not limited thereto. The

electrical disconnection region ER2 (ER4) and the physical disconnection region ER1 (ER5) may be disposed at interchanged positions so that the physical disconnection region ER1 (ER5) and the electrical disconnection region ER2 (ER4) may be provided in this order from the select gate formation region ER9 on each side of the select gate formation region ER9.

[0181] For example, FIG. 8, in which any part corresponding to that in FIG. 5 is denoted by an identical reference sign, illustrates a planar layout of a memory cell formation part 52 in which the electrical disconnection region ER2 (ER4) and the physical disconnection region ER1 (ER5) of the memory cell formation part 22a illustrated in FIG. 5 are interchanged. In this case, in the memory cell formation part 52, a physical disconnection region ER11 is disposed at one end of the select gate formation region ER9, a physical disconnection region ER15 is disposed at the other end of the select gate formation region ER9, and an electrical disconnection region ER12 (ER14) is disposed at an end of the physical disconnection region ER11 (ER15).

[0182] In the memory cell formation part 52, the strip-shaped memory gate electrode MG extends in the select gate formation region ER9, and an extended electrode portion 55a (55b) as extension of the memory gate electrode MG from the select gate formation region ER9 is provided in the physical disconnection region ER11 (ER15) and the electrical disconnection region ER12 (ER14). In the present embodiment, the extended electrode portion 55a (55b) has a leading end in a trifurcated fork shape when viewed from above the semiconductor substrate, and includes a connection part 56d disposed in the physical disconnection region ER11 (ER15), and an extension part 56a and end parts 56b and 56c disposed in the electrical disconnection region ER12 (ER14).

[0183] In this case, the connection part 56d includes a basal part 57a extending in the physical disconnection region ER11 (ER15) from an end of the memory gate electrode MG in the select gate formation region ER9, and a fork part 57b trifurcated from the basal part 57a. The extension part 56a is disposed at a center fork part of the fork part 57b, and the end parts 56b and 56c are disposed at both end fork parts of the fork part 57b.

[0184] The connection part 56d as a non-sidewall formation part in the physical disconnection region ER1 includes four physical disconnection portions 54a, 54b, 54c, and 54d. The physical disconnection portion 54a is disposed on an outer peripheral wall connecting the first sidewall 11 of the memory gate electrode MG with a sidewall of the end part 56b. The physical disconnection portion 54b is disposed on an outer peripheral wall connecting the sidewall of the end part 56b with a sidewall of the extension part 56a. The physical disconnection portion 54c is disposed on an outer peripheral wall connecting another sidewall of the extension part 56a with a sidewall of the end part 56c. The physical disconnection portion 54d is disposed on an outer peripheral wall connecting the sidewall of the end part 56c with the second sidewall 12 of the memory gate electrode MG.

[0185] In the physical disconnection portions 54a, 54b, 54c, and 54d, no conduction layer made of, for example, a semiconductor material is provided along an outer peripheral wall of the connection part 56d so that the outer peripheral wall of the connection part 56d is externally exposed. With this configuration, the physical disconnection portions 54a, 54b, 54c, and 54d provide physical disconnection through gaps between the source side select gate electrode SG disposed along the first sidewall 11 of the memory gate electrode MG and the

drain side select gate electrode DG disposed along the second sidewall 12 of the memory gate electrode MG, thereby achieving a non-conductive state between the source side select gate electrode SG and the drain side select gate electrode DG. No cap film CP is disposed on the connection part 56d of the extended electrode portion 55a (55b) in the physical disconnection region ER11 (ER15), and the memory gate contact MGC is provided at a predetermined position of the connection part 56d.

[0186] Six electrical disconnection portions 53a, 53b, 53c, 53d, 53e, and 53f are disposed in the electrical disconnection region ER12 (ER14). The electrical disconnection portions 53c and 53d are disposed on facing sidewalls of the extension part 56a disposed on an extended line along the memory gate electrode MG in the select gate formation region ER9. The electrical disconnection portions 53a and 53b are disposed on facing sidewalls of the end part 56b disposed laterally outside of the extension part 56a. The electrical disconnection portions 53e and 53f are disposed on facing sidewalls of the end part 56c disposed laterally outside of the extension part 56a. Similarly to the memory gate electrode MG in the select gate formation region ER9, the cap film CP is disposed on the extension part 56a and the end parts 56b and 56c of the extended electrode portion 55a (55b) in the electrical disconnection region ER12 (ER14).

[0187] The electrical disconnection portions 53a, 53b, 53c, 53d, 53e, and 53f all have identical configurations and each includes the i-type sidewall-shaped intrinsic semiconductor layers Ia and Ib and the sidewall-shaped opposite-conductivity-type semiconductor layer OC. The opposite-conductivity-type semiconductor layer OC are disposed between the intrinsic semiconductor layers Ia and Ib. The opposite-conductivity-type semiconductor

layer OC has a conductivity type (in this case, p-type) different from a conductivity type of the source side select gate electrode SG and the drain side select gate electrode DG.

[0188] Accordingly, for example, even when a foreign object adheres to the connection part 56d, providing conduction between the source side select gate electrode SG and the electrical disconnection portion 53a of the end part 56b, the electrical disconnection portion 53a provides a p-i-n junction along the first sidewall 11 of the memory gate electrode MG and the sidewall of the end part 56b from the n-type source side select gate electrode SG as a starting point, thereby blocking current from the source side select gate electrode SG at the electrical disconnection region ER2 (ER4).

[0189] in addition, for example, even when a foreign object adheres to the electrical disconnection portion 53a of the end part 56b in addition to the connection part 56d, providing conduction between the source side select gate electrode SG and the electrical disconnection portion 53b of the end part 56b, the electrical disconnection portion 53b of the end part 56b provides a p-i-n junction along the first sidewall 11 of the memory gate electrode MG and the sidewall of the end part 56b from the n-type source side select gate electrode SG as a starting point, thereby blocking current from the source side select gate electrode SG at the electrical disconnection region ER2 (ER4).

[0190] Similarly to the above-described embodiments, in the memory cell formation part 52, the six electrical disconnection portions 53a, 53b, 53c, 53d, 53e, and 53f for achieving disconnection between the source side select gate electrode SG and the drain side select gate electrode DG are provided along sidewalls of the extended electrode portion 55a (55b). Accordingly, the source

side select gate electrode SG and the drain side select gate electrode DG are disconnected from each other at the increased number of places as compared to conventional cases, thereby preventing any false reading operation occurring due to voltage variation at a data reading operation as compared to conventional cases.

[0191] In the memory cell formation part 52 illustrated in FIG. 8, the memory gate contact MGC is formed on the connection part 56d in the physical disconnection region ER1 provided between the select gate formation region ER9 and the electrical disconnection region ER12 (ER14) through a manufacturing process, and thus a sufficient positioning margin for the memory gate contact MGC needs to be provided in both of the select gate formation region ER9 and the electrical disconnection region ER12 (ER14).

[0192] In the memory cell formation part 22a according to the second embodiment illustrated in FIG. 5, however, a sufficient positioning margin for the memory gate contact MGC needs to be provided only in the electrical disconnection region ER2 (ER4), and thus the physical disconnection region ER1 (ER5) can have a reduced width as compared to a case with the memory cell formation part 52 illustrated in FIG. 8 accordingly and can be formed in a compact size as compared to the case with the memory cell formation part 52 illustrated in FIG. 8.

[0193] Although the above description is made on the memory cell formation part 52 including the trifurcated extended electrode portions 55a and 55b, the present invention is not limited thereto. Each extended electrode portion may be a bifurcated extended electrode portions or an extended electrode portion forked into four or more, and may have various shapes such as an F shape and a Y shape. A plurality of electrical disconnection portions can be disposed on a fork part of

such an extended electrode portion, and thus, similarly to the above-described embodiments, the source side select gate electrode SG and the drain side select gate electrode DG can be disconnected from each other at the increased number of places as compared to conventional cases.

[0194] In the non-volatile semiconductor memory device 41 according to the above-described fourth embodiment illustrated in FIG. 7, the electrical disconnection region ER2 (ER4) and the physical disconnection region ER1 (ER5) may be disposed at interchanged positions so that the physical disconnection region ER1 (ER5) and the electrical disconnection region ER2 (ER4) are provided in this order on each side of the connection regions ER10 and ER11. In such a case, the non-sidewall formation parts 46c, 46e, and 46g are provided at an end of the forked connection part 46a, the extension part 46b is provided at a leading end of the non-sidewall formation part 46c, the end part 46d is provided at a leading end of the non-sidewall formation part 46e, and the extension part 46f is provided at a leading end of the non-sidewall formation part 46g. With this configuration, similarly to the above-described embodiments, the number of the electrical disconnection portions 43a, 43b, 43c, 43d, 43e, and 43f can be increased, and accordingly, the source side select gate electrode SG and the drain side select gate electrode DG can be disconnected from each other at the increased number of places as compared to conventional cases.

Reference Signs List

[0195] 1, 21, 31, 41 non-volatile semiconductor memory device

2a, 2b, 2c, 2d, 2e, 2f, 2g, 2h, 2i, 2j memory cell

3a, 3b, 3c, 3d, 22a, 22b, 22c, 32a, 32b, 32c, 42a,
42b, 52 memory cell formation part
4a, 4b, 4c memory gate structure
5a, 5b, 5c drain side select gate structure
6a, 6b, 6c source side select gate structure
11 first sidewall
12 second sidewall
15a, 15b, 15c, 15d, 25a, 25b, 35a, 35b, 45a, 45b,
55a, 55b extended electrode portion
CP cap film
ER9 select gate formation region
MG memory gate electrode
DG drain side select gate electrode
SG source side select gate electrode

Claims

1. A non-volatile semiconductor memory device comprising a plurality of memory cell formation parts, wherein each memory cell formation part includes:
 - a first select gate structure including a first select gate electrode on a well of a semiconductor substrate through a first select gate insulating film;
 - a second select gate structure including a second select gate electrode on the well through a second select gate insulating film;
 - a memory gate structure provided between the first select gate structure and the second select gate structure through sidewall spacers and including a lower gate insulating film, a charge storage layer, an upper gate insulating film, and a memory gate electrode stacked on the well in this order; and
 - an extended electrode portion as an extension portion extending from the memory gate electrode in a select gate formation region in which the first select gate structure and the second select gate structure are disposed facing each other, and
 - three or more opposite-conductivity-type semiconductor layers of a conductivity type different from a conductivity type of the first select gate electrode and the second select gate electrode, or three or more intrinsic semiconductor layers are provided on sidewalls of the extended electrode portion.
2. A non-volatile semiconductor memory device comprising a plurality of memory cell formation parts, wherein
 - each memory cell formation part includes:

a first select gate structure including a first select gate electrode on a well of a semiconductor substrate through a first select gate insulating film;

a second select gate structure including a second select gate electrode on the well through a second select gate insulating film;

a memory gate structure provided between the first select gate structure and the second select gate structure through sidewall spacers and including a lower gate insulating film, a charge storage layer, an upper gate insulating film, and a memory gate electrode stacked on the well in this order, and

an extended electrode portion as an extension portion extending from the memory gate electrode in a select gate formation region in which the first select gate structure and the second select gate structure are disposed facing each other connects one memory cell formation part and the other memory cell formation part, and

three or more opposite-conductivity-type semiconductor layers of a conductivity type different from a conductivity type of the first select gate electrode and the second select gate electrode, or three or more intrinsic semiconductor layers are provided on sidewalls of the extended electrode portion.

3. The non-volatile semiconductor memory device according to claim 1 or 2, wherein

the extended electrode portion includes:

an extension part extending from the memory gate electrode in the select gate formation region;

an end part having straight shape that includes a sidewall disposed facing a sidewall of the extension part and is disposed in parallel to the extension part; and

a connection part connecting the extension part and the end part, and

the opposite-conductivity-type semiconductor layers or the intrinsic semiconductor layers are disposed along the sidewalls of the extension part and the end part.

4. The non-volatile semiconductor memory device according to any one of claims 1 to 3, wherein a physical disconnection portion in which no semiconductor layer is disposed on a sidewall of the extended electrode portion is disposed between the opposite-conductivity-type semiconductor layers adjacent to each other or between the intrinsic semiconductor layers adjacent to each other.

5. The non-volatile semiconductor memory device according to claim 4, wherein

a cap film is provided on an upper surface of the memory gate electrode, but no cap film is provided and a memory gate contact is provided on an upper surface of the extended electrode portion in a physical disconnection region in which the physical disconnection portion is disposed.