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CIRCUITRY FOR REDUCING DEMODULATION PHASE ERROR AS FOR AN AUTOMATIC DEGHOSTING SYSTEM

The present invention relates to circuitry for reducing demodulation phase error in a system for processing radio frequency signals which may include multipath distortion components. The circuitry substantially compensates for phase errors in the demodulated composite video signals that are caused by the multipath distortion components.

Television reception has long been plagued by multipath distortion, the reception of undesired multiple signals. These undesired signals, reflected from buildings and other large objects or resulting from poorly terminated cable networks, appear as delayed versions of the direct television signal and are commonly referred to as ghost signals.

The ghost signals are delayed from the direct signal as a function of the relationship of the signal path lengths between the direct and ghost signals. The randomness of this relationship from one receiver location to another dictates that the phase of the ghost (delayed direct) carrier signal may have any relationship to the phase of the direct carrier signal.

In many automatic deghosting systems the incoming television signals are synchronously demodulated in phase with the picture carrier signal. Exemplary systems of this type are described in the article entitled "Adaptive Multipath Equalization for T.V. Broadcasting", IEEE Transactions on Consumer Electronics, May 1977, pp. 175-181 by H. Thedick; U.S. Patent No. 4,285,006 entitled, "Ghost Cancellation Circuit System"; and U.S. Patent No. 4,374,400 entitled "Television Ghost Cancellation System with Ghost Carrier Phase Compensation".

In a typical system of this type, the picture carrier signal is extracted from the modulated television signals provided by the intermediate frequency (IF) amplifier. This carrier signal is used to synchronize a

phase locked loop (PLL) which provides a regenerated carrier signal. A synchronous detector is responsive to this regenerated carrier signal and to the modulated television signals provided by the IF amplifier to develop two baseband signals, I and Q, representing, respectively, the in-phase and quadrature phase modulation components of the IF signals. The I and Q signals are used by the system to cancel, respectively, the in-phase and quadrature phase ghost signal components of the synchronously demodulated I signal.

When the incoming television signals include a relatively strong ghost signal component having a delayed direct carrier phase that is not the same as the carrier phase of the direct signal, the direct signal components of the I and Q signals developed by this method may be distorted. This distortion may occur because the IF carrier signal of the incoming television signal is the vector sum of the direct and delayed direct (ghost) carrier signals and, consequently, has a different phase than the direct carrier signal.

When the extracted carrier signal is used to synchronously demodulate the television signals provided by the IF amplifier, the resulting baseband signals are distorted by crosstalk from the quadrature component of the modulated television signals. Since television signals are vestigal sideband modulated signals, this quadrature component is the Hilbert transform of the in-phase components having frequencies greater than 1 MHz. The distortion caused by this quadrature component may appear as excessive peaking of vertical edges in the reproduced image or as an apparent loss of horizontal resolution depending on whether the quadrature component tends to reinforce or cancel the respective in-phase component.

In accordance with the principles of the present invention, circuitry is provided for reducing demodulation phase error in a system for processing radio frequency television signals. The system includes an input terminal

for applying a radio frequency television signal having a direct signal component including a direct carrier signal and a delayed direct signal component including a delayed direct carrier signal. The radio frequency television signal includes a carrier signal which is a vector sum of the direct carrier signal and the delayed direct carrier signal. Means are coupled to said input terminal for extracting the carrier signal from the radio frequency television signal. Further means are coupled to the carrier signal extracting means and includes phase locked loop circuitry for generating an oscillatory signal having a frequency and phase determined by the extracted carrier signal. The phase locked loop circuitry including phase comparator means responsive to the extracted carrier signal and to the oscillatory signal for generating a phase difference signal representing the difference in phase between the oscillatory and extracted carrier signals. Detection means are coupled to the input terminal and are responsive to the radio frequency television signal and to the oscillatory signal for generating first (I) and second (Q) baseband signals each having direct and delayed direct signal components. The direct signal components of the first and second baseband signals may include reciprocal crosstalk distortion components. The baseband signals represent amplitude modulated information carried by the radio frequency television signal. Additional means are coupled to the detection means and are responsive to at least one of the baseband signals for generating a phase control signal proportional to the difference in phase between the direct carrier signal and the vector sum of the direct carrier signal and the delayed direct carrier signal. Finally a phase correction circuit is provided responsive to the phase control signal for modifying one of the phase difference signal and the first baseband signal to generate a modified first baseband signal having substantially reduced crosstalk distortion components.

In one embodiment of the present invention the phase correction circuit includes an adder and a voltage

controlled oscillator and the phase control signal tends to change the phase of the oscillatory signal in a sense to reduce the magnitude of the phase control signal.

In a further embodiment of the present invention the phase correction circuit includes means for generating a phase correction signal and means for combining the phase correction signal and the first baseband signal.

Figure 1 is a block diagram of a portion of a television receiver including an embodiment of the present invention;

Figure 2 is a block diagram of a demodulation phase error detector which may be used in the portion of the television receiver shown in Figure 1;

Figure 3 is a block diagram of a phase locked loop which may be used in the portion of the television receiver shown in Figure 1;

Figures 4A-4E are waveform diagrams of amplitude versus time that are useful in explaining the operation of the portion of the television receiver shown in Figure 1;

Figure 5 is a block diagram of an alternative demodulation phase error detector which may be used in the portion of the television receiver shown in Figure 1;

Figure 6 is a block diagram of a further embodiment of the present invention;

Figure 7 is a block diagram of a demodulation phase error detector which may be used with the embodiment of Figure 6; and

Figure 8 is a block diagram of a complex multiplier used in the embodiment of Figure 6.

Referring to Figure 1, RF signals are received by an antenna 8 and applied to tuner circuitry 10. The tuner circuitry 10, which may be of conventional design, heterodynes the RF signals with a signal developed by a local oscillator to develop IF signals, which include composite video signals modulating an IF carrier. These IF signals are applied to and amplified by an IF amplifier 12 and applied to carrier reference signal extracting circuitry 14. The circuitry 14 may, for example, be a

conventional band-pass filter having a narrow-bandwidth frequency response characteristic centered about the IF carrier frequency.

The signal provided by the circuitry 14 is the IF carrier signal to the relative exclusion of any modulation components. This carrier signal is applied to a phase locked loop (PLL) 16 which generates an oscillatory signal having the same frequency as, and locked in phase to the IF carrier signal. The PLL 16 is described in more detail in reference to Figure 3, below.

The signal generated by the PLL 16 is applied to one input terminal of a synchronous detector 18 and to 90° phase shifting circuitry 20. The circuitry 20 develops a signal that is quadrature phase related to the regenerated carrier signal provided by the PLL 16. This quadrature carrier signal is applied to one input terminal of a synchronous detector 22. The synchronous detectors 18 and 22 multiply the IF signal, also applied thereto from IF amplifier 12, by the respective in-phase and quadrature phase carrier signals. The detectors 18 and 20 thereby respectively generate baseband signals I and Q representing the in-phase and quadrature phase modulation signal components of the IF signals respectively.

The I and Q signals are applied to automatic deghosting circuitry 24. The deghosting circuitry 24, which may, for example, be similar to that set forth in the Thedick article or the U.S. patents referenced above, processes the I signal to substantially remove multipath distortion components and provides a deghosted signal, I', at its output terminal.

As set forth above, ghost signals having carrier phases which differ from the carrier phase of the direct signal may cause the carrier phase of the incoming signals to be different from that of the direct signal. The ghost signals will be a delayed direct signal component including a delayed direct carrier signal. This difference in phase propagates through the tuner 10 and IF amplifier 12 so the phase of the carrier signal extracted by the circuitry 14

may not match the phase of the IF carrier of the direct signal. The extracted carrier signal would be the vector sum of the direct carrier signal and the delayed direct carrier signal. Since the signals developed by the PLL 16 are locked in phase to the extracted carrier signal, the I signal developed by the synchronous detector 18 may include crosstalk components from the quadrature phase component of the direct signal. Also, the Q signal developed by the synchronous detector 22 may include crosstalk components from the in-phase component of the direct signal. Moreover, since the automatic deghosting circuitry 24 does not correct the crosstalk distortion, the signal I' provided by the deghoster 24 may also be distorted.

The effects of this distortion are shown in Figures 4A, 4B, 4D, and 4E. Figures 4A and 4B are waveform diagrams representing, respectively, the in-phase and quadrature phase components of the leading edge of the vertical synchronization pulse for the direct signal. The leading edge of vertical sync is a training signal generally used by automatic deghosting systems. None of the waveforms shown in Figures 4A-4E include any ghost signal components. In the present embodiment, the ghost signals causing the demodulation phase errors are assumed to be delayed from the direct signal by an amount of time greater than 2τ, the amount of time between the points A and B on the waveform 4B.

As shown in Figure 4A, the in-phase component of the direct signal is a smooth transition from a value corresponding to black level at C to a value corresponding to the sync tip level at D without change of direction. The waveform shown in Figure 4B is the quadrature phase component of the signal, the Hilbert transform of the components of signal shown in Figure 4A having frequencies greater than 1 MHz.

Figures 4D and 4E respectively show the effects of demodulation phase errors on the I and Q signals. In Figure 4D, the I waveform of the direct signal is no longer a smooth transition without change in direction from point

C' to D'. The Q waveform of Figure 4E has different levels before (A') and after (B') the leading edge of vertical sync. It is this distortion of the quadrature component of the leading edge of the vertical sync pulse that is used by the present embodiment of the invention to detect and correct demodulation phase errors.

Referring to Figure 1, the Q signal provided by the synchronous detector 22 is applied to one input terminal of a demodulation phase error detector 26. A signal VSYNC, which may, for example be generated by vertical synchronization signal separating circuitry (not shown) is applied to another input terminal of the demodulation phase error detector 26. The signal VSYNC is shown in Figure 4C. It may, for example, consist of a single pulse for each field which occurs substantially coincident with the leading edge of the vertical synchronization pulse component of the demodulated composite video signal.

Figure 2 is a block diagram of a demodulation phase error detector suitable for use as the detector 26. Q signals from the synchronous detector 22 are applied to the signal input port of sample and hold circuitry 210. The signal VSYNC is applied to a delay element 216 wherein it is delayed by an amount of time τ and applied to the control input terminal of the circuitry 210. The output of delay element 216 serves as a control input signal. The sample and hold circuitry 210 samples the Q signal when the control input signal is high and holds the value of this sample while the control signal is low. The value of the sample held by the circuitry 210 is applied to a first input terminal of a subtracter 218.

The Q input signal is also applied to a delay element 212 which provides a time delay substantially equal to 2τ time periods. The signal provided by the delay element 212 is applied to second sample and hold circuitry 214, which is also controlled by the delayed VSYNC signal provided by the delay element 216. The output sample value of the sample and hold circuitry 214 is applied to a second

input terminal of the subtractor 218. The subtractor 218 subtracts the sample value provided by the circuitry 214 from that provided by the circuitry 210 and applies the result to the PLL 16.

Figure 3 is a block diagram of a phase locked loop suitable for use as the PLL 16. Reference signals from the carrier reference signal extracting circuitry 14 of Figure 1 are applied to one input terminal of a phase comparator 310 and the output signal of a voltage controlled oscillator (VCO) 318 is applied to the other input terminal. The output signal of the phase comparator 310 is proportional to the difference in phase between these two signals. This phase difference signal is applied to one input terminal of an adder 312, the other input terminal of which is coupled to receive the output signal of the demodulation phase error detector 26 scaled by a factor K via the scaling circuitry 314.

The adder 312 applies the sum of the phase difference signal and the scaled phase error signal to the input terminal of a low-pass filter 316, the loop filter of the PLL. The low-pass filter 316 integrates the signals applied to its input terminal to produce a control signal for the VCO 318 at its output terminal. The VCO 318, which may be of conventional design, has a free running frequency approximately equal to the IF carrier frequency. The signals provided by the low-pass filter 316 adjust the frequency and phase of the signal produced by the VCO 318 until it has substantially the same frequency and phase as the direct carrier signal component of the IF signals. The output of the VCO 318 which as noted above is fed back to the phase comparator 310 serves as the output of the PLL 16.

To understand how this occurs, consider, once again the figures 4A-4E. The waveform 4B shows the portion of the demodulated quadrature signal, Q, corresponding to the leading edge of the vertical synchronization pulse when the signal provided by the PLL 16 has the same frequency and phase as the direct carrier signal. The points A and B

correspond to the values held by the sample and hold circuitry 214 and 210 respectively. Since these values are approximately equal, the signal provided by the demodulation phase error detector 26 to the PLL 16 is approximately equal to zero and does not contribute significantly to the phase error signal applied to the low pass filter 316 by the adder 312.

Alternatively, when the phase of the signal provided by the PLL 16 is not the same as the phase of the direct carrier signal, the corresponding points on the quadrature waveform, A' and B' of FIGURE 4E, have different values. In this instance, the values provided by the demodulation phase error detector 26 are non-zero and contribute significantly to the phase adjustment signal developed by the adder 312. As set forth above, this signal is integrated by the low-pass filter 316 to develop a frequency control signal for the VCO 318. The amplitude and polarity of the phase adjustment signal are controlled by the phase comparison circuitry 310 and the scaling circuitry 314 to ensure that the signal provided by the VCO 318 converges to the frequency and phase of the direct carrier signal.

As set forth above, the demodulation phase error signal used by this embodiment of the invention is the difference between the values of the Q signal before and after the leading edge of the vertical synchronization pulse. For this system to perform well for signals which may have different amplitudes, it is preferable for the television system to include automatic gain control (AGC) circuitry before the demodulation phase error detector 26. This circuitry ensures that phase errors of the same magnitude produce correction signals having substantially the same magnitude.

Figure 5 is a block diagram of a demodulation phase error detector which performs well without AGC circuitry. This demodulation phase error detector includes two circuits, 500 and 530, each of which is identical to the demodulation phase error detector illustrated in Figure

2. In this embodiment, the I signal is applied to the circuit 530. This connection is shown in Figure 1 by the dashed line from detector 18 to detector 26. The circuit 500 develops values at its output subtractor 518 representing the difference between the amplitude of the Q signal before and after the leading edge of vertical sync. The circuit 530 develops values at its output subtractor 528 representing the difference between the amplitude of the I signal before and after the leading edge of vertical sync.

The output signals from subtractors 518 and 528 are applied to a divider 540. In the divider 540, the difference between the Q signal amplitude values is divided by the difference between the I signal amplitude values. The value provided by the divider 540 is the tangent of the phase angle between the IF carrier and the direct carrier. This value is substantially independent of the range of amplitude values occupied by the I and Q signals. The values developed by the divider 540 are applied as demodulation phase error signals to the PLL 16 as set forth above.

Basic to understanding the operation of the demodulation phase error detector are the equations describing the synchronous demodulation of the in-phase, I', and quadrature phase, Q', components of a vestigial sideband modulated signal using a regenerated carrier which differs in phase from the carrier of the modulated signal by an angle θ. These well known equations may be expressed as:

$$I' = I \cos \theta - Q \sin \theta \qquad (1)$$

and

$$Q' = I \sin \theta + Q \cos \theta \qquad (2)$$

where I and Q are the baseband in-phase and quadrature phase components which would be obtained if the regenerated carrier had the same phase as the carrier of the desired signal. In this instance, the desired signal is the direct signal component of the IF television signal and θ is the phase angle by which the IF carrier of the combined direct

and delayed direct (ghost) television signal differs from the IF carrier of the direct signal. Using equation (2) the values of A' and B' of FIGURE 4E may be expressed as functions of the values A and B of FIGURE 4B and the values C and D of FIGURE 4A as:

$$A' = C \sin \theta + A \cos \theta \quad (3)$$

$$B' = D \sin \theta + B \cos \theta \quad (4)$$

Similarly, using equation (1), the values C' and D' of FIGURE 4D may be expressed as:

$$C' = C \cos \theta - A \sin \theta \quad (5)$$

$$D' = D \cos \theta - B \sin \theta \quad (6)$$

The output signal from the divider 540 of Figure 5 may be described by the equation:

$$\text{Tan } \theta = (B'-A')/(D'-C') \quad (7)$$

substituting the equations (3) through (6) into the equation (7) and combining like terms yields:

$$\text{Tan } \theta = ((D-C) \sin \theta + (B-A) \cos \theta)/((D-C) \cos \theta - (B-A) \sin \theta) \quad (8)$$

From figure 4B it is noted that A = B. This identity is substituted into the equation (8), yielding:

$$\text{Tan } \theta = (D-C) \sin \theta/(D-C) \cos \theta \quad (9)$$

the factors (D-C) in the numerator and denominator of equation (9) cancel, so the equation (9) becomes the well known identity:

$$\text{Tan } \theta = \sin \theta/\cos \theta \quad (10)$$

The embodiments described above are in terms of analog signals and analog circuitry. The embodiment illustrated in Figures 6-8 practices the present invention using digital signals and digital circuitry.

Referring to Figures 6-8, elements which are the same as those shown in Figures 1-5 are similarly numbered.

In these Figures, broad arrows represent busses for multiple-bit parallel digital signals and line arrows represent connections carrying analog signals or single bit digital signals. Depending on the processing speed of the devices, compensating delays may be required in certain of the signal paths. One skilled in the art of digital signal

processing circuit design would know where such delays would be needed in a particular system.

Referring to FIGURE 1, RF signals are received by the antenna 8 and applied to tuner circuitry 10. The tuner heterodynes the RF signals with a signal developed by a local oscillator (not shown) to develop IF signals which include composite video signals modulating an IF carrier. These IF signals are amplified by an IF amplifier 12 and applied to carrier reference signal extracting circuitry 14 in the same manner as explained with respect to Figure 1.

The signal provided by the circuitry 14 is the IF carrier signal to the relative exclusion of any modulation components. This carrier signal is applied to the phase locked loop (PLL) 16 which generates a relatively stable oscillatory signal that is locked in frequency and phase to the extracted carrier signal. As before, this oscillatory signal is applied to one input terminal of a synchronous detector 18 and to the 90° phase shifting circuitry 20. The circuitry 20 develops a signal that is quadrature phase related to the oscillatory signal provided by the PLL 16.

This quadrature oscillatory signal is applied to one input terminal of the synchronous detector 22. The signal provided by IF amplifier 12 is applied to a second input terminal of each of the synchronous detectors 18 and 22. The synchronous detectors 18 and 22 multiply the IF signal by the respective in-phase and quadrature phase oscillatory signals to generate respectively baseband signals I and Q. Signals I and Q represent, respectively, the in-phase and quadrature phase modulation components of the IF signals.

The I and Q signals from detectors 18 and 22 are applied to and digitized by analog to digital converters (ADC's) 626 and 624 respectively. The digitized I and Q signals are applied to a complex multiplier 628 and to a demodulation phase error detector 630. Also applied to the detector 630 is the VSYNC signal illustrated in Figure 4C. The demodulation phase error detector 630 and a read-only memory (ROM) 632 develop correction signals C_I and C_Q.

These signals are applied to multiplier 628 where they are combined with the digitized signals I and Q to develop respectively in-phase and quadrature phase signals, I' and Q' which are substantially free of direct signal crosstalk distortion components. The signals I' and Q' are applied to automatic deghosting circuitry 34. The deghosting circuitry 34, which may, for example, be similar to that set forth in the Thedick article or the U.S. Patents referenced above, processes the I' signal to substantially remove multipath distortion components and provides a deghosted signal I" at its output terminal.

FIGURE 7 is a block diagram of a demodulation phase error detector suitable for use as the detector 630. The detector shown in FIGURE 2 includes two sample difference circuits 700 and 730 which develop signals representing the difference between the sample values of the respective Q and I signals taken before and after the leading edge of vertical sync. Since the circuits 700 and 730 are identical, only one, 700, is described in detail.

Digital samples representing the signal Q are applied to the data input port of a register 710. The signal VSYNC, is applied to the delay element 716 wherein it is delayed by an amount of time, τ, and is applied to the clock input terminal (CK) of the register 710. The register 710 loads the sample value applied to its data input port coincident with the leading edge of the VSYNC pulse and holds this sample value until the next occurrence of a VSYNC pulse. The sample value held by the register 710 is applied to a first input terminal of a subtracter 718.

The digitized Q signal is also applied to a delay element 712 which provides a time delay substantially equal to an amount of time, 2τ. The signal provided by the delay element 712 is applied to a register 714, which is clocked by the delayed VSYNC signal provided by the delay element 716. The sample value held by the register 714 is applied to a second input terminal of the subtracter 718. The subtracter 718 subtracts the sample value held by the

register 714 from that held by the register 710 and applies the result to sample dividing circuitry 740.

The sample values provided by the circuitry 700 represents the difference between the amplitude of the Q signal before and after the leading edge of vertical sync (i.e. B'-A' in FIGURE 4E). The circuitry 730 similarly provides sample values from subtractor 728 representing the difference between the amplitude of the I signal before and after the leading edge of vertical sync (i.e. D'-C' in FIGURE 4D) to a second input port of the sample dividing circuitry 740.

In the sample dividing circuitry 740 the difference between the Q sample values (B'-A') is divided by the difference between the I sample values (D'-C'). The signal, PE, provided by the dividing circuitry 740, which corresponds to the output signal of the demodulation phase error detector 630, (FIGURE 6), is substantially equal to the tangent of the phase angle separating the extracted IF carrier and the direct IF carrier. This signal is similar to the signal described above with respect to Figure 5 as the output from the divider 540. The quations (1)-(10) similarly apply. This signal is applied to the ROM 632 which develops the correction signals C_I and C_Q that are applied to the complex multiplier 628.

The signal PE provided by the demodulation phase error detector 630 is applied to the address input port of ROM 632 which is programmed to provide two transfer functions, TC_I and TC_Q. The transfer function TC_I is equal to the cosine of the arctangent of the applied address code and TC_Q is equal to minus the sine of the arctangent of the applied address code. Since the address codes are equal to the tangent of θ, the transfer functions TC_I and TC_Q provide the correction signals C_I and C_Q:

$$C_I = \cos \theta \qquad (11)$$

$$C_Q = -\sin \theta. \qquad (12)$$

These correction signals and the synchronously demodulated signals I and Q may be considered to be two

complex signals each having real and imaginary parts corresponding to the in-phase and quadrature phase signals respectively. The complex multiplier 628 combines these two complex signals to develop a phase corrected complex signal having real and imaginary parts, I' and Q' respectively.

FIGURE 8 is a block diagram showing the complex multiplier 628. The digital signal Q from ADC 24 is applied to one input port of a conventional digital multiplier 310. The digital signal C_Q from ROM 32 is applied to the other input port of multiplier 310. Multiplier 810 forms the product of the signals Q and C_Q and applies this product to one input port of a subtracter 814. Similarly, the product of the signals I and C_I is formed by a multiplier 812 which applies the result to another input port of the subtracter 814. Subtracter 814 subtracts the product of the signals Q and C_Q from the product of I and C_I to develop the corrected in-phase signal I'.

Additional multipliers 816 and 818 form the products of I and C_Q and of Q and C_I respectively. The output signals of the multipliers 816 and 818 are applied to an adder 820 which sums the signals to develop the corrected quadrature signal Q'.

Using the equations 1, 2, 11, and 12, the signals I' and Q' provided by the complex multiplier 28 may be described by the equations:

$$I' = (i \cos\theta - q \sin\theta)\cos\theta - (i \sin\theta + q \cos\theta)(-\sin\theta) \quad (13)$$

and

$$Q' = (i \sin\theta + q \cos\theta)\cos\theta + (i \cos\theta - q \sin\theta)(-\sin\theta) \quad (14)$$

Expanding the equations (13) and (14) yields:

$$I' = i \cos\theta \cos\theta - q \sin\theta \cos\theta + i \sin\theta \sin\theta + q \cos\theta \sin\theta \quad (15)$$

$$I' = i (\cos^2\theta + \sin^2\theta) \quad (16)$$

$$I' = i \tag{17}$$

$$Q' = i \sin\theta \cos\theta + q \cos\theta \cos\theta - i \cos\theta \sin\theta + q \sin\theta \sin\theta \tag{18}$$

$$Q' = q (\cos^2\theta + \sin^2\theta) \tag{19}$$

$$Q' = q \tag{20}$$

Consequently, the direct signal components of the signals I' and Q' produced by the complex multiplier 628 are substantially free of any demodulation phase error distortion components.

CLAIMS:

1. A circuit for reducing demodulation phase error in a system for processing radio frequency television signals comprising an input terminal for applying a radio frequency television signal having a direct signal component including a direct carrier signal and a delayed direct signal component including a delayed direct carrier signal, wherein said radio frequency television signal includes a carrier signal which is a vector sum of said direct carrier signal and said delayed direct carrier signal;

means coupled to said input terminal for extracting said carrier signal from said radio frequency television signal;

means coupled to said carrier signal extracting means and including phase locked loop circuitry for generating an oscillatory signal having a frequency and phase determined by said extracted carrier signal, said phase locked loop circuitry including phase comparator means responsive to said extracted carrier signal and to said oscillatory signal for generating a phase difference signal representing the difference in phase between said oscillatory and extracted carrier signals;

detection means coupled to said input terminal and responsive to said radio frequency television signal and to said oscillatory signal for generating first and second baseband signals each having direct and delayed direct signal components, wherein the direct signal components of said first and second baseband signals may include reciprocal crosstalk distortion components, said baseband signals representing amplitude modulated information carried by said radio frequency television signal;

means coupled to said detection means and responsive to at least one of said baseband signals for generating a phase control signal proportional to the difference in phase between said direct carrier

signal and the vector sum of said direct carrier signal and said delayed direct carrier signal; and

a phase correction circuit responsive to said phase control signal for modifying one of said phase difference signal and said first baseband signal to generate a modified first baseband signal having substantially reduced crosstalk distortion components.

2. A circuit as claimed in claim 1 wherein said phase correction circuit includes an adder and a voltage controlled oscillator and said phase control signal tends to change the phase of said oscillatory signal in a sense to reduce the magnitude of said phase control signal.

3. A circuit as claimed in claim 1 wherein said phase correction circuit includes means for generating a phase correction signal and means for combining said phase correction signal and said first baseband signal.

4. A circuit as claimed in claims 1, 2, or 3 wherein:

said radio frequency television signals include a synchronizing signal component having periodic transitions; and

said phase control signal generating means includes means responsive to said first and second baseband signals for generating a signal proportional to the ratio of the difference between the values of said second baseband signal at times immediately before and immediately after one of said periodic transitions and the difference between the values of said first baseband signal at times immediately before and immediately after one of said periodic transitions.

5. A circuit as claimed in claim 3 wherein:

said phase correction signal generating means includes means responsive to said phase control signal for generating said phase correction signal being proportional to the cosine of the difference in phase between said direct carrier signal and the vector sum of said direct and delayed direct carrier signals; and

said combining means includes means for multiplying said first baseband signal by said phase correction signal.

6. A circuit as claimed in claim 3 wherein:

said phase control signal is proportional to the tangent of the difference in phase between said direct carrier signal and the vector sum of said direct and delayed direct carrier signals;

said phase correction signal generating means includes means responsive to said phase difference signal for generating said first and second phase correction signals being proportional, respectively, to the cosine and sine of the phase difference represented by said phase difference signal and

said combining means includes a complex multiplier having first and second real and imaginary input ports and real and imaginary output ports, said first real and imaginary input ports being coupled to receive said first and second baseband signals respectively, said second real and imaginary input ports being coupled to receive said first and second phase correction signals respectively, and said real and imaginary output ports providing respectively, said modified first and second baseband signals having substantially reduced crosstalk distortion components.



7. A circuit as claimed in claim 1 wherein the magnitude of said phase control signal generated by said generating means is proportional to a phase angle by which said oscillatory signal differs from being quadrature phase related to said direct carrier signal.

8. A circuit as claimed in claim 1 or 7 wherein:

said radio frequency television signal includes a vertical field synchronizing signal component; and

said phase control signal generating means is responsive to components of the baseband signal provided by said detection means corresponding to said vertical field synchronizing signal component for generating said phase control signal.

9. A circuit as claimed in claim 8 wherein:

said vertical field synchronizing signal component includes periodic transitions; and

said phase control signal generating means includes:

sample and hold means coupled to said second synchronous detection means for generating first and second samples corresponding to the values of said second baseband signal at a time immediately prior to one of said periodic transitions and at a time immediately after one of said periodic transitions respectively; and

sample subtraction means, coupled to said sample and hold means, for generating a signal proportional to the difference between said first and second samples.

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10. A circuit as claimed in Claim 1 wherein said phase locked loop comprises:

a variable oscillator responsive to a frequency control signal for generating said oscillatory signal;

phase comparison means coupled to said variable oscillator and to said means for extracting said carrier signal, for generating a phase difference signal proportional to the difference in phase between said oscillatory signal and said extracted carrier signal; and

means coupled to said phase comparison means for combining said phase difference signal and said phase control signal to develop the frequency control signal for said variable oscillator.

11. A phase error reduction circuit substantially as hereinbefore described with reference to Figure 1 of the accompanying drawings alone or together with Figure 3 and/or one of Figures 2 and 5.

12. A phase error reduction circuit substantially as hereinbefore described with reference to Figure 6 of the accompanying drawings alone or together with Figure 7 and/or Figure 8.