

Description

The present invention concerns motion estimation, particularly, though not exclusively, in the context of video coders employing inter-frame differential coding.

Figure 1 shows a known form of video coder. Video signals (commonly in digital form) are received at an input 1. A subtractor 2 forms the difference between the input and a predicted signal from a predictor 3 which is then further coded in box 4. The coding performed here is not material to the present invention, but may include thresholding (to suppress transmission of zero or minor differences) quantisation or transform coding for example. The input to the predictor is the sum, formed in an adder 5 of the prediction and the coded difference signal decoded in a local decoder 6 (so that loss of information in the coding and decoding process is included in the predictor loop).

The differential coding is essentially inter-frame, and the predictor 3 could simply consist of a one-frame delay; as shown however a motion estimator 7 is also included. This compares the frame of the picture being coded with the previous frame being supplied to the predictor. For each block of the current frame (into which the picture is regarded as divided) it identifies that region of the previous frame which the block most closely resembles. The vector difference in position between the identified region and the block in question is termed a motion vector (since it usually represents motion of an object within the scene depicted by the television picture) and is applied to the predictor to shift the identified region of the previous frame into the position of the relevant block in the current frame, thereby making the predictor output a better prediction. This results in the differences formed by the subtractor 2 being, on average, smaller and permits the coder 4 to encode the picture using a lower bit rate than would otherwise be the case.

The motion estimator must typically compare each block with the corresponding block of the previous frame and regions positionally shifted from that block position; this involves a considerable amount of processing and often necessitates many accesses to stored versions of both frames.

According to the present invention a motion detector for video signals comprises:

means for the reception and temporary storage of video signals representing one frame of a picture and another frame of a picture in which each frame is formed from a plurality of lines and the one frame is constituted by a plurality of non-overlapping rows of blocks, each of the rows being constituted by a plurality of non-overlapping blocks of picture elements formed from respective portions of a respective set of frame lines;

arithmetic means arranged to compare each of the blocks of the one frame with a corresponding region of the other frame and with a plurality of positionally shifted regions of the other frame which represent a desired two-dimensional search extent;

and first means responsive to the results of the comparisons to produce vector information indicating a positional shift, if any, of the position of a region of the other frame to the position of a block in the one frame which meets a criterion of similarity, the set of vector information so produced constituting the estimation of the motion between the frames;

CHARACTERISED IN THAT the motion detector includes:

(i) delay means arranged:

(a) to make available, in turn, regions of picture elements in a predetermined sequence of regions of picture elements, each region corresponding to a region of the other frame of the same size as the block of the one frame, where successive regions within the sequence of regions correspond to regions progressively shifted horizontally in a direction along the lines of the other frame, all the picture elements of a region being made available simultaneously; and

(b) to repeat step (a) for successive sequences of regions corresponding to regions progressively shifted perpendicular to the direction along the lines of the other frame to an extent corresponding to the desired search extent (SI), vertically,

(ii) delay and storage means arranged:

(c) to make available, in turn, blocks of picture elements in a predetermined sequence from a row of blocks, all the picture elements of a block being made available simultaneously and for a period corresponding to the desired search extent, horizontally, in the line direction of the picture; and

(d) to repeat the predetermined sequence for as many times as there are successive sequences of regions shifted in the vertical direction at step (b);

and in which:

(iii) the arithmetic means are arranged to form the sum of the moduli or other monotonically increasing even function of the differences between the picture elements made available for a block and the picture elements made available for a region; and

(iv) that the first means are arranged in operation to ascertain for each block the vector information corresponding to the region whose sum meets the said criterion.

One embodiment of the invention will now be described, with reference to the accompanying drawings, in which:

- 5 Figure 2 is a diagram of a television picture illustrating a co-ordinate system and search area;
- Figure 3 is a block diagram of part (P1 of Fig 5) of a motion estimator according to the invention;
- Figure 4 is a diagram of the search area S_N of Figure 2;
- Figure 5 is a block diagram of a complete motion estimator; and
- Figure 6 is a block diagram of the sorter CSO of Figure 5.

10 The motion estimator to be described regards a "current" frame of a television picture which is being coded as being divided into 8×8 blocks - that is, eight picture elements (pixels) horizontally by eight lines vertically. Although the principles are equally applicable to interlaced systems, for simplicity of description a non-interlaced picture is assumed. It is designed to generate for each block a motion vector which indicates the position of the 8×8 region, lying within a defined search area of the (or a) previous frame of the picture, 15 which is most similar to the block in question. Figure 2 illustrates a field with an 8×8 block N (shaded) and a typical associated 23×23 search area indicated by a rectangle S_N . If the pixels horizontally and lines vertically are identified by coordinates x, y , with an origin at the top left - hand corner, then the search area for a block whose upper left hand corner pixel has coordinates x_N, y_N is the area extending horizontally from (x_N-8) to (x_N+14) and vertically from (y_N-8) to (y_N+14) .

20 In order to obtain the motion vector it is necessary to conduct a search in which the block is compared with each of the 256 possible 8×8 regions of the previous frame lying within the search area - i.e. those whose upper left pixel has coordinates x_N+u, y_N+v where u and v are in the range -8 to $+7$. The motion vector is the values of u, v for which the comparison indicates the greatest similarity. The test for similarity can be any conventionally used - e.g. the sum of the absolute values of the differences between each of the 25 pixels in the "current" block and the relevant region of the previous frame.

Thus, if the current frame and previous frame pixel values are $a(i,j)$ and $b(i,j)$ respectively then the sum of differences is

$$30 \quad E_{x,y}(v,u) = \sum_{i=0}^7 \sum_{j=0}^7 |a(x+i,y+j) - b(x+u+i,y+v+j)|$$

Commonly the search is carried out for each block of the current picture in turn. However because the search area associated with a block overlaps the search areas of a number (24 in the case of blocks not 40 close to the edge of the picture) of other blocks this (see the search area shown dotted in Fig 2 for block $N+1$) often requires multiple accesses to the previous frame information stored in a frame store, which are time consuming and may interfere with other coder functions.

The motion estimator to be described is assumed to be provided, in real time, with

- (a) a digital video signal corresponding to the "current" frame of a picture to be coded.
- 45 (b) a digital video signal corresponding to the previous frame of the picture.

The signals consist of a sequence of 8-bit digital words representing the luminance of successive picture elements of the first line, (though chrominance signals could be similarly processed if desired) followed by similar sequences for the second, third and subsequent lines.

Unlike the block-by-block approach mentioned earlier, the apparatus is arranged so that all comparisons 50 involving a particular line of the picture are carried out consecutively. As will be seen, this requires a storage capacity of only a total of sixteen line delays for the previous frame.

Figure 3 shows part of the apparatus, the operation of which will be described with reference to figure 4. The "position" in the picture of an 8×8 block or region will be considered as defined by the x, y coordinates of its upper left pixel. Thus the block N in figure 4 is at position x, y . The apparatus of figure 2 serves to compare the 8×8 block N at x, y with the 8×8 regions at $(x+u), (y+v)$ where u ranges from -8 to $+7$ and v from 0 to $+7$ - ie the regions whose positions are within the lower broken line area S_1 in figure 4. In figure 3, the previous frame is received (following a 9-pixel delay XD, the purpose of which will be apparent later) at an input P1 (all signal paths in the figure are 8-bit unless otherwise indicated by a diagonal

bar and adjacent number). This supplies a tapped delay line consisting of eight one-line delay units LD1...LD8, so that the signal for any line of the picture is available at the output of LD8 and that for the seven later lines is available at the outputs of LD7, LD6 etc. The current picture signal is supplied via input CI to a delay line with storage having eight sections DS1... DS8. Each section consists of two delay units of one line period duration; one half of each section forms part of an eight line period delay line and the other half forms a recirculating store. When the last line of a group of eight lines has entered the delay line, the roles of the two halves of each section are reversed so that while the next eight lines are entering the delay line the eight already entered are repeatedly available at the outputs of the recirculating sections.

Thus, referring to figure 4, (and ignoring the 9-pixel offset and assuming that line y is the first of a block) at the conclusion of line y+7, lines y, y+1...y+7 of the current frame are about to be output from DS8,DS7...DS1, whilst lines y,y+1,...y+7 of the previous frame are about to be output from LD8,LD7,...LD1.

The outputs of LD8 and DS8 feed respective (8-bit wide) 8-stage serial in parallel out (SIPO) registers PS8, CS8 clocked at pixel rate. The eight outputs of the latter are latched in a latch CL8 every 16 pixels synchronously with the horizontal block structure of the frame. Thus, once pixel x+7 of line y has entered the SIPO CS8, pixels x to (x+7) are available at the output of latch CL8 on the next clock pulse. At this time, pixels x-8 to x-1 are available at the outputs of the SIPO PS8 (due to the 9-pixel delay XD).

The outputs of the PS8 and CL8 are supplied to subtractors M81 - M88; the sum of the moduli of the differences is formed in a summation unit A8. Thus in the circumstances described in the preceding paragraph, the summer output represents the "sum of differences" between the first line of the current picture block N, and the first line of the region indicated by chain-dot lines in figure 4.

The arrangement consisting of PS8,CS8, CL8, M81-88 and A8 is provided for the outputs of LD8 and DS8; seven further such arrangements are provided (though, for clarity, not shown in Figure 3) for the outputs of LD7/DS7, LD6/DS6...LD1/DS1. They function in an identical manner, except that, being connected to earlier taps of the delay lines, they operate on the seven later lines of the picture. The outputs of the summers A8...A1 are added in an adder AA which produces the "sum of differences" between the current block N and the 8 x 8 region of the previous frame indicated by the chain-dot lines in figure 4. This is the value $E_{xy}(-8,0)$ according to the definition given above.

One pixel clock cycle later, the SIPO's PS8...1 now contain pixels x-7 to x instead of x-8 to x-1. The output of the latch CL8 is unchanged, thus the comparison now is between the current block and block (x-7),0 and adder AA produces an output $E_{xy}(-7,0)$. This process continues for 16 clock cycles, at the conclusion of which the adder AA has produced 16 results $E(-8,0), E(-7,0) \dots E(7,0)$. The first pass of the search area S1 in figure 4 is now complete.

The pixels of the next-but-one block N+2 of the current frame (i.e. those with horizontal co-ordinates (x+16) to (x+23)) are now present in the SIPO's CS8...; these are clocked into the latches CL8..., at which point pixels (x+8) to (x+15) are available at PS8, corresponding to search position for the new block, and the first pass now proceeds for block N+2, and successive alternate blocks until the end of the line.

At the conclusion of a line period, line y+1 of the previous frame is appearing at the output of LD8; however, by the recirculating action of DS8, line y of the current frame appears again at the output of DS8, and the second pass for block N takes place, it being this time compared with the chain-dot region of figure 4, shifted down by one line. It will be seen, that after eight line periods, a comparison will have been made between block N and all the regions defined by the area S1 (and similarly for all the even numbered blocks in a row).

When this has occurred, the delay and store stages DS8... are clocked and lines y+8 to y+15 of the current frame now become available at their outputs. Line y+8 of the previous frame is just about to appear at the output of delay LD8, and the arrangement of figure 2 is ready to accommodate the next row of blocks.

It will be observed however that the search process for block N is incomplete; the search area S2 (fig 4) has not been dealt with. Also the odd numbered blocks have received no attention. Referring now to figure 5, the arrangements of figure 3 (apart from delay XD) now appear as processor P1. A second processor P2 handles the upper search area S2; it is identical in all respects to P1 but is supplied with the previous frame signal via an 8 line delay (shown explicitly as ELD though in practice the signal could be tapped from LD8 of the processor P1), giving the desired result of defining a search area S2 which is 8 lines earlier than S1. It is noted in passing that were the search S_N area smaller (i.e. 17x17 or less rather than 23x23) one processor (suitably timed) would suffice.

The even-numbered blocks are handled by a further pair of processors P3, P4 which are identical to P1 and P2 and receive the same signal inputs as P1 and P2 respectively. However their latches CL8 are clocked (every 16 pixels as before) with pulses which are 8 pixels out of phase with those supplied to the processors P1 and P2. Although the figure shows identical processors (which may be a convenient modular

hardware implementation), certain of the elements within the processors may if desired be common to two or more of the processors, (e.g. the lines DS8....DS1).

We will now consider the further processing of the "sum of difference" values E. It is necessary to find for each block of the current frame the position (u,v) giving the lowest E. Since the E values for a given block appear over an 8-line period, interspersed with those for other blocks in the same horizontal row, a degree of sorting is also necessary. Two compare and sort units CSE,CSO are shown in Figure 5 for the even and odd blocks respectively, with outputs VOE,VOO for the output motion vectors.

Unit CSO is shown in Figure 6 and is identical to CSE (except for the timing of the inputs, of course).

The outputs of the processors P1, P2 are applied to the unit. A vector generator VG synchronised by pixel clock (and line and field synchronising pulses) produces the value of the vector component u (4 bits) and the lower 3 bits of component v associated with the E value being received from the processor P1.

The two E values received simultaneously from P1 and P2 always relate to the same block of the current picture, so that these can readily be compared by a comparator C1. The comparator output controls a data selector SEL1 to output the smaller of the received values; the comparator output also is appended to the vector generator output to form the most insignificant bit of v.

The description so far has conveniently ignored problems that may arise where the block under consideration is within 8 lines or pixels of the edge of the picture - i.e. certain of the regions defined by x, y, u, v overlap the line and field blanking periods. This is readily overcome by disregarding such regions. A border detector BG serves to override the action of the selector SEL1 by:

- (a) at the top of the picture, where results for such regions are produced by processor P2, forcing the selector to pass the output from processor P1;
- (b) at the bottom of the picture, where results for such regions are produced by the processor P1, forcing the selector to pass the output from processor P2;
- (c) at the sides of the picture, where both processors produce such results, setting the output of the selector to its maximum value, thereby obliging the subsequent stages of the sorter to select a different value.

A first-in-first-out store FIFO1 stores the lowest E value for each odd block of a row. All the store locations are set to their maximum value at the commencement of a row. Each processor pass generates, for any block N, sixteen E values in succession. When the first of these is received from the selector SEL 1 a comparator C2 compares it with the previous value recorded in the store for the relevant block and controls the selector SEL2 to enter into a latch whichever is the lower of the two values. A second selector SEL3 then switches to feed the latch output to the comparator C2 (and selector SEL1) and the comparator compares each of the remaining fifteen values with the value held in the latch L1; again, the selector SEL1 passes the lower value of the pair to form the new latched value. After the sixteen values have been compared, the content of the latch is loaded back into the store. In the same inner, selectors SEL4, SEL5 and latch L2 select for entry into a second store FIFO2 either the vector previously stored therein or the incoming vector (from VG and C1).

After all eight passes of the current row have taken place, the store FIFO1 contains the lowest "sum of differences" value E for each block of the row, and the store FIFO2 contains the corresponding vectors u,v. These can then be read out and output to the output VOO prior to the processing of the next row.

In some circumstances it may be easier to generate in the vector generator VG vectors which are coded differently from those required at the output, in which case a vector mapping unit VM - which may be a simple look-up table - can be included.

It has been assumed that the previous frame region to be identified is the one having the smallest difference from the current block in question. However it may be desired to give a bias to the zero vector - i.e. a non-zero vector is output only if a region u,v gives a sum of differences E(u,v) which is less by a predetermined amount than the value E (0,0) for the undisplaced region of the previous frame - e.g. is less than 75% of E(0,0). This can be achieved by a scaling unit ZVS which normally passes the values received from the processor P1 unchanged, but reduces the value to 75% of the input value when a signal VO from the vector generator VG indicates a position (0,0).

Claims

1. A motion detector for video signals comprising:
 - means (DS, CS, CL, LD, PS) for the reception and temporary storage of video signals representing one frame of a picture and another frame of a picture in which each frame is formed from a plurality of lines and the one frame is constituted by a plurality of non-overlapping rows of blocks, each of the rows being constituted by a plurality of non-overlapping blocks of picture elements formed from respective

hardware implementation), certain of the elements within the processors may if desired be common to two or more of the processors, (e.g. the lines DS8....DS1).

We will now consider the further processing of the "sum of difference" values E. It is necessary to find for each block of the current frame the position (u,v) giving the lowest E. Since the E values for a given block appear over an 8-line period, interspersed with those for other blocks in the same horizontal row, a degree of sorting is also necessary. Two compare and sort units CSE,CSO are shown in Figure 5 for the even and odd blocks respectively, with outputs VOE,VOO for the output motion vectors.

Unit CSO is shown in Figure 6 and is identical to CSE (except for the timing of the inputs, of course).

The outputs of the processors P1, P2 are applied to the unit. A vector generator VG synchronised by pixel clock (and line and field synchronising pulses) produces the value of the vector component u (4 bits) and the lower 3 bits of component v associated with the E value being received from the processor P1.

The two E values received simultaneously from P1 and P2 always relate to the same block of the current picture, so that these can readily be compared by a comparator C1. The comparator output controls a data selector SEL1 to output the smaller of the received values; the comparator output also is appended to the vector generator output to form the most insignificant bit of v.

The description so far has conveniently ignored problems that may arise where the block under consideration is within 8 lines or pixels of the edge of the picture - i.e. certain of the regions defined by x, y, u, v overlap the line and field blanking periods. This is readily overcome by disregarding such regions. A border detector BG serves to override the action of the selector SEL1 by:

- (a) at the top of the picture, where results for such regions are produced by processor P2, forcing the selector to pass the output from processor P1;
- (b) at the bottom of the picture, where results for such regions are produced by the processor P1, forcing the selector to pass the output from processor P2;
- (c) at the sides of the picture, where both processors produce such results, setting the output of the selector to its maximum value, thereby obliging the subsequent stages of the sorter to select a different value.

A first-in-first-out store FIFO1 stores the lowest E value for each odd block of a row. All the store locations are set to their maximum value at the commencement of a row. Each processor pass generates, for any block N, sixteen E values in succession. When the first of these is received from the selector SEL 1 a comparator C2 compares it with the previous value recorded in the store for the relevant block and controls the selector SEL2 to enter into a latch whichever is the lower of the two values. A second selector SEL3 then switches to feed the latch output to the comparator C2 (and selector SEL1) and the comparator compares each of the remaining fifteen values with the value held in the latch L1; again, the selector SEL1 passes the lower value of the pair to form the new latched value. After the sixteen values have been compared, the content of the latch is loaded back into the store. In the same inner, selectors SEL4, SEL5 and latch L2 select for entry into a second store FIF02 either the vector previously stored therein or the incoming vector (from VG and C1).

After all eight passes of the current row have taken place, the store FIF01 contains the lowest "sum of differences" value E for each block of the row, and the store FIF02 contains the corresponding vectors u,v. These can then be read out and output to the output VOO prior to the processing of the next row.

In some circumstances it may be easier to generate in the vector generator VG vectors which are coded differently from those required at the output, in which case a vector mapping unit VM - which may be a simple look-up table - can be included.

It has been assumed that the previous frame region to be identified is the one having the smallest difference from the current block in question. However it may be desired to give a bias to the zero vector - i.e. a non-zero vector is output only if a region u,v gives a sum of differences E(u,v) which is less by a predetermined amount than the value E (0,0) for the undisplaced region of the previous frame - e.g. is less than 75% of E(0,0). This can be achieved by a scaling unit ZVS which normally passes the values received from the processor P1 unchanged, but reduces the value to 75% of the input value when a signal VO from the vector generator VG indicates a position (0,0).

Claims

1. A motion detector for video signals comprising:
 - means (DS, CS, CL, LD, PS) for the reception and temporary storage of video signals representing one frame of a picture and another frame of a picture in which each frame is formed from a plurality of lines and the one frame is constituted by a plurality of non-overlapping rows of blocks, each of the rows being constituted by a plurality of non-overlapping blocks of picture elements formed from respective



portions of a respective set of frame lines;

arithmetic means (M, A & AA of P1 and P3) arranged to compare each of the blocks of the one frame with a corresponding region of the other frame and with a plurality of positionally shifted regions of the other frame which represent a desired two-dimensional search extent (SI);

and first means responsive to the results of the comparisons to produce vector information (VOO, VOE) indicating a positional shift, if any, of the position of a region of the other frame to the position of a block in the one frame which meets a criterion of similarity, the set of vector information so produced constituting the estimation of the motion between the frames;

CHARACTERISED IN THAT the motion detector includes:

(i) delay means (LD, PS) arranged:

(a) to make available, in turn, regions of picture elements in a predetermined sequence of regions of picture elements, each region corresponding to a region of the other frame of the same size as the block of the one frame, where successive regions within the sequence of regions correspond to regions progressively shifted horizontally in a direction along the lines of the other frame, all the picture elements of a region being made available simultaneously; and

(b) to repeat step (a) for successive sequences of regions corresponding to regions progressively shifted perpendicular to the direction along the lines of the other frame to an extent corresponding to the desired search extent (SI), vertically,

(ii) delay and storage means (DS, CS, CL) arranged:

(c) to make available, in turn, blocks of picture elements in a predetermined sequence from a row of blocks, all the picture elements of a block being made available simultaneously and for a period corresponding to the desired search extent (SI), horizontally, in the line direction of the picture; and

(d) to repeat the predetermined sequence for as many times as there are successive sequences of regions shifted in the vertical direction at step (b);

and in which:

(iii) the arithmetic means (M, A and AA) are arranged to form the sum of the moduli or other monotonically increasing even function of the differences between the picture elements made available for a block and the picture elements made available for a region; and

(iv) that the first means (CSO, CSE) are arranged in operation to ascertain for each block the vector information corresponding to the region whose sum meets the said criterion.

2. A detector according to Claim 1 in which the desired search extent (SI) horizontally in the line direction is greater than or equal to twice the extent of a block in that direction, the delay and storage means are arranged concurrently to form a plurality q (where q is an integer greater than one) of different sequences containing groups of picture elements corresponding to every q-th block in the line direction, and the arithmetic means comprise a plurality q of arrangements for forming the said sums for the respective sequences.

3. A detector according to either one of Claims 1 and 2 in which the delay and storage means is arranged concurrently to make available an additional sequence corresponding to regions (or blocks) shifted by the predetermined number of lines relative to the first mentioned sequence, that the detector includes additional arithmetic means (M, A & AA of P2 and P4) responsive to the additional sequence to compare each block of the said one frame with a further plurality of positionally shifted regions of the said other frame, which represent an extension (S2) of the said search extent, and that the means (CSO, CSE) for producing vector information are connected to receive the sums from both the first mentioned arithmetic means (in P1,P3) and the additional arithmetic means (in P2,P4).

4. A detector according to any one of the preceding claims in which the first means comprise means (C1, C2) for comparing values output by the arithmetic means in respect of a block with that one of the previous values for that block which meets the criterion, and includes means (FIFO1) for intermediate storage of partial results during comparisons of values for other blocks.

5. A detector according to Claim 4 in which the first means includes means (VG) for generating vector values corresponding to the regions represented by the values output by the arithmetic means, switching means (SEL4, L2, SEL5) to select the vector value corresponding to the latest region to meet the criterion, and means (FIFO2) for intermediate storage of the vector values corresponding to the said intermediately stored partial results.



6. A detector according to any one of the preceding claims in which the said criterion is met by a region for which a comparison value equal in the case of the unshifted region to a predetermined proportion of the said sum and equal in the case of the other regions to the said sum is less than the comparison value for all other regions compared with the block.

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Patentansprüche

1. Bewegungsdetektor für Videosignale, der aufweist:

10 eine Einrichtung (DS, CS, CL, LD, PS) zum Empfang und zum vorübergehenden Speichern von Videosignalen, die einen Rahmen eines Bildes und einen anderen Rahmen eines Bildes darstellen, wobei jeder Rahmen aus einer Vielzahl von Zeilen gebildet ist und der eine Rahmen aus einer Vielzahl von sich nicht überlappenden Reihen von Blöcken aufgebaut ist, wobei jede der Reihen aus einer Vielzahl von sich nicht überlappenden Blöcken von Bildelementen aufgebaut ist, die aus jeweiligen Abschnitten eines jeweiligen Satzes von Rahmenzeilen gebildet sind;

15 eine Arithmetik-Einrichtung (M, A & AA von P1 und P3), die angeordnet ist, um jeden der Blöcke des einen Rahmens mit einem entsprechenden Bereich des anderen Rahmens und mit einer Vielzahl von positionsmäßig verschobenen Bereichen des anderen Rahmens zu vergleichen, die ein gewünschtes zweidimensionales Suchgebiet (SI) darstellen;

20 und eine erste Einrichtung, die auf die Ergebnisse der Vergleiche anspricht, um eine Vektorinformation (VOO, VOE) zu erzeugen, die eine positionsmäßige Verschiebung, falls vorhanden, der Position eines Bereichs des anderen Rahmens zu der Position eines Blocks; in dem einen Rahmen anzeigt, die einem Kriterium einer Ähnlichkeit genügt, wobei der so erzeugte Satz von Vektorinformationen die Einschätzung der Bewegung zwischen den Rahmen darstellt;

dadurch gekennzeichnet, daß der Bewegungsdetektor aufweist:

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- (i) eine Verzögerungseinrichtung (LD, PS), die angeordnet ist:

30 (a) um ihrerseits Bereiche von Bildelementen in einer vorbestimmten Reihenfolge von Bereichen von Bildelementen verfügbar zu machen, wobei jeder Bereich einem Bereich des anderen Rahmens mit der gleichen Größe wie der Block des einen Rahmens entspricht, wobei aufeinanderfolgende Bereiche innerhalb der Sequenz von Bereichen Bereichen entsprechen, die fortschreitend horizontal in einer Richtung längs der Zeilen des anderen Rahmens verschoben sind, wobei alle die Bildelemente eines Bereichs gleichzeitig verfügbar gemacht werden; und

35 (b) um Schritt (a) für aufeinanderfolgende Sequenzen von Bereichen zu wiederholen, die Bereichen entsprechenden, die fortschreitend senkrecht zur Richtung entlang der Zeilen des anderen Rahmens vertikal verschoben sind, und zwar um ein Ausmaß, das dem gewünschten Suchgebiet (SI) entspricht,

- (ii) eine Verzögerungs- und Speichereinrichtung (DS, CS, CL), die angeordnet ist:

40 (c) um ihrerseits Blöcke von Bildelementen in einer vorbestimmten Sequenz von einer Reihe von Blöcken verfügbar zu machen, wobei alle die Bildelemente eines Blocks gleichzeitig und für eine Periode entsprechend dem gewünschten Suchgebiet (SI) verfügbar gemacht werden, und zwar horizontal in der Zeilenrichtung des Bildes; und

(d) um die vorbestimmte Sequenz so oft zu wiederholen, wie es aufeinanderfolgende Sequenzen von Bereichen gibt, die in der Vertikalrichtung in Schritt (b) verschoben sind;

und in dem:

45 (iii) die Arithmetikeinrichtung (M, A und AA) angeordnet ist, um die Summe der Moduli oder einer anderen monoton zunehmenden geraden Funktion der Differenzen zwischen den Bildelementen, die für einen Block verfügbar gemacht sind, und den Bildelementen, die für einen Bereich verfügbar gemacht sind, zu bilden; und

50 (iv) die erste Einrichtung (CSO, CSE) bei Betrieb angeordnet ist, um für jeden Block die Vektorinformation, die dem Bereich entspricht, dessen Summe das Kriterium erfüllt, zu gewährleisten.

2. Detektor nach Anspruch 1, in dem das gewünschte Suchgebiet (SI) horizontal in der Zeilenrichtung größer oder gleich zweimal dem Ausmaß eines Blocks in dieser Richtung ist, wobei die Verzögerungs- und Speichereinrichtungen gleichzeitig angeordnet sind, um eine Vielzahl q (wobei q eine ganze Zahl größer als eins ist) von verschiedenen Sequenzen zu bilden, die Gruppen von Bildelementen entsprechend jedem q-ten Block in der Zeilenrichtung enthalten, und wobei die Arithmetikeinrichtung eine Vielzahl q von Anordnungen zum Bilden der Summen für die jeweiligen Sequenzen aufweist.

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3. Detektor nach einem der Ansprüche 1 und 2, wobei die Verzögerungs- und Speichereinrichtung gleichzeitig angeordnet sind, um eine zusätzliche Sequenz entsprechend Bereichen (oder Blöcken) verfügbar zu machen, die um die vorbestimmte Anzahl von Zeilen relativ zur erstgenannten Sequenz verschoben sind, wobei der Detektor eine zusätzliche Arithmetikeinrichtung (M, A & AA von P2 und P4) aufweist, die auf die zusätzliche Sequenz anspricht, um jeden Block des einen Rahmens mit einer weiteren Vielzahl von positionsmäßig verschobenen Bereichen des anderen Rahmens zu vergleichen, was eine Ausdehnung (S2) des Suchgebiets darstellt, und wobei die Einrichtung (CSO, CSE) zum Erzeugen der Vektorinformation verbunden ist, um die Summen von sowohl der zuerst erwähnten Arithmetikeinrichtung (in P1, P3) und der zusätzlichen Arithmetikeinrichtung (in P2, P4) zu empfangen.
4. Detektor nach einem der vorhergehenden Ansprüche, wobei die erste Einrichtung eine Einrichtung (C1, C2) zum Vergleichen von Werten, die von der Arithmetikeinrichtung bezüglich eines Blocks ausgegeben worden sind, mit denen der vorhergehenden Werte für diesen Block, der das Kriterium erfüllt, aufweist, sowie eine Einrichtung (FIFO1) zum Zwischenspeichern von Teilergebnissen während Vergleichen von Werten für andere Blöcke aufweist.
5. Detektor nach Anspruch 4, wobei die erste Einrichtung eine Einrichtung (VG) zum Erzeugen von Vektorwerten entsprechenden den Bereichen, die durch die Werte dargestellt sind, die von der Arithmetikeinrichtung ausgegeben werden, eine Schalteinrichtung (SEL4, L2, SEL5), um den Vektorwert entsprechend dem letzten Bereich auszuwählen, um das Kriterium zu erfüllen, und eine Einrichtung (FIFO2) zum Zwischenspeichern der Vektorwerte entsprechend den zwischenzeitlich gespeicherten Teilergebnissen aufweist.
6. Detektor nach einem der vorhergehenden Ansprüche, bei dem das Kriterium von einem Bereich erfüllt wird, für den ein Vergleichswert, der in dem Fall des unverschobenen Bereichs gleich einem vorbestimmten Anteil der Summe ist und der in dem Fall der anderen Bereiche gleich dieser Summe ist, Kleiner als der Vergleichswert für alle anderen, mit dem Block verglichenen Bereiche ist.

Revendications

1. Détecteur de mouvement pour signaux vidéo, comprenant :

des moyens (DS, CS, CL, LD, PS) de réception et d'enregistrement temporaire de signaux vidéo représentant une trame d'une image, et une autre trame d'une image dans laquelle chaque trame est formée à partir d'une pluralité de lignes et la trame en question est constituée par une pluralité de rangées de blocs ne se chevauchant pas, chacune de ces rangées étant constituée par une pluralité de blocs ne se chevauchant pas d'éléments d'images formés à partir de portions respectives d'un jeu respectif de lignes de trame ;

des moyens arithmétiques (M, A et AA de P1 et P3) disposés de manière à comparer chacun des blocs de la trame en question avec une région correspondante de l'autre trame, et avec une pluralité de régions décalées de l'autre trame, qui représentent un domaine de recherche désirée à deux dimensions (SI) ;

un des premiers moyens coopérant avec les résultats des comparaisons, de manière à produire des informations vectorielles (VOO, VOE) indiquant le cas échéant un décalage de position entre la position d'une région de l'autre trame, et la position d'un bloc dans la trame qui remplit un critère de similitude, le jeu d'information vectoriel ainsi produit constituant l'estimation du mouvement entre les trames ; caractérisé en ce que le détecteur de mouvement inclut :

(i) des moyens de retardement (LD, PS) disposés :

(a) pour rendre disponibles, tour à tour des régions d'éléments d'images selon une séquence prédéterminée de régions d'éléments d'images, chaque région correspondant à une région de l'autre trame de même taille que le bloc de la première trame, des régions successives à l'intérieur de la séquence de région correspondant à des régions déplacées progressivement horizontalement dans une direction le long des lignes de l'autre trame, tous les éléments d'image d'une région étant rendus disponibles simultanément ; et

(b) pour répéter l'étape (a) pour des séquences successives de régions correspondant aux régions progressivement déplacées perpendiculairement à la direction le long des lignes de l'autre trame jusqu'à un domaine correspondant au domaine désire de recherche (SI), verticalement,

(ii) des moyens de retardement et d'enregistrement (DS, OS, CL) disposés



(c) pour rendre disponibles à tour de rôle des blocs d'éléments d'images selon une séquence prédéterminée à partir d'une rangée de blocs, tous les éléments d'image d'un bloc étant rendus disponibles simultanément et durant une période correspondant au domaine désiré de recherche (SI) horizontalement, dans la direction des lignes de l'image ; et

5 (d) pour répéter la séquence prédéterminée autant de fois qu'il y a de séquences successives de régions déplacées dans la direction verticale à l'étape (b) ;

et en ce que :

10 (iii) les moyens arithmétiques (M, A et AA) sont disposés de manière à former la somme des modules ou de tout autre fonction paire croissante monotone, des différences entre les éléments d'images rendus disponibles pour un bloc, et les éléments d'images rendus disponibles pour une région ; et

(iv) les premiers moyens (CSO, CSE) sont disposés en opération pour établir pour chaque bloc, les informations vectorielles correspondant à la région dont la somme remplit ledit critère.

15 2. Détecteur selon la revendication 1, dans lequel le domaine désiré de recherche (SI) horizontalement dans la direction des lignes, est plus grand ou égal au double du domaine d'un bloc dans cette direction, les moyens de retardement et d'enregistrement sont disposés simultanément de manière à former une pluralité q (où q est un entier plus grand que 1) de séquences différentes contenant des groupes d'éléments d'images correspondant à chaque q-ième bloc dans la direction des lignes, et les
20 moyens arithmétiques comprennent une pluralité q d'arrangements permettant la formation desdites sommes pour les séquences respectives.

3. Détecteur selon l'une des revendications 1 ou 2, dans lequel les moyens de retardement et d'enregistrement sont disposés simultanément afin de rendre disponible une séquence additionnelle correspondant aux régions (ou blocs) déplacées par le nombre prédéterminé des lignes relatives à la séquence
25 premièrement mentionnée, le détecteur inclut des moyens arithmétiques additionnels (M, A et AA de P2 et P4) coopérant avec la séquence additionnelle, afin de comparer chaque bloc de ladite première trame avec une autre pluralité de région déplacée de ladite autre trame qui représentent une extension (S2) dudit domaine de recherche, et les moyens (CSO, CSE) de production des informations vectorielles sont reliées de manière à recevoir les sommes provenant à la fois des moyens arithmétiques
30 premièrement mentionnés (dans P1, P3) et des moyens arithmétiques additionnels (dans P2, P4).

4. Détecteur selon l'une quelconque des revendications précédentes, dans lequel les premiers moyens comprennent des moyens (C1, C2) de comparaison des valeurs sorties par les moyens arithmétiques à
35 partir d'un bloc, avec celle des valeurs précédentes de ce bloc qui remplit le critère, et incluent des moyens (FIFO1) d'enregistrement intermédiaire des résultats partiels durant les comparaisons de valeur pour les autres blocs.

5. Détecteur selon la revendication 4, dans lequel les premiers moyens incluent des moyens (VG) générant des valeurs vectorielles correspondant aux régions représentées par les valeurs sorties par
40 les moyens arithmétiques, des moyens de commutation (SEL4, L2, SEL5) pour sélectionner la valeur vectorielle correspondant à la dernière région remplissant le critère, et des moyens (FIFO2) d'enregistrement intermédiaire des valeurs vectorielles correspondant auxdits résultats partiels enregistrés de manière intermédiaire.

45 6. Détecteur selon l'une quelconque des revendications précédentes, caractérisé en ce que ledit critère est rempli par une région pour laquelle une valeur de comparaison égale dans le cas de région non déplacée, à une proportion prédéterminée de ladite somme, et égale dans le cas des autres régions, à ladite somme, est inférieure à la valeur de comparaison pour toutes les autres régions par rapport au
50 bloc.

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