EC directly below the memory gate electrode MG. Hence, when charge is injected from the memory well MW into the charge storage layer EC, charge may be injected also into the charge storage layer EC1 in the sidewall spacer 102.
[0070] As illustrated in FIG. 4B, in which any corresponding part to that in FIG. 4A is denoted by an identical reference numeral, for example, when the memory cell 100 according to Comparative Example 1 is left at a high temperature, charge in the charge storage layer EC gradually diffuses into the charge storage layer EC1, which is disposed in the sidewall spacer 102 between the memory gate electrode MG and the first select gate electrode DG, as time elapses. Accordingly, in the memory cell 100 according to Comparative Example 1, charge may be stored not only in the charge storage layer EC but also in the charge storage layer EC1 directly above a region ER2 of the memory well MW between the memory gate electrode MG and the first select gate electrode DG, and also in the nitride sidewall layer 104.
[0071] As described above, in the memory cell 100 according to Comparative Example 1, charge is likely to be stored in the charge storage layer EC1 directly above the region ER2 of the memory well MW between the memory gate electrode MG and the first select gate electrode DG, and also in the nitride sidewall layer 104. When a large amount of charge is thus stored or once charge is stored in the charge storage layer EC1 and the nitride sidewall layer 104, the stored charge has a charge centroid close to the substrate due to the small thickness of the sidewall spacer 102 below the charge storage layer EC1. As a result, in the memory cell 100 according to Comparative Example 1, a resistance increases in the region ER2 of the memory well MW between the memory gate electrode MG and the first select gate electrode DG, resulting in reduction in a memory current in a reading

operation. Thus, it is difficult to improve reading performance and achieve high speed operation.

[0072] In the memory cell 2 according to the present invention, as illustrated in FIG. 5, in which any corresponding part to that in FIG. 1 is denoted by an identical reference numeral, the charge storage layer EC is provided only in the region ER1, in which the memory gate electrode MG faces the memory well MW. The nitride sidewall layer 32a in the sidewall spacer 28a is apart from the charge storage layer EC, and the nitride sidewall layer 32a is disposed farther from the memory well MW than the charge storage layer EC.

[0073] With this configuration, in the memory cell 2, charge is prevented from being injected into the nitride sidewall layer 32a when charge is injected into the charge storage layer EC. Even after a predetermined time after the charge injection into the charge storage layer EC, the charge does not migrate from the charge storage layer EC into the sidewall spacers 28a and 28b. Accordingly, the charge is maintained only in the charge storage layer EC in the region ER1 below the memory gate electrode MG.

[0074] As a result, in the memory cell 2, charge is prevented from being stored in a region directly above the region ER2 of the memory well MW between the memory gate electrode MG and the first select gate electrode DG. Even when charge is stored in the nitride sidewall layer 32a in the sidewall spacer 28a, the stored charge has a charge centroid far from the substrate. Accordingly, the resistance is maintained low in the region ER2 of the memory well MW between the memory gate electrode MG and the first select gate electrode DG (the second select gate electrode SG), and thereby reading performance is improved and high speed operation is achieved.

[0075] (5) Operations and effects

Claims

1. A memory cell comprising:

a memory well;

a drain region disposed on a memory well surface of the memory well and connected to a bit line;

a source region disposed on the memory well surface and connected to a source line;

a memory gate structure disposed between the drain region and the source region and including a lower memory gate insulating film, a charge storage layer, an upper memory gate insulating film, and a memory gate electrode stacked in this order over the memory well, the memory gate structure having a first sidewall and a second sidewall;

a first select gate structure disposed between the drain region and the memory gate structure and including a first select gate insulating film disposed on the memory well and including a first select gate electrode disposed on the first select gate insulating film;

a second select gate structure disposed between the source region and the memory gate structure and including a second select gate insulating film disposed on the memory well and including a second select gate electrode disposed on the second select gate insulating film;

a first sidewall spacer disposed between the memory gate structure and the first select gate structure and including a first insulating layer and a first sidewall layer disposed in the first insulating layer, the first sidewall layer being made of an insulating material different from an insulating material of the first insulating layer, the first sidewall layer being disposed along the first sidewall of the memory gate structure and at a predetermined distance from the first sidewall of the memory gate structure such that the first sidewall layer is apart from the charge storage layer; and

a second sidewall spacer disposed between the memory gate structure and the second select gate structure and

including a second insulating layer and a second sidewall layer disposed in the second insulating layer, the second sidewall layer being made of an insulating material different from an insulating material of the second insulating layer, the second sidewall layer being disposed along the second sidewall of the memory gate structure and at the predetermined distance from the second sidewall of the memory gate structure such that the second sidewall layer is apart from the charge storage layer,

wherein a distance between the memory well surface and a lower surface of each of the first and second sidewall layers is greater than a thickness of the lower memory gate insulating film,

the first sidewall layer is disposed in the first sidewall spacer to separate the memory gate electrode from the first select gate electrode,

the second sidewall layer is disposed in the second sidewall spacer to separate the memory gate electrode from the second select gate electrode,

a width of each of the first and second sidewall spacers is greater than or equal to 5 nm, and

a thickness of each of the first and second select gate insulating films is less than or equal to 3 nm.

2. The memory cell according to claim 1, wherein

the first sidewall layer includes a first wall portion and a first lower end portion, the first wall portion extending along the first sidewall of the memory gate structure, the first lower end portion being integrated with a lower end of the first wall portion and extending along the memory well surface toward the first select gate electrode, and

the second sidewall layer includes a second wall portion and a second lower end portion, the second wall portion extending along the second sidewall of the memory gate structure, the second lower end portion being integrated

with a lower end of the second wall portion and extending along the memory well surface toward the second select gate electrode.

3. The memory cell according to claim 1, wherein the distance between the memory well surface and the lower surface of each of the first and second sidewall layers is 10 nm or more.

4. The memory cell according to claim 1, wherein a height of each of the first select gate structure and the second select gate structure from the memory well is less than or equal to a height of the memory gate structure.

5. The memory cell according to claim 1, wherein each of the first and second sidewall layers is a nitride sidewall layer.

6. A non-volatile semiconductor memory device comprising a plurality of memory cells according to claim 1, the plurality of memory cells being disposed in a matrix of rows and columns and being connected by at least one bit line and at least one source line.

7. A memory cell comprising:

a memory well;

a drain region disposed on a memory well surface of the memory well and connected to a bit line;

a source region disposed on the memory well surface and connected to a source line;

a memory gate structure disposed between the drain region and the source region and including a lower memory gate insulating film, a charge storage layer, an upper memory gate insulating film, and a memory gate electrode stacked in this order over the memory well, the memory gate structure having a first sidewall and a second sidewall;

a first select gate structure disposed between the drain region and the memory gate structure and including a first select gate insulating film disposed on the memory well and including a first select gate electrode disposed on the first select gate insulating film;

a second select gate structure disposed between the source region and the memory gate structure and including a second select gate insulating film disposed on the memory well and including a second select gate electrode disposed on the second select gate insulating film;

a first sidewall spacer disposed between the memory gate structure and the first select gate structure and including a first insulating layer and a first sidewall layer disposed in the first insulating layer, the first sidewall layer being made of an insulating material different from an insulating material of the first insulating layer, the first sidewall layer being disposed along the first sidewall of the memory gate structure and at a predetermined distance from the first sidewall of the memory gate structure such that the first sidewall layer is apart from the charge storage layer; and

a second sidewall spacer disposed between the memory gate structure and the second select gate structure and including a second insulating layer and a second sidewall layer disposed in the second insulating layer, the second sidewall layer being made of an insulating material different from an insulating material of the second insulating layer, the second sidewall layer being disposed along the second sidewall of the memory gate structure and at the predetermined distance from the second sidewall of the memory gate structure such that the second sidewall layer is apart from the charge storage layer,

wherein a distance between the memory well surface and a lower surface of each of the first and second sidewall layers is greater than a thickness of the lower memory gate insulating film,

the first sidewall layer is disposed in the first sidewall spacer to separate the memory gate electrode from the first select gate electrode,

the second sidewall layer is disposed in the second sidewall spacer to separate the memory gate electrode from the second select gate electrode,

the first sidewall layer is in contact with a sidewall of the first select gate structure, and

the second sidewall layer is in contact with a sidewall of the second select gate structure.