

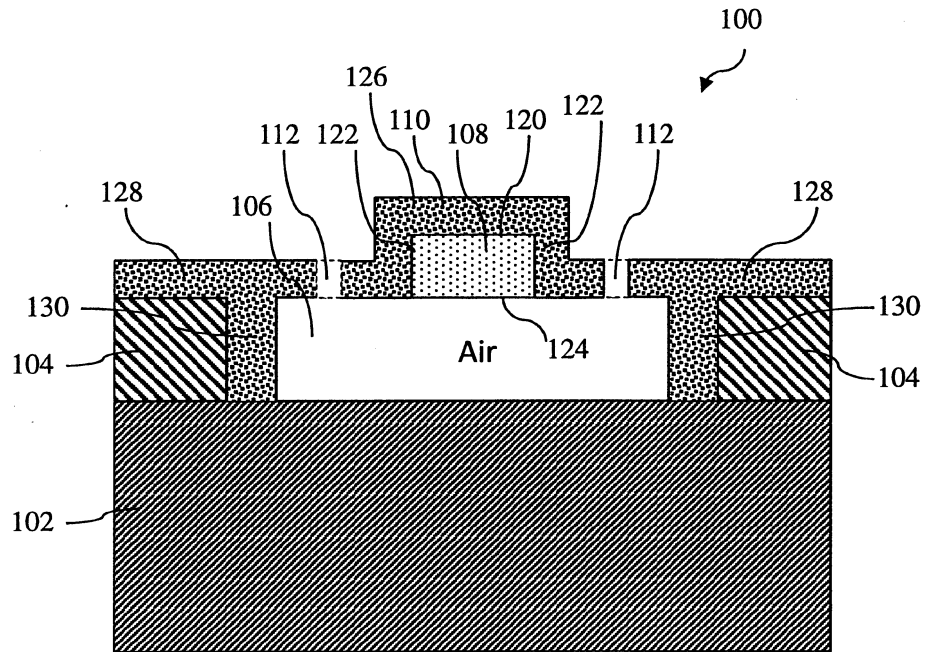


FIG. 1

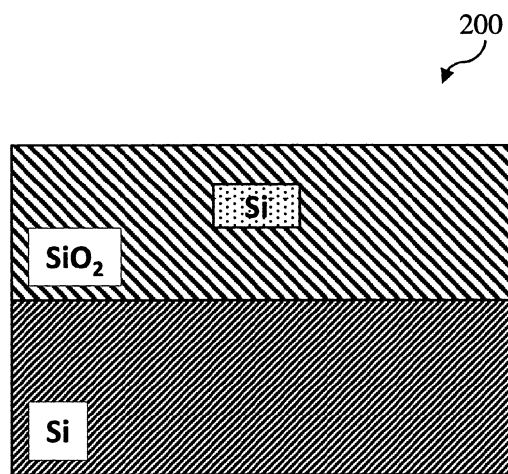


FIG. 2

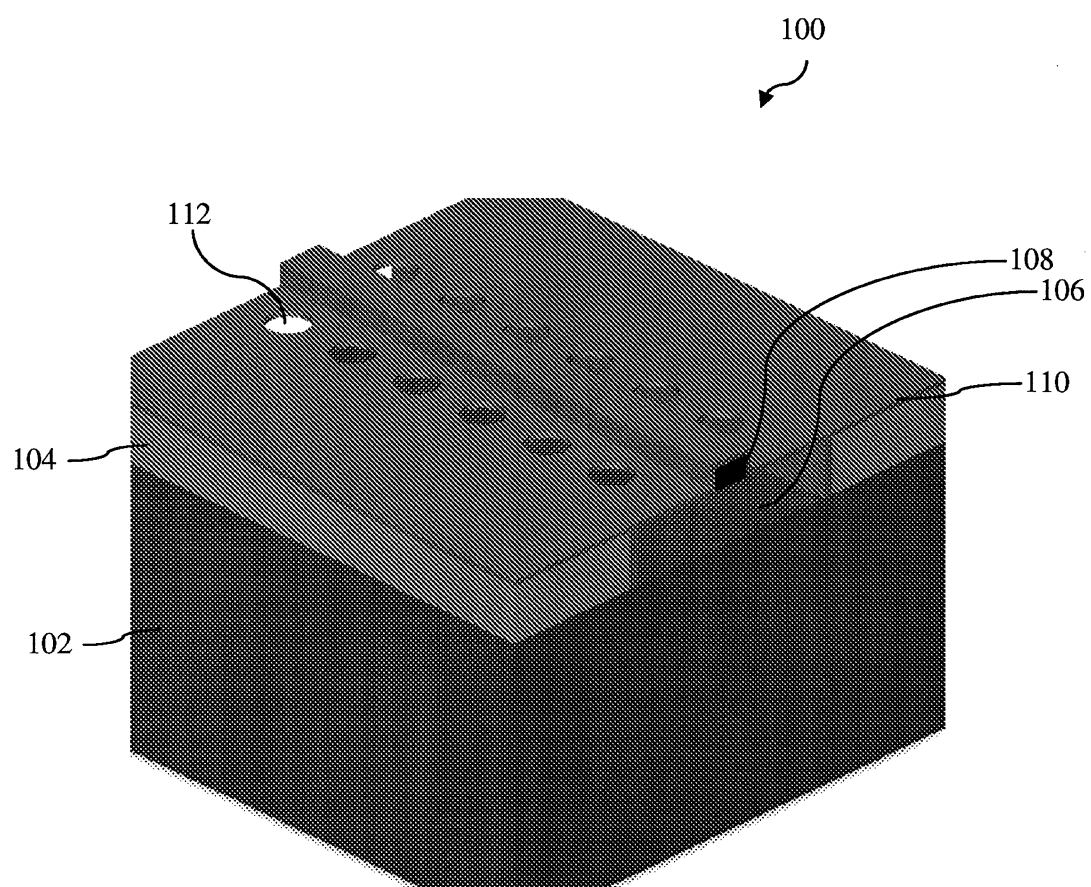


FIG. 3

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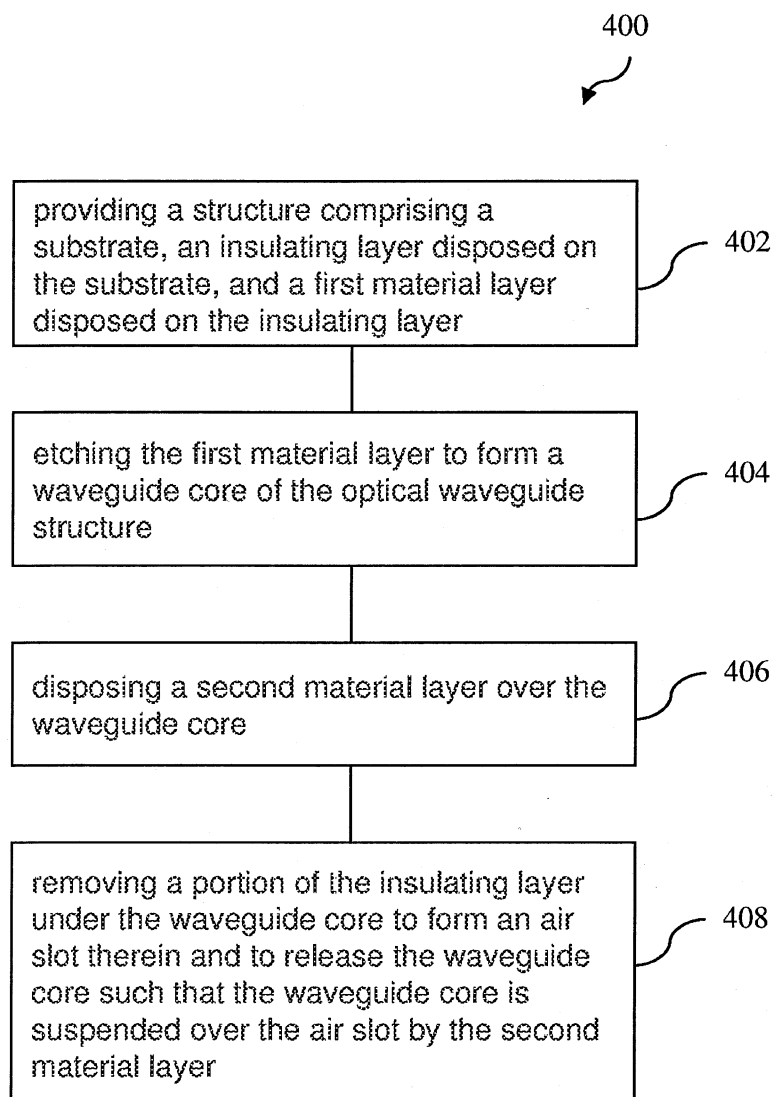
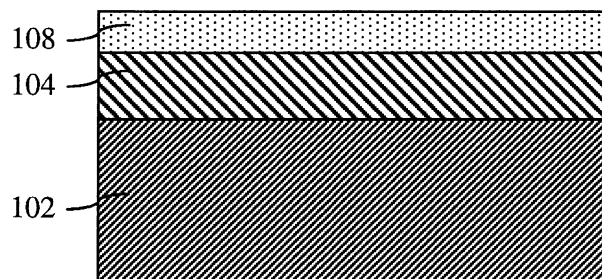
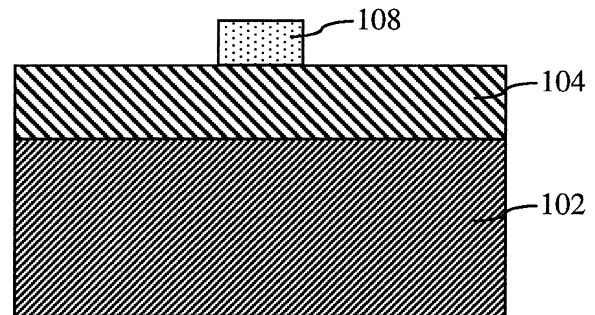


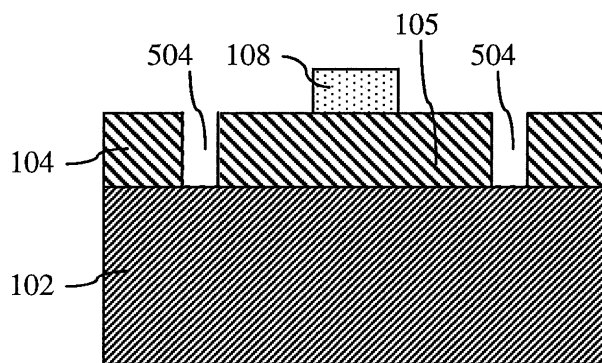
FIG. 4



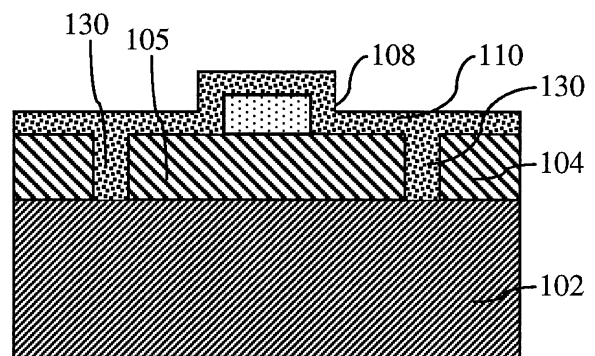
SOI wafer

FIG. 5A

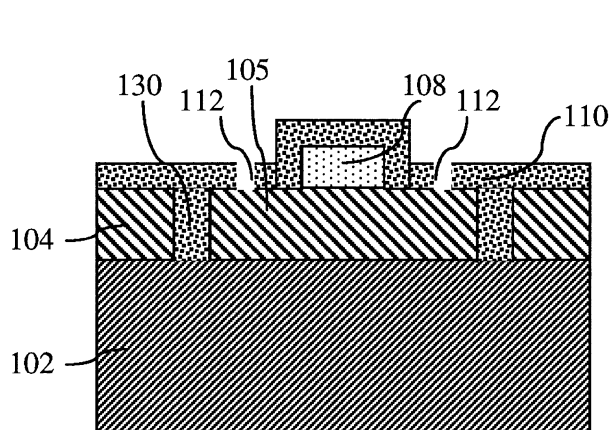
Waveguide etching and polish

FIG. 5B

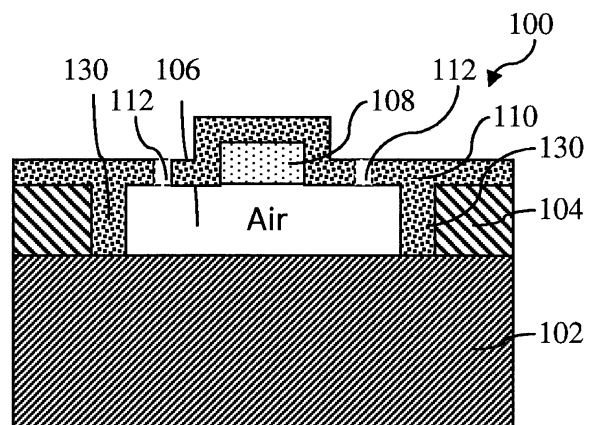
Oxide layer etching

FIG. 5C

Dielectric material deposition

FIG. 5D

Dielectric material layer etching

FIG. 5E

Release

FIG. 5F

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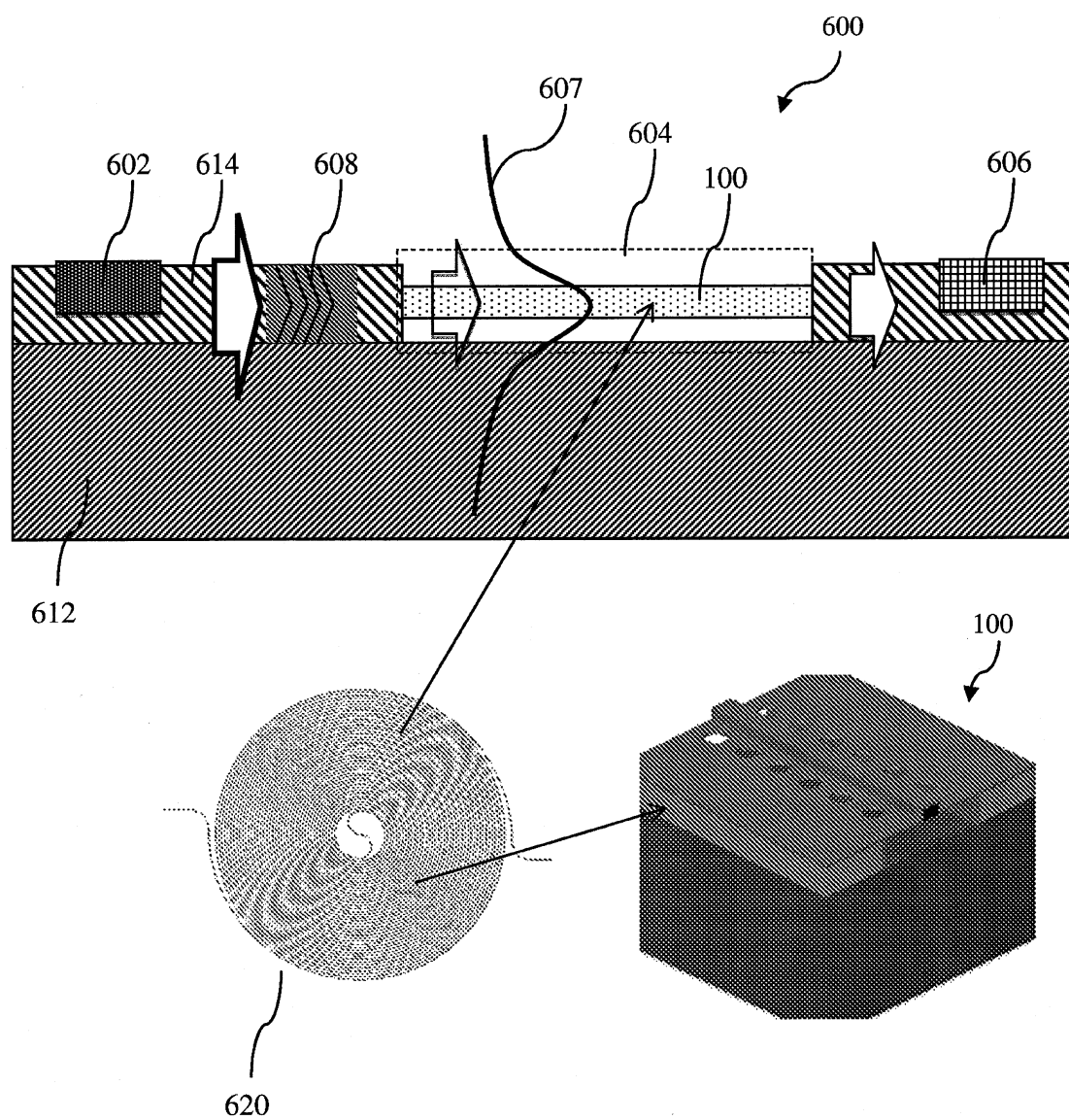


FIG. 6A

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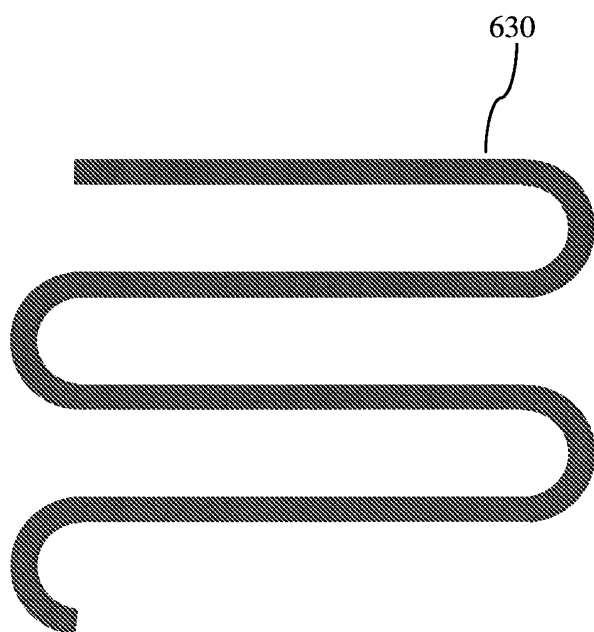


FIG. 6B

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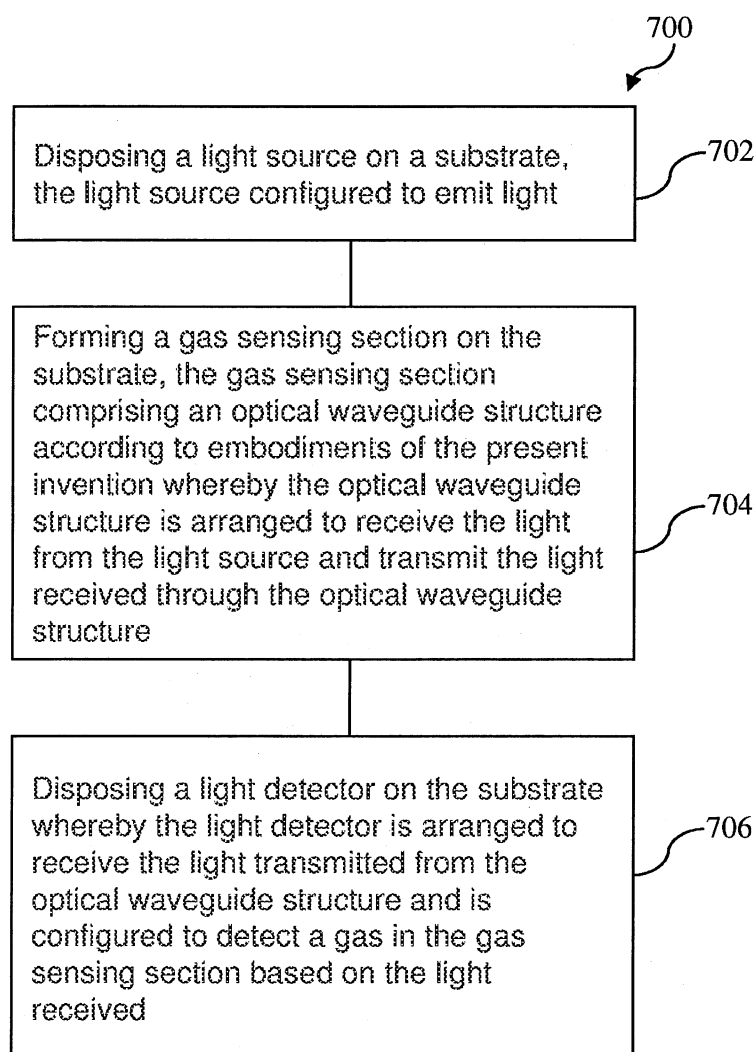


FIG. 7

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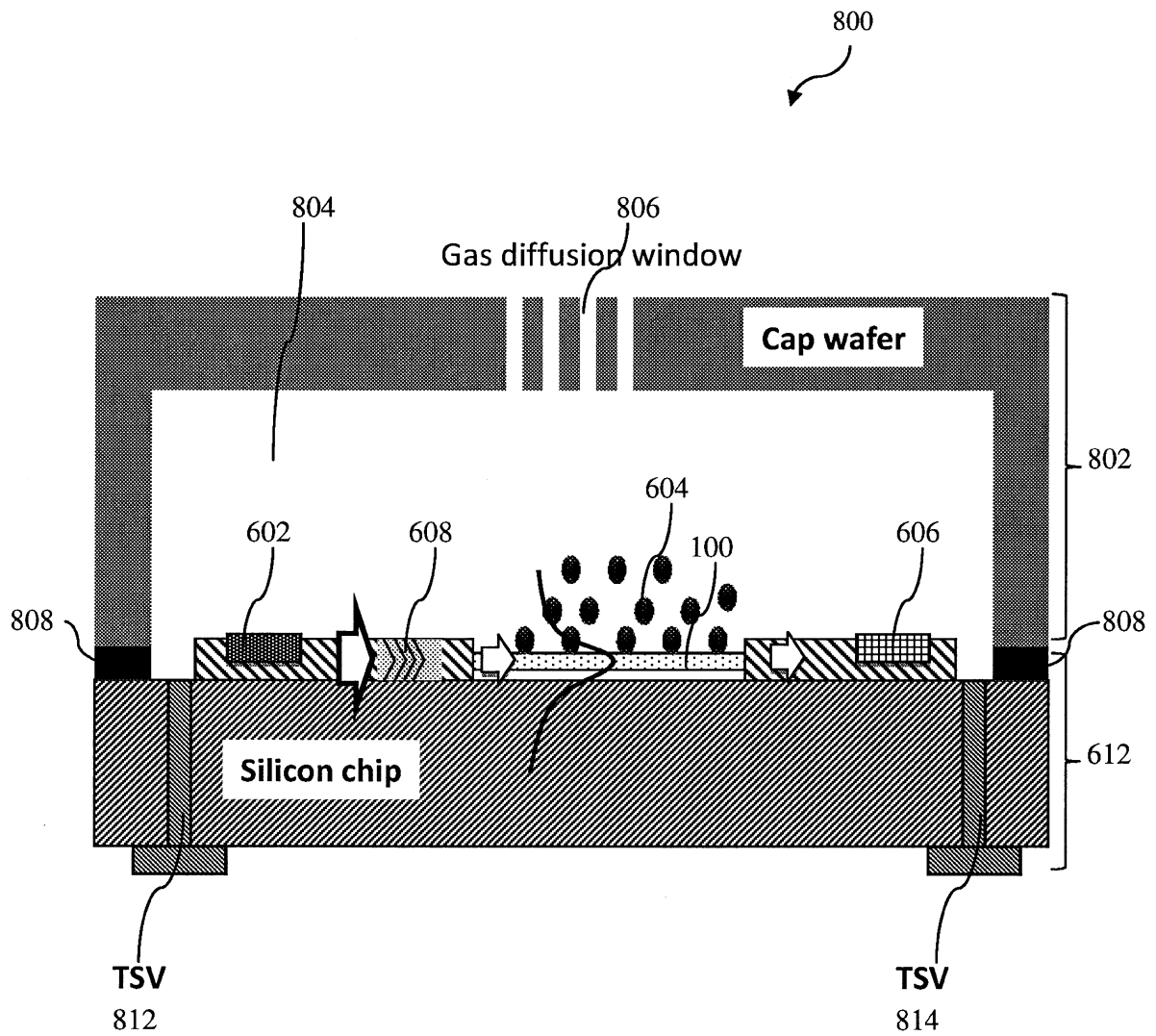


FIG. 8

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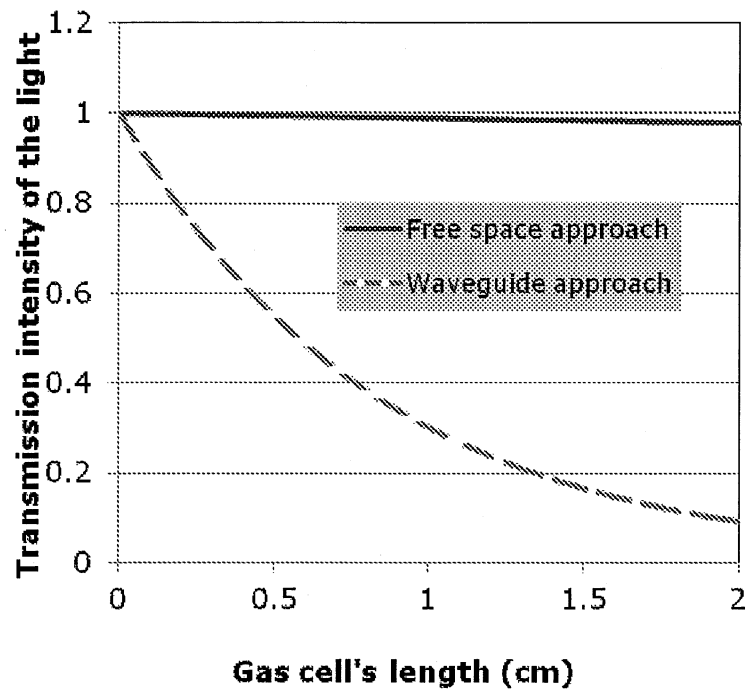


FIG. 9A

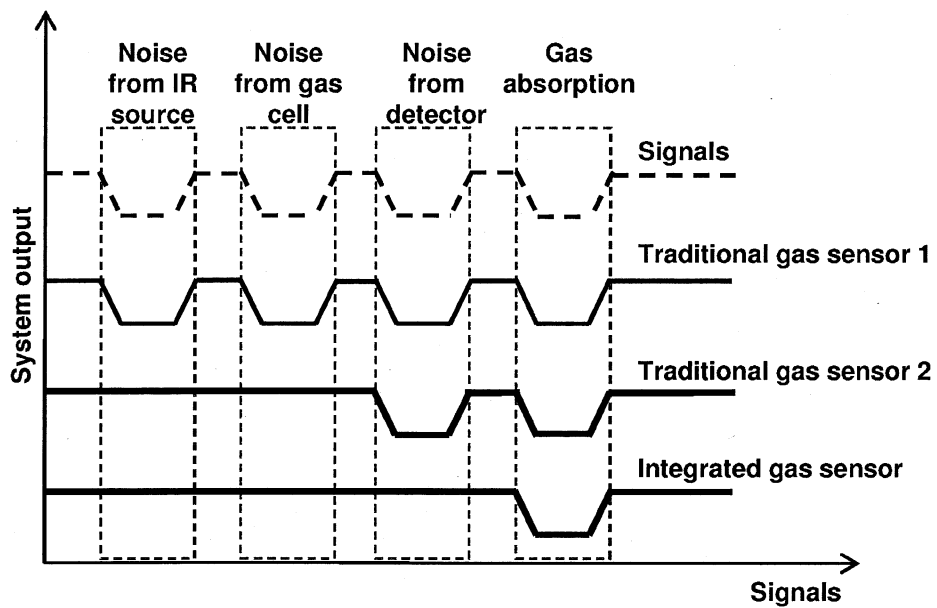


FIG. 9B