TELEVISION DISPLAY SYSTEM WITH REDUCED LINE-SCAN ARTIFACTS

This invention is divided from application no. 8311282 ("the parent application") which relates to a television display apparatus such as a television receiver arranged for reduced visibility of line-scan artifacts resulting from interlaced scanning of the scene being imaged.

Television receivers and monitors presently in use do not give the best pictures which are possible within the constraints of existing line-scanning standards. It is desirable to provide subjective improvements to produce a "high-fidelity" display. This problem is discussed in detail in the article "High Definition Television Studies On Compatible Basis With Present Standards" by Broder Wendland which appears in the book "Television Technology in the 80's" published by SMPTE.

A major problem with 525 line-per-frame, 30 frame per-second (525/30) scanning systems such as the NTSC system and in other systems such as 625/25 (PAL) are those artifacts which are derived from the line-scan process itself. The artifacts arise mainly due to the interlace process in the standards. Interlace is a technique for "shuttering" equivalent to the shuttering process in motion-picture technology. The purpose of interlace is to increase the flicker rate of the picture being displayed to reduce the perceptibility of the periodic appearance and disappearance (flicker) of the picture. A high flicker rate is desirable because it gives the appearance of a continuously-existing picture.

In a 525/30 system, 525 lines are scanned in 1/30 second, giving a 30 Hz sample rate. The interlace process divides the 525-line picture or frame into two successive 262 1/2-line fields termed odd (lines 1,3,5...) and even (lines 2,4,6...). The 262 1/2 lines of the odd field are scanned in 1/60 seconds, followed by scanning of an additional 262 1/2 lines of the even field, with the even-field lines occupying the spaces between the lines of

the odd field. In effect, the raster scanned by either field alone may be considered to create a white or colored image interleaved with an unmodulated black raster (FIGURE 1). During the next following field, the black lines of the black raster of the previous field are overwritten by the white lines of the following field, but rather than eliminating the visibility of the black raster, the subjective effect or illusion is to create an apparent vertical drift of the black raster. The moving black raster is easily seen when viewing a wide-screen display at close range.

Another artifact caused by interlaced scanning results from the visibility of the scanning lines on the edges of moving objects. This results from a difference in position of the moving object from field to field. The edges of objects in motion have half the nominal vertical resolution and take on a ragged or serrated appearance broken by the clearly visible black scan lines. FIGURE 2a illustrates the effect of a black circular object in motion on a white background with the serrate edges clearly visible.

According to the present invention, a system for producing an image of a scene which is line scanned in an interlaced manner producing frames of successively generated first and second fields of field-interlaced line-scan video signals, each frame of which is representative of the scene comprises:

means responsive to said interlaced line-scanned video signals for generating successive fields of a first progressive non-field-interlaced video signal alternating in each generated field between lines of successive ~~different~~ fields of said interlaced signals;

means, including storage for at least one line of said video signals, responsive to said interlaced line-scanned video signals for generating successive fields of a second progressive non-interlaced video signal alternating in each generated field between lines from a field of said field-interlaced line-scanned video signals and interstitial lines derived solely from adjacent lines of the same field of the field-interlaced signals;

means responsive to said interlaced line-scanned video signals for detecting motion in said scene; and

means for selectively displaying said first progressive non-interlaced video signal in the absence of motion, and said second progressive non-interlaced video signal in the presence of motion.

FIGURE 1 represents a scanned image containing one field of information and showing the "black raster";

FIGURE 2 represents a full frame image of a moving circular object displayed by interlaced line scanning showing a serrated-edge effect;

FIGURES 3 and 9 illustrate in block-diagram form embodiments of the invention of the parent application in which interplation of successive lines generates interstitial lines for display;

FIGURES 4, 5 and 6 show details of the embodiment of FIGURE 3 and a modification thereof;

FIGURE 7 is an alternative, using instead a field-delay memory for generating interstitial lines for display;

FIGURE 8 is a television broadcast receiver incorporating the display;

FIGURE 10 is a diagram aiding in understanding of the arrangement of FIGURE 9;

FIGURES 11 and 14 are other arrangements described also in the parent application, in which a memory of 527 horizontal lines allows repeated reading of a full NTSC frame without loss of incoming information, FIGURE 14 being an arrangement in which repeated full-frame information further has the line-scan structure reduced by estimation;

FIGURE 12 represents the memory of FIGURE 11 at different times; and

FIGURE 13 is an embodiment of the present invention which displays either alternate current and field-or-frame stored data or alternate current and estimated-line date, depending on the presence or absence of motion in the scene.

In the configuration of FIGURE 3, standard analog NTSC composite interlace-scanned color television signals are applied to a terminal 10 from a source (not shown) and are converted to digital form by an analog-to-digital converter 12 operated at a clock rate under the control of a clock signal applied to a terminal 14 from a source (not shown). The clock signals are also applied to appropriate portions of the remainder of FIGURE

3 for timing of the various operations. Generally speaking, the digitized video is applied to an estimator 300 which produces interstitial estimated lines at a double rate for application to a display. Digitized composite video is applied to a luminance-chrominance decoder illustrated as a block 14 which separates the luminance (Y) and the two chrominance signals (I,Q) and applies them to luminance, I and Q estimators 16, 17 and 18, respectively. Each estimator produces a succession of lines of unmodified video (F_u) delayed from the current video by H (the time for one horizontal line, which for U.S. standards is about 63μS). Each estimator also contemporaneously produces lines of estimated or interpolated video (F_e). The delayed unmodified video derived from the luminance information F_{uY} is applied to a first in-first out (FIFO) buffer 20 which may comprise for example a CCD delay line. The estimated video derived from the luminance information F_{eY} is similarly applied to FIFO buffer 22. The unmodified delayed video derived from the I and Q color information (F_{uI}, F_{uQ}) is applied to FIFO buffers 24 and 26, respectively, and the estimated color information (F_{eI}, F_{eQ}) is applied to buffers 28 and 30. Each of the six buffers receives data continuously, and the buffers are read out alternately in pairs 20,22; 24,28; 26,30 to continuously produce separate Y, I and Q output signals. The structure of the buffers may be similar to that described in U.S. Patent Application Serial No. 124,107 filed 25 Feb 1980, (corresponding to GB 2071960A).

The buffers are arranged for accepting input signal clocked at one rate and for reading out the signal at a double rate. The double-rate operation during read-out increases the bandwidth of the signal by a factor of two and also shortens the duration of the signals by a factor of two. Consequently, each active line of video which normally occurs in approximately 53 microseconds (μS) and which is written into a buffer in 53μS is read out of the buffer in about 26 μS. To produce continuous video, a three-pole double-throw toggle switch or

electronic gate 32 has a toggle 32a coupled to the outputs of the buffers 20 and 22 for selectively coupling each buffer to an output digital-to-analog converter (DAC) 34. Similarly, a toggle b of switch 32 is arranged to couple the outputs of buffers 24 and 28 alternately to a DAC 36, and a toggle c couples the output of buffers 26 and 30 to a DAC 38. The separate Y, I and Q are reconstituted and filtered to produce reconstituted analog signal free from quantizing steps. The reconstituted Y, I and Q signals are applied to a matrix circuit 40 which generates R, G and B signals which are applied to a display unit including a kinescope operated at a 31.5 KHz rate for scanning 262 1/2 lines of delayed unprocessed video alternated with 262 1/2 lines of estimated video in 1/60 second for a total of 525 lines.

Thus, the arrangement of FIGURE 3 for each 262 1/2-line field of interlaced incoming video produces and displays 525 lines of progressively scanned or non-interlaced video. Such an image more closely approximates the appearance of a flat-field display (a display not having scanning lines), as illustrated by the image of a moving circular object displayed in interpolated manner shown in FIGURE 2b.

FIGURE 4 illustrates FIFO buffer pair 20, 22 in more detailed block form. In FIGURE 4, estimated signal F_e is applied to an input terminal 410 and coupled to the inputs of estimated-signal delay lines D_{e1} and D_{e2}. Unmodified delayed signal F_u is applied to an input terminal 412 and is coupled to the inputs of clocked delay lines D_{n1} and D_{n2} which may be CCD delay lines. A write clock generator is coupled, through switches 32e and 32b, in the positions shown, to delay lines D_{e2} and D_{n2} whereby D_{e2} and D_{n2} are clocked simultaneously at a low rate for loading with the estimated and unmodified signals, respectively. The loading occurs in approximately 53 μS. During the loading interval, output terminal 414 is coupled by way of switch 32a to the outputs of delay lines D_{e1} and D_{n1} for receiving a signal from whichever delay

line is clocked. In the positions shown, read clock 416 is coupled by switch S2 and switch 32c to clock D_{n1}, which reads out at twice the write-in rate. Switches 32a, 32b and 32d are operated simultaneously by a switch control circuit 418 which receives horizontal sync indicative of the beginning of each incoming horizontal line. The horizontal sync signal may be derived for example from a sync separator (not shown) coupled to input terminal 10 of FIGURE 3 to which the analog video is applied. Switches 32a, d and e are operated from the positions shown in FIGURE 4 at the occurrence of the next horizontal sync interval. The switches are operated at each horizontal sync time so that they alternate positions. Switch S2 is operated at twice the rate of switches 32. Control of switch S2 is accomplished by resetting a counter and switch control circuit 420 at the time of occurrence of each incoming horizontal sync pulse. Counter 420 counts read clock pulses equal to the number of cells of storage of a delay line and toggles switch S2 so as to couple read clock generator 416 to the second delay line to be read out just as the first of the pair is emptied. Thus S2 normally toggles near the time of the center of aline of incoming video. Thus, video is continuously available at output terminal 414. FIGURE 4b shows as F_e, F_u the video signals applied to either terminal 410 or 412, which signals are substantially identical. The outgoing video 430 composed of alternate time-compressed F_e, F_U segments is also shown in time relationship therewith.

FIGURE 5 illustrates the construction of an estimator such as estimator 16 of FIGURE 3. In FIGURE 5, input signal is applied to a one-line (1H) delay line 510 and to an input of an adder or summing circuit 512. Also applied to another input of adder 512 is video signal delayed by 1H. The output of the adder is a signal having an amplitude equal to the sum of the amplitudes of the input signals. In order to normalize the signal to produce a signal having an amplitude equal to the arithmetic average of the input and delayed input signals,

the amplitude is divided by two in an attenuator 514. The averaged output signals is applied to an output terminal 516 and represents estimated output signal Fe. The undelayed input signal is also applied to an output terminal 518 and represents output signal F_u.

Other estimators may be used. FIGURE 6 illustrates a square-law interpolator in which the input signal is applied to a cascade of 1H delay lines 612, 614 and 616. The input and output signals of each delay line are applied to individual multipliers 618, 626, 628, and 630 which may be standard 8x8 multipliers for multiplying the signals by a known function (obtained from table look-up ROM 620). Multiplier ROM 620 generates a running variable in response to horizontal sync pulses applied to an input terminal 624 and applies the running variable as a second input to multipliers 618, 626, 628 and 630. The multiplied output of the multipliers is applied to a summing circuit 632 to generate at an output terminal 634, an estimated value F_e of an interstitial signal as described in more detail in U.S. Patent Application Serial No. 262,619 filed 11 May 1981, (corresponding to GB 2100092A.) The unmodified lines F_u are obtained from the delayed input signal 610 at the output of the 1 H delay line 612 and are applied to the output terminal 636.

The arrangement of FIGURE 3 when used with the square-law interpolator of FIGURE 6 requires three such interpolators. The arrangement of FIGURE 9 by comparison with the arrangement of FIGURE 3 produces a flat field display from interlaced composite video by the use of a single square-law interpolator and only two FIFO buffers. In FIGURE 9, composite video which may be either analog or digital is applied by way of an input terminal 910 to the input of a square-law interpolator 912 and to a cascade of delay lines 914-918. The output of delay line 914 is designated F_n, and the outputs of delay lines 916 and 918 are designated F_{n+1} and F_{n+2}, respectively. The corresponding undelayed input signal is designated F_{n-1}, corresponding to the designations used in the

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aforementoned Powers patent application. The output of interpolator 912 designated as $F_{n+1/2}$ is applied to an even-line buffer 920, while the signal F_n delayed by delay line 914 is applied to an odd-line buffer 922. The outputs of buffers 920 and 922 are applied to the terminals of a switch or gate illustrated as a toggle switch 925. Switch 925 couples the output signals from buffers 920 and 922 by way of two paths to outputs of a luminance chrominance decoder 924. One of the two paths includes a delay 926. The decoder produces Y, I and Q signals which are applied to a matrix 928 in which R, G and B signals are generated which are applied to a display 930. The delay of each of delay lines 914-918 is set to slightly exceed 1H. For the NTSC system, the excess delay equals the time of 1/2-cycle of the color subcarrier (SC/2). This is explained in greater detail by reference to FIGURE 10, which illustrates sample points on portions of four successive horizontal lines 1010-1016. For purposes of illustration, the sampling is assumed to be at the rate of 4 x SC and phased on the I axis. The lower line 1016 represents the current input line F_{n-1}, while lines 1014, 1012, and 1010 corresponds to F_n, F_{n+1}, and F_{n+2}, respectively. The relative phase of the chrominance component is shown for each sample. Also shown is a dotted line 1018 representing a line of estimated video currently being interpolated from the surrounding four scanned lines of incoming video. Assuming that the pixel currently being estimated is 1020, it is clear that if delays 914-918 each have a value of 1H that the estimate would be formed from the values of pixels 1022-1028 vertically arrayed about point 1020. However, with such an array, the estimate would be made from four points, two of which have a value of Y-I and two having a value of Y+I. Consequently, the chrominance value would be suppressed, and the resulting estimated value would include only luminance. This monochrome estimate is prevented by the use of delay in excess of 1H by the amount of half a subcarrier cycle, which is approximately

140 nanoseconds for standard NTSC. With these delays, the interpolation for point 1020 is derived from four nearby samples 1030-1036 which lie along a diagonal and are outlined by a line 1040. All the samples 1030-1036 have the same subcarrier phase, so that the chrominance value does not cancel from the value of the estimated pixel.

The interpolation in interpolator 912 produces an estimated line of video 1018 between input lines 1012 and 1014, thereby producing a line of video designated $F_{n+1/2}$ concurrently with the current line of video. Since two lines of video are being generated simutaneously, time compression must be used as described in conjunction with FIGURE 3, and toggle 925 is used to arrange the estimated and unchanged lines into a time-multiplexed or time-alternating pattern for further processing. Delay line 926 has a delay of 1/2 H which because of the time compression has the same effect as a 1H delay at the standard rate. Luminance-Chrominance decoder 924 creates sum and difference signals to create luminance and chrominance signals, respectively. The I and Q signals are separated by phase detection relative to burst, and the resulting Y, I and Q signals are applied to matrix 928 for converion to R, G and B which are applied to display 930 for display at a 31.5 KHz scan rate. Thus, the arrangement of FIGURE 9 accepts interlaced composite video and produces at the field rate a flat-field display consisting of lines of unmodified video alternated with lines of square-law estimated video. Thus the number of lines being displayed is doubled, which reduces the visibility of the line-scan structure.

The arrangement of FIGURE 7 uses a field store for generating a full raster of 525 lines of non-interlaced video for display, derived from fields of interlaced incoming video. In FIGURE 7, interlaced fields of composite color signals having horizontal lines of video identified by horizontal sync signals recurring at a 15,734 Hz rate are applied by way of an input terminal 701 to a timing control circuit 702 and to an A/D converter

704. The signals are digitized in ADC 704 and are applied as current signal to the input of a field delay 706 and to a FIFO buffer 708. For each line of current video applied to the input of FIFO buffer 708, a corresponding line from the previous field is applied from the output of delay 706 to a FIFO buffer 710. Conceptually, the current and field-delayed signals applied to buffers 708 and 710 correspond to the current and estimated signals applied to the buffers in FIGURE 3. Buffers 708 and 710 receive their input signals continuously and read out the signals sequentially at a line rate double that of either of their input signals (31.5 KHz) as described in conjunction with FIGURE 4. The 31.5 KHz signals at the outputs of buffers 708 and 710 are alternately coupled to a conductor 712 by a toggle switch or gate 714 controlled by a switch drive control circuit 716 synchronized by timing control circuit 702. Thus, double-rate or 31.5 KHz time-compressed video signals appear on conductor 712 and are applied to a luminance-chrominance decoder 716 for separating the Y, I and Q components of the composite signal for conversion to analog by a DAC array 718. The analog Y, I and Q signals are applied to matrix and video drive circuits illustrated as a block 720, which drives a display tube 722 scanned at 31.5 KHz, twice the horizontal rate of the incoming signal. The vertical deflection rate is 1/60 second, the normal field rate of the incoming video signal. The arrangement of FIGURE 7 requires only a field store to produce a progressively scanned non-interlaced display of 525 lines in 1/60 seconds for NTSC (625 lines in 1/50 second for PAL and similar signals). This reduces the line-scan pattern and gives a better approximation of a flat field display without objectionable increase in flicker. The arrangement of FIGURE 7 has the advantage of requiring only a field store in order to produce the progressively scanned non-interlaced display, but has the disadvantage that each displayed raster consists of a current field and the preceding field. During a shift of scene, this can result in the display of a raster scan

consisting of interleaved new and old-scene information. Also, the flicker rate cannot be increased by more than a factor of 2:1. The arrangement of FIGURE 11 includes a memory capable of storing slightly more than one frame of incoming information, and allows a progressively scanned non-interlaced display in which the flicker rate is increased for better simulation of a flat field. In FIGURE 11, analog interlaced video is applied by way of an input terminal 1110 to an ADC 1112 and to a synchronizing circuit 1114. Parallel-format digital information is applied to a memory with an architecture which is rendered easiest to understand by depiction as a wheel 1116. The wheel has a thickness of 8 bits, corresponding to the number of input lines, and the distance from the inner to the outer radius represents the number of samples per horizontal line, for the case of NTSC signals sampled at four times subcarrier, this corresponds to 910 bits. Thus, each pie-shaped section represents 910 samples each of 8 bits. Signal is applied to the memory by a write address generator depicted as a wiper 1118 which writes each line of incoming video into a pie-shaped segment such as 11002, so that the oldest information in each line appears at the outer edge of the wheel and the newest pixel information is stored in the 8 memory bits at the innermost radius. In the position shown, wiper 1118 started a field by writing line 1 of field 1 into pie-shaped segment 11001 and then in succession wrote lines 3,5,7 into segments 11003, 11005, 11007, respectively, and so forth about the wheel. The field which was started by writing into 11001 was completed by writing half a line into segment 11525, thereby completing 262 1/2 lines or one field.

Memory segment 11525 as shown in FIGURE 11 is being addressed by a READ wiper 1134 which rotates in the direction shown by the arrow about the memory wheel, following WRITE wiper 1118 by one horizontal line, corresponding to one segment. A corresponding READ wiper 1136 on the opposite side of the memory wheel rotates in

the same direction as READ WIPER 1134, but one field later whereby wiper 1136 reads older information.

A toggle illustrated as a switch 1138 is operated at 2_{fH} so as to alternately connected READ wipers 1134 and 1136 to an output conductor 1140 which couples the signals to a luminance-chrominance decoder 1142 which decodes the signals into Y, I and Q components which are passed through a matrix 1144 to a display 1146 for progressively scanned display of lines taken alternately from positions on the memory wheel one field apart.

In FIGURE 11, WRITE wiper 1118 is shown as having just finished line writing 525 of the first or odd field into memory segment 11525, and is in the process of writing the first line of the next field (line 2 of the even field) into segment 11002. READ wiper 1134 follows WRITE wiper 1118 by one memory segment, and corresponding wiper 1136 rotates about the wheel in the same direction as READ wiper 1134. When READ wiper 1134 is on segment 11525, READ wiper 1136 is on an empty address adjacent address 11001.

During the next incoming horizontal line of information, WRITE wiper 1118 will write into segment 11004, while READ wipers 1136 and 1134 step to segments 11001 and 11002, respectively, and line 1 of the odd field is read out from segment 11001 and just-laid-down line 2 of the even field is read from segment 11002. The reading proceeds alternately at an 8xSC rate providing video time-compressed by a factor of 2. Consequently, the reading-out of the two lines of video in segments 11001 and 11002 occurs within the time required to write a single line into segment 11004.

As time progresses during the second field, wiper 1118 proceeds in a clockwise direction writing even lines into memory segments, and read-out proceeds with READ wiper 1136 reading out odd lines while wiper 1134 reads the corresponding just-laid-down even line.

Eventually, WRITE wiper 1118 will reach a position such as is shown in FIGURE 12a at which it has

just finished writing even line 524 into memory segment 11524 and has stepped to the next following empty segment 12001. At the same time, READ wiper 1134 steps to segment 11524 just vacated by WRITE wiper 1118, and simultaneously READ wiper 1136 steps to segment 11525. During the next line interval of the incoming signal, segment 12001 is written into or filled with the first line of the first field of the next frame. At the time when segment 12001 is just full, reading of segment 11525 is completed. WRITE wiper 1118 steps to the last empty segment 12003, while at the same time READ wiper 1136 steps to the next segment 11002 and READ wiper 1134 steps forward two spaces to segment 11001. This position is shown in FIGURE 12b. While segment 12003 is being filled with the second line of video of the odd field of the second frame, READ wiper 1134 reads line 1 of the preceding frame, followed in quick succession by reading of line 2 of the preceding frame by wiper 1136.

The reading of lines 1 and 2 from segments 11001 and 11002 constitutes the beginning of the second reading of the preceding frame. The reading of the frame occurs in the time required for writing in one field of current information. Since the current information cannot be overwritten into the memory until the second reading of the presently stored information has occurred, READ wiper 1134 precedes WRITE wiper 1118 in its clockwise excursion about the memory wheel, until near the end of the incoming first field of the second frame, the wiper positions are as illustrated in FIGURE 12c.

In FIGURE 12c, wipers 1134 and 1136 are positioned to read the last portions of the preceding frame by a second reading of lines 524 and 525 from memory segments 11524 and 11525. WRITE wiper 1118 is positioned at the memory location which was 11523 and writes into it line 2 of the second field of the second frame, thus converting memory segment 11523 to identification number 12002. When reading of 11524 and 11525 is completed, READ wiper 1136 steps clockwise to 12001 in readiness for the

next read cycle and wiper 1134 steps counter clockwise by one step to segment 12002, and WRITE wiper 1118 steps clockwise by one memory segment to 11525. This positions READ wiper 1134 behind WRITE wiper 1118 for the next reading cycle as illustrated in FIGURE 12d, during which READ wiper 1136 steps successively through odd segments 12001, 12003...and READ wiper 1134 steps through even segments 12002, 12004 in a corresponding manner.

Near the end of the first reading of the second frame, the wiper positions are as shown in FIGURE 12e. Wipers 1134 and 1136 are positioned to read lines 524 and 525 from segments 12524 and 12525, and WRITE wiper 1118 is positioned to write into segment 11522 (now containing "old" data, or essentially empty). Segment 11522 is overwritten with line 1 of field 1 of a third frame (becoming 13001) at the same time that the last two lines of Frame 2 are read from 12524 and 12525. The second reading of Frame 2 begins with wiper 1134 jumping ahead by two lines to segment 12001 while wiper 1136 steps ahead to 12002, in readiness for the second reading of lines 1 and 2 of Frame 2. At this time, WRITE wiper 1118 steps ahead to segment 11524 preparatory to overwriting into the segment the second odd line of field 3, connecting it to identification 13003. It will be recognized that this is the same condition as that prevailing at the beginning of the second reading of Frame 1. The operation continues with the cyclical advancing and retarding of the READ wipers relative to the WRITE wiper position to produce multiple readings of each frame while at the same time providing continuous writing into the frame store, which contains only two lines of memory more than a complete frame. As a result of the two extra memory segments over a frame, the operation results in a counter clockwise progression or "precession" of the two "empty" segments about the periphery of the wheel.

FIGURE 11b is a more detailed block diagram of control portions of the memory arrangement of FIGURE 11a. Those elements in FIGURE 11b corresponding to elements in

FIGURE 11a are designated by the same reference numerals. Memory 1116 is illustrated as a standard rectangular memory having 527 lines each consisting of 910 pixels each having 8 bits. The address of each pixel includes a most-significant-bit (MSB) relating to the line number and a least-significant bit (LSB) relating to the pixel number. The WRITE pixel addresses are generated by a pixel address counter 1148 which receives 4xSC clock pulses and produces 910 unique addresses which are applied to memory 1116 as the LSB WRITE address. The MSB of the WRITE addresses are produced by a divide-by-527 counter chain illustrated as a block 1150 which counts horizontal-rate pulses and produces as a decoded output the MSB control of the address of WRITE wiper 1118. As described, WRITE wiper 1118 progresses through the memory periodically without stopping.

READ wiper 1136 makes a regular progression through the memory in synchronism with the WRITE wiper but offset therefrom by a constant 265 lines. Consequently, the MSB for the addresses for READ wiper 1136 can be generated by the decoded output of a divide-by-527 counter chain 1152 which is reset to zero by a decoder 1154 each time counter 1150 reaches the count of 265. The MSB produced by counter chain 1152 is coupled to the MSB portion of the READ address of memory 1116 by way of a half-line switch 1156 operated by a 2 fH signal derived by a decoder 1158 coupled to address counter 1148. Decoder 1158 decodes the output of counter 1148 and produces an output pulse each time the count reaches either 455 or 910. The LSB of the read address is generated by a pixel address counter 1160 driven by an 8xSC clock which results in reading of each line of information at double the writing rate.

The MSB for control of READ wiper 1134 is generated by a divide-by-527 counter chain 1162 which counts horizontal-rate signals and produces address control signals applied to the MSB input of the memory by way of switch 1156.

The stepping forward and stepping back of the position of READ wiper 1134 relative to WRITE wiper 1118 is accomplished by a 263-decoder 1164 which responds to a count of 263 by counter chain 1150 and which sets counter 1162 to the count of 262, whereby wiper 1134 follows wiper 1118. A 527-decoder 1165 responds to a full count of 527 of counter 1150 and at that time sets counter 1162 to a count of 1. Since counter chain 527 resets itself to a count of zero upon the occurrence of the full count of 527, the resetting causes the addresses for wiper 1134 to precede the addresses for wiper 1118 by one line, as required.

Multiple readings of the same frame can result in an error in the chrominance phase which results from lack of completion of a full four-field chrominance frame. For this purpose, the output signal applied to luminance chrominance decoder 1141 may include a phase shifter for shifting the chrominance phase at the beginning of reading of each new frame. For this purpose, a 001-decoder 1166 is coupled to the read MSB line and sets a flip-flop coupled to the phase-control input of decoder 1142.

The arrangement of FIGURE 14 uses the full-frame-plus-two-lines system such as 1100 of FIGURE 11 together with an estimator such as the estimator of FIGURE 3 for producing repetitive full frames of 525 lines from memory 1116 interleaved with 525 estimated interstitial lines for producing a progressive display of 1050 lines with a high flicker rate. In FIGURE 14, double-rate (525 line in 1/60 second) progressive video is produced at the output of switch 1138 as described in conjunction with FIGURE 11. This double-rate information is passed through a luminance-chrominance decoder 1410 for separation into Y, I and Q components which are applied to an estimator 300 of the type shown in FIGURE 3, except that the delays are H/2 (corresponding to about 31.7 μS) for generating interstitial lines. Estimator 300 estimates the value which an interstitially scanned line would have, generating pairs of unmodified and estimated lines which

are time-compressed by a further factor of two. These estimates are made for each of the Y, I and Q signals, which are then applied to a DAC array 1420 for producing analog Y, I and Q signals for application by way of a matrix 1422 to a display 1424 for producing a progressively scanned image of 1050 lines each 1/60 second.

FIGURE 8 illustrates a broadcast television receiver incorporating the display units according to the invention. In FIGURE 8, an antenna 802 is coupled to a tuner 804 which selects one channel from among those received by the antenna and converts that channel to an intermediate frequency (IF) for amplification by an IF amplifier 806. The amplified signal is applied to a second detector 808 for demodulation to baseband. At the output of the second detector is a composite television signal together with an audio signal FM-modulated onto a 4.5 MHz carrier. The FM carrier is selected by an audio filter 810 and applied to an audio FM detector 812 for producing baseband audio signal which is applied to an audio amplifier 814 and speaker 816. The composite video signal at the output of a second detector is applied to a sync separator 820 which separates horizontal sync for use in keying an AGC program or control circuit 822 and for other purposes in the receiver and display unit. The composite video applied to programmer 822 is keyed and the amplitude of the keyed signal is used to control the gain of controllable stages in tuner 804 and amplifier 806. The composite video is also applied to a display unit according to the invention which may be a display unit similar to display unit 700 of FIGURE 7. As described, display unit 700 receives a field of interlaced signal each 1/60 second and produces in a like interval a progressively scanned or non-interlaced raster including information from the current field and from the previous field. Naturally, an estimator-type display as described in conjunction with FIGURE 3 can be used instead of display 700 in FIGURE 8.

As mentioned, the arrangement of FIGURE 7 is subject to a problem in the presence of a change in scene or substantial motion in a scene, in which case multiple interlaced images appear on the scanned raster. However, in the absence of motion as for example in areas in which there is an unchanged background, the display produced by progressive scanning of current lines of video interlaced with lines from a field store gives an accurate representation of the image. The interpolators of FIGURES 3 and 9 merely produce an estimate of the interstitial video, which may sometimes be erroneous. However, the effects of motion do not greatly influence the estimated video. FIGURE 13 illustrates an arrangement including an estimator and a field or frame-store memory together with an arrangement for switching between estimates, depending upon whether motion exists in a particular portion of the raster being estimated. In FIGURE 13, digital video is applied by way of an input terminal 1310 to inputs of an interpolating line estimator 900 and a field or frame-store memory system 700. Estimator 900 is similar to the square law interpolator designated generally as 900 and illustrated in FIGURE 9. Field or frame-store memory system 700 is similar to the system of FIGURE 7. The input signal applied to input terminal 1310 is also applied to a motion detector 1312 for comparison with delayed data for establishing the presence or absence of motion by generation of a switch control signal on an output conductor 1314. The signal on on conductor 1314 is applied to a multiplex switch 1316 which in the presence of motion couples to an output circuit the signal from estimator 900 and in the absence of motion couples to the output circuit the output of the field or frame store memory. The output circuit may include a luminance-chrominance decoder, matrix and display as illustrated in FIGURES 7 or 9.

Motion detector 1312 may include a first and second delay line 1320 and 1322 coupled respectively to receive low-pass filtered current and delayed

signals and to further delay them by a transmission-line delay such as a CCD delay line. At each step of the delay as the signal passes through delays 1320 and 1322, comparators illustrated generally as 1324 compare each current pixel with the ~~field~~-delayed corresponding pixel and each produces a signal indicative of the degree of match. The signals are summed through weighting resistors designated generally as 1326 and applied to a comparator 1328 which compares the weighted signal with a predetermined threshold illustrated as a battery 1330 for deciding whether there is or is not motion locally in the scene. In order to match the time of occurrence of the signals being processed with the time of occurrence of the control signal, further delays 1332 and 1334 may be required. Other known forms of motion detector may also be used.

Other embodiments of the invention will be apparent to those skilled in the art. In particular, display functions not shown may be incorporated at suitable points; such functions include gamma correction, vertical and horizontal aperture correction, color, tint, brightness and contrast control, clamping, delay matching, coring and paring the like, which are all known funtions and which may be implemented in known fashion. While the embodiments shown perform their functions in a digital mode, analog signal processing can be used.

CLAIMS: 1. A system for producing an image of a scene which is line scanned in a field-interlaced manner for producing frames of successively generated first and second fields of line-scan video signals each frame of which is representative of the scene, comprising:

means responsive to said interlaced line-scanned video signals for generating successive fields of a first progressive non-field-interlaced video signal alternating in each generated field between lines of successive fields of said interlaced signals;

means, including storage for at least one line of said video signals, responsive to said interlaced line-scanned video signals for generating successive fields of a second progressive non-interlaced video signal alternating in each generated field between lines from a field of said field-interlaced line-scanned video signals and interstitial lines derived solely from adjacent lines of the same field of the field-interlaced signals;

means responsive to said interlaced line-scanned video signals for detecting motion in said scene; and

means for selectively displaying said first progressive non-interlaced video signal in the absence of motion, and said second progressive non-interlaced video signal in the presence of motion.

2. A system according to claim 1 wherein said second non-interlaced signal alternates between lines of said interlaced line-scanned video signal and interstitial lines generated by interpolation from such adjacent lines.

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