CLAIMS

1. A non-volatile SRAM memory cell including an SRAM (static random access memory) and a non-volatile memory unit comprising:

the SRAM including a first access transistor, a second access transistor, a first load transistor, a second load transistor, a first drive transistor, and a second drive transistor,

a first storage node between the first load transistor and the first drive transistor connected in series, one end of the first load transistor being connected with one end of the first drive transistor, and

a second storage node between the second load transistor and the second drive transistor connected in series, one end of the second load transistor being connected with one end of the second drive transistor,

wherein the other end of each of the first load transistor and the second load transistor is connected with a power supply line, and the other end of each of the first drive transistor and the second drive transistor is connected with a reference voltage line, and

the first access transistor has one end connected with the first storage node and with gates of the second load transistor and the second drive transistor, the other end connected with a complementary first bit line, and a gate connected with a word line; and the second access transistor has one end connected with the second storage node and with gates of the first load transistor and the first drive transistor, the other end connected with a complementary second bit line, and a gate connected with the word line,

the first access transistor, the second access transistor, the first load transistor, the second load transistor, the first drive transistor, and the second drive transistor of the SRAM each include a gate insulating film having a thickness less than or equal to 4 nm, and

the non-volatile memory unit includes a first memory cell and a second memory cell,

the first memory cell includes: a first drain region connected with the first storage node; a first source region connected with a source line; a first memory gate structure disposed between the first drain region and the first source region and including a first lower memory gate insulating film, a first charge storage layer, a first upper memory gate insulating film, and a first memory gate electrode stacked in this order; a first drain side select gate structure including a first drain side gate insulating film and a first drain side select gate electrode stacked between the first drain region and the first memory gate structure, the first drain side select gate structure being disposed adjacent to a first sidewall of the first memory gate structure, with one first sidewall spacer disposed between the first sidewall of the first memory gate structure and the first drain side select gate structure; and a first source side select gate structure including a first source side gate insulating film and a first source side select gate electrode stacked between the first source region and the first memory gate structure, the first source side select gate structure being disposed adjacent to a second sidewall of the first memory gate structure, with another first sidewall spacer disposed between the second

sidewall of the first memory gate structure and the first source side select gate structure,

the second memory cell includes: a second drain region connected with the second storage node; a second source region connected with the source line; a second memory gate structure disposed between the second drain region and the second source region and including a second lower memory gate insulating film, a second charge storage layer, a second upper memory gate insulating film, and a second memory gate electrode stacked in this order; a second drain side select gate structure including a second drain side gate insulating film and a second drain side select gate electrode stacked between the second drain region and the second memory gate structure, the second drain side select gate structure being disposed adjacent to a first sidewall of the second memory gate structure, with one second sidewall spacer disposed between the first sidewall of the second memory gate structure and the second drain side select gate structure; and a second source side select gate structure including a second source side gate insulating film and a second source side select gate electrode stacked between the second source region and the second memory gate structure, the second source side select gate structure being disposed adjacent to a second sidewall of the second memory gate structure, with another second sidewall spacer disposed between the second sidewall of the second memory gate structure and the second source side select gate structure, wherein

the one first sidewall spacer, the other first sidewall spacer, the one second sidewall spacer, and the other second sidewall spacer each have a width more than or equal to 5 nm, and the first drain side gate

insulating film, the first source side gate insulating film, the second drain side gate insulating film, and the second source side gate insulating film each have a thickness less than or equal to 4 nm.

2. The non-volatile SRAM memory cell according to claim 1, wherein

the first charge storage layer is not disposed in the one first sidewall spacer and the other first sidewall spacer, and the second charge storage layer is not disposed in the one second sidewall spacer and the other second sidewall spacer.

3. The non-volatile SRAM memory cell according to claim 1, wherein

the first load transistor and the second load transistor are arranged in an N-type well, and

the first access transistor, the second access transistor, the first drive transistor, the second drive transistor, and the non-volatile memory unit are arranged in a P-type well disposed adjacent to the N-type well.

4. The non-volatile SRAM memory cell according to claim 1, further comprising:

a drain side select gate line connected with the first drain side select gate electrode and the second drain side select gate electrode,

a source side select gate line connected with the first source side select gate electrode and the second source side select gate electrode, and

a memory gate line connected with the first memory gate electrode and the second memory gate electrode.

5. A non-volatile semiconductor memory device comprising the non-volatile SRAM memory cells according to claim 4, the non-volatile SRAM memory cells being disposed in a matrix of rows and columns, wherein

the source line, the drain side select gate line, and the source side select gate line are shared by the non-volatile SRAM memory cells.

6. A non-volatile SRAM memory cell including an SRAM (Static Random Access Memory) and a non-volatile memory unit comprising:

the SRAM including a first access transistor, a second access transistor, a first load transistor, a second load transistor, a first drive transistor, and a second drive transistor,

a first storage node between the first load transistor and the first drive transistor connected in series, one end of the first load transistor being connected with one end of the first drive transistor, and

a second storage node between the second load transistor and the second drive transistor connected in series, one end of the second load transistor being connected with one end of the second drive transistor,

wherein the other end of each of the first load transistor and the second load transistor is connected with a power supply line, and the other end of each of the first drive transistor and the second drive transistor is connected with a reference voltage line, and

the first access transistor has one end connected with the first storage node and with gates of the second load transistor and the second drive transistor, the other end connected with a complementary

first bit line, and a gate connected with a word line; and the second access transistor has one end connected with the second storage node and with gates of the first load transistor and the first drive transistor, the other end connected with a complementary second bit line, and a gate connected with the word line, and

the non-volatile memory unit including a first memory cell and a second memory cell, the first memory cell including a first drain side select transistor, a first source side select transistor, and a first memory transistor between the first drain side select transistor and the first source side select transistor connected in series, the first drain side select transistor having one end connected with the first storage node, the second memory cell including a second drain side select transistor, a second source side select transistor, and a second memory transistor between the second drain side select transistor and the second source side select transistor connected in series, the second drain side select transistor having one end connected with the second storage node, the first source side select transistor and the second source side select transistor each having one end connected with a source line, and

the first memory transistor and the second memory transistor each including a charge storage layer into which charge is injected by a quantum tunneling effect that occurs in accordance with a charge storage gate voltage applied to a memory gate electrode,

wherein in the SRAM, the first access transistor, the second access transistor, the first load transistor, the second load transistor, the first drive transistor, and the second drive transistor each include a gate

insulating film having a thickness less than or equal to 4 nm, and

in the non-volatile memory unit, neither the drain region nor the source region is formed between the first drain side select transistor and the first memory transistor, and between the first source side select transistor and the first memory transistor, and between the second drain side select transistor and the second memory transistor, and between the second source side select transistor and the second memory transistor, and

when charge is to be injected into the charge storage layer of any one of the first memory transistor and the second memory transistor, a voltage of 0 V is applied to the source line and a voltage of 0 V is applied to a gate of the first source side select transistor and to a gate of the second source side select transistor to turn off the first source side select transistor and the second source side select transistor while a power supply voltage VDD less than or equal to 1.5 V is applied to a gate of the first drain side select transistor and a gate of the second drain side select transistor to turn on one of the first drain side select transistor and the second drain side select transistor due to a voltage difference between the first storage node and the second storage node so that a voltage at the first storage node or the second storage node is applied to the first memory transistor or the second memory transistor through any one of the first drain side select transistor or the second drain side select transistor, so as to allow charge injection into the charge storage layer of one of the first memory transistor and the second memory transistor by the quantum tunneling effect while charge injection into the charge storage layer of

the other of the first memory transistor and the second memory transistor is prevented.

7. The non-volatile SRAM memory cell according to claim 6, wherein, when charge is to be injected into the charge storage layer of one of the first memory transistor and the second memory transistor while charge injection into the charge storage layer of the other of the first memory transistor and the second memory transistor is prevented, a voltage of 0 V is applied to the source line and a voltage of 0 V is applied to the gate of the first source side select transistor and to the gate of the second source side select transistor to turn off the first source side select transistor and the second source side select transistor while a power supply voltage VDD less than or equal to 1.5 V is applied to the gates of the first and the second drain side select transistors to turn off one of the first drain side select transistor and the second drain side select transistor that prevent the charge injection into the charge storage layer, due to a voltage difference between the first storage node and the second storage node, so that a depletion layer is formed in a memory well facing the memory gate electrode in any one of the second memory transistor and the first memory transistor while a potential of at least a surface of the memory well is increased in accordance with the charge storage gate voltage applied to the memory gate electrode, so as to reduce a voltage difference between the memory gate electrode and the surface of the memory well to prevent the charge injection into the charge storage layer.

8. The non-volatile SRAM memory cell according to claim 7, wherein

when the depletion layer is formed in the first memory cell, the depletion layer prevents the potential of the memory well of the first memory transistor from being applied to a select gate insulating film of each of the first drain side select transistor and the first source side select transistor, and

when the depletion layer is formed in the second memory cell, the depletion layer prevents the potential of the memory well of the second memory transistor from being applied to a select gate insulating film of each of the second drain side select transistor and the second source side select transistor.

9. A non-volatile semiconductor memory device comprising the non-volatile SRAM memory cells according to claim 6, the non-volatile SRAM memory cells being disposed in a matrix of rows and columns.