Claims

What is claimed:

1. A semiconductor device, comprising:

a semiconductor wafer having a plurality of first conductive vias formed in the semiconductor wafer and a cavity formed in the semiconductor wafer;

a first semiconductor die disposed within the cavity;

a second semiconductor die mounted to the semiconductor wafer over the first semiconductor die and electrically connected to the first conductive vias;

an encapsulant deposited over the semiconductor wafer and second semiconductor die;

a first interconnect structure formed over the semiconductor wafer opposite the second semiconductor die and electrically connected to the first conductive vias; and

a second interconnect structure formed over the second semiconductor die and encapsulant.

2. The semiconductor device of claim 1, further including a heat sink or shielding layer formed over the second semiconductor die.

3. The semiconductor device of claim 1, further including a third interconnect structure formed through the encapsulant around the second semiconductor die.

4. The semiconductor device of claim 1, wherein the third interconnect structure includes a plurality of conductive pillars.

~~5. The semiconductor device of claim 1, further including a plurality of second conductive vias formed through the first semiconductor die or second semiconductor die.~~

~~6. The semiconductor device of claim 1, further including a passive device mounted to the semiconductor wafer.~~

~~7~~1. A semiconductor device, comprising:

a first substrate ~~having~~ including a plurality of conductive vias formed ~~partially~~ through a ~~first~~ surface of the first substrate and a cavity formed partially but not completely through the ~~first surface of the~~ first substrate;

a second substrate disposed within the cavity;

a first semiconductor die mounted to ~~the first~~ a surface of ~~first substrate over~~ the second substrate and ~~electrically connected~~ to the ~~conductive vias~~ first substrate; ~~and~~

~~an encapsulant deposited over the first surface of the first substrate and first semiconductor die~~

a first interconnect structure formed on a first surface of the first semiconductor die and contacting the second substrate and first semiconductor die; and

an encapsulant deposited over the surface of the first substrate and first semiconductor die with a second surface of the first semiconductor die coplanar with a surface of the encapsulant and with a trench of the first substrate adjacent to the cavity completely occupied by the encapsulant.

~~8~~2. The semiconductor device of claim ~~7~~1, wherein ~~a portion of a second surface of the first substrate opposite the first surface of the first substrate is removed to expose~~ the conductive vias ~~and an interconnect structure is formed over the~~

~~second surface of~~ are exposed from the first substrate ~~and electrically connected to the conductive vias~~.

~~9~~3. The semiconductor device of claim ~~7~~1, further including ~~an~~a second interconnect structure formed over the first semiconductor die and encapsulant.

~~10~~4. The semiconductor device of claim ~~7~~1, further including a heat sink or shielding layer formed over the first semiconductor die.

~~11~~5. The semiconductor device of claim ~~7~~1, further including ~~an~~a second interconnect structure formed through the encapsulant around the first semiconductor die.

~~12~~6. The semiconductor device of claim ~~7~~1, wherein the second substrate includes a second semiconductor die.

~~13~~7. The semiconductor device of claim ~~7~~1, further including a passive device mounted to the first substrate.

8. The semiconductor device of claim 1, wherein the first substrate, second substrate, and first semiconductor die include matching coefficients of thermal expansion (CTE) to reduce warpage of the semiconductor device.

~~14. A semiconductor device, comprising:~~

~~a substrate having a plurality of first conductive vias formed partially through a first surface of the substrate and a cavity formed partially through the first surface of the substrate;~~

~~a semiconductor component disposed in the cavity;~~

~~a first semiconductor die mounted to the substrate over the semiconductor component and electrically connected to the first conductive vias; and~~

~~an encapsulant deposited over the first surface of the substrate and first semiconductor die.~~

~~15. The semiconductor device of claim 14, further including an interconnect structure formed over a second surface of the substrate opposite the first surface of the substrate and electrically connected to the first conductive vias.~~

~~16. The semiconductor device of claim 14, further including an interconnect structure formed over the first semiconductor die and encapsulant.~~

~~17. The semiconductor device of claim 14, further including a heat sink or shielding layer formed over the first semiconductor die.~~

~~18. The semiconductor device of claim 14, further including an interconnect structure formed through the encapsulant around the first semiconductor die.~~

~~19. The semiconductor device of claim 14, wherein the semiconductor component includes a second semiconductor die.~~

~~20. The semiconductor device of claim 14, further including a plurality of second conductive vias formed through the first semiconductor die or semiconductor component.~~

~~21. A semiconductor device, comprising:~~

~~a substrate having a plurality of conductive vias formed partially through a first surface of the substrate and a cavity formed partially through the first surface of the substrate;~~

~~a first semiconductor die disposed in the cavity;~~

~~a second semiconductor die mounted to the substrate over the first semiconductor die and electrically connected to the conductive vias; and~~

~~an encapsulant deposited over the first surface of the substrate and second semiconductor die.~~

~~22. The semiconductor device of claim 21, further including an interconnect structure formed over a second surface of the substrate opposite the first surface of the substrate and electrically connected to the conductive vias.~~

~~23. The semiconductor device of claim 21, further including an interconnect structure formed over the second semiconductor die and encapsulant.~~

~~24. The semiconductor device of claim 21, further including a heat sink or shielding layer formed over the second semiconductor die.~~

~~25. The semiconductor device of claim 21, further including an interconnect structure formed through the encapsulant around the second semiconductor die.~~