

Triggered Silicon Controlled Rectifier for RF ESD Protection

Background of the Invention

Abstract

An ESD protection circuit is formed at the input/output interface contact of an integrated circuit to protect the integrated circuit from damage caused by an ESD event. The ESD protection circuit has a polysilicon bounded SCR connected between a signal input/output interface contact of the integrated circuit and a power supply connection of the integrated circuit and a biasing circuit. The biasing circuit is connected to the polysilicon bounded SCR to bias the polysilicon bounded SCR to turn on more rapidly during the ESD event. The biasing circuit is formed by at least one polysilicon bounded diode and a first resistance. Other embodiments of the biasing circuit include a resistor/capacitor biasing circuit and a second diode triggering biasing circuit.

FIG. 4a