



Abstract of the Disclosure:

In a CMOS gate array, each of bonding pads corresponding to input cells for signals and bonding pads corresponding to input cells for supply voltages
5 is formed of a plurality of conductor layers, whereas each of bonding pads (non-connected pads) corresponding to input/output cells not to be used is formed of, for example, the uppermost conductor layer. Thus, the bonding pad (non-connected pad)
10 corresponding to the input/output cell not to be used becomes greater in the thickness of an underlying insulator film and longer in its spacing from a semiconductor substrate in comparison with each of the bonding pad for the signal and the bonding pad for the
15 supply voltage.