

CLOCK DRIVER APPARATUS WITH
PROGRAMMABLE OUTPUT CHARACTERISTICS

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CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation in part of U.S.
10 Patent Application Ser. No. 08/960,408, filed October 29,
1997, by the same inventors herein and entitled Integrated
Circuit Assembly Having Output Pads with Programmable
Characteristics and Method of Operation.

FIELD OF THE INVENTION

15 The present invention relates to clock drivers and
clock trees and, more specifically, to providing clock
drivers and clock trees with programmable output
characteristics.

BACKGROUND OF THE INVENTION

20 In application specific integrated circuits (ASICs)
and in other integrated circuits a clock signal may be
distributed to thousands and perhaps tens of thousands of
"locations." This distribution is conventionally achieved
using clock trees and a typical clock tree consists of a
25 plurality of buffer drivers arranged in stages with each
stage having more outputs than inputs.

If a representative clock tree provides a 1:10 input
to output ratio at each stage and has four stages, then the

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number of clock signal lines increases from 1 to 10, 10 to 100, 100 to 1,000 and 1,000 to 10,000 at stages 1-4, respectively. This staged increase in the number of signal lines provides a like increase in the number of simultaneous or nearly simultaneous clock signal transitions (e.g., from positive to negative and vice versa). Since clock signal transitions are a source of electromagnetic interference (EMI), large numbers of simultaneous clock signal transitions produce an undesirably large amount of EMI. This problem is further exacerbated as semiconductor technologies advance. Reduction in integrated circuit feature size increases the density of clock signal transitions per unit area. Furthermore, faster operating speeds tend to increase a circuit's sensitivity to EMI and other parasitics.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a clock signal driver that permits selection of the shape of the output clock signal.

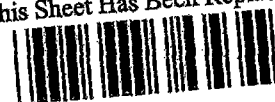
It is another object of the present invention to provide a clock signal driver wherein the amount of signal modification is programmable.

It is also an object of the present invention to provide a clock driver with selectable resistive values so that when those values are combined with load capacitance values, a selectable time constant is effectively achieved.

These and related objects of the present invention are achieved by use of a clock driver with programmable output characteristics as described herein.

In one embodiment, the present invention includes a driver circuit, comprising: a first MOS transistor coupled between a voltage supply and ground and having a first output; a second MOS transistor coupled between a voltage supply and ground and having a second output,

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said first output and said second output coupled together to form a driver circuit output; selection logic coupled to said first and second MOS transistors for selectably enabling one or more of said transistors to produce an
5 output clock signal that transitions under the effects of a time constant that includes a resistive component from said selected one or more of said transistors. The selection logic may be configured to receive a clock signal, a first transistor select signal and a second
10 transistor select signal and to produce a first transistor enable signal that is propagated to said first transistor and a second transistor enable signal that is propagated to said second transistor. The first and second MOS transistors are preferably CMOS transistors.
15 The transistors may be tri-stated to permit a signal to be driven through the transistors output conductor.

In another embodiment, the present invention includes a clock tree comprising: a plurality of clock signal drivers arranged in such a manner as to form a
20 first, second and third stage of clock signal drivers; and wherein at least one of said clock signal drivers includes a first and a second MOS transistor having coupled outputs and selection logic that selectably enabling one or more of said transistors. At least one
25 of said clock signal drivers preferably produces an output clock signal that transitions under the effects of a time constant that includes a resistive component from said selected one or more of said transistors.

In yet another embodiment, the present invention
30 includes a clock signal driving apparatus, comprising: a clock signal input; a clock signal buffer coupled to said clock signal input that buffers a clock signal received from said input and produces a buffered clock signal at an output thereof; and logic that permits modification of the
35 shape of the transitions of said buffered clock signal.



The buffer preferably includes a selectable semiconductor resistive element. The resistive device may be configured as a MOS transistor and the modification logic selected so as to enable or disable the MOS transistor.

- 5 The attainment of the foregoing and related advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention taken together with the drawings.

10 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of a clock tree in accordance with the present invention.

Fig. 2 is a schematic block diagram of a clock signal driver circuit in accordance with the present invention.

- 15 Fig. 3 is a schematic block diagram of selection logic 231 for use in circuit 100 of Fig. 2 in accordance with the present invention.

DETAILED DESCRIPTION

Referring to Fig. 1, a schematic block diagram of a clock tree in accordance with the present invention is shown. The embodiment of Fig. 1 illustrates a representative clock tree having four stages, though it should be recognized that the clock tree may have more or less stages without departing from the present invention.

- 25 Clock tree 5 includes a clock source 8 which is conventionally a crystal oscillator or the like. A clock signal output from source 8 is propagated over line 9 to a first stage (10) buffer driver 11 (hereinafter referred to as a "driver"). The output of driver 11 is delivered to a plurality of second stage (20) drivers, four of which are shown (21-24). While four are shown, it should be recognized that this number can be as large or as small as permitted by known fanout or load determining factors such as impedance, conductor length, etc. The outputs of the



second stage drivers are in turn coupled to the input of third stage (30) drivers 31-36 and the third stage drivers are similarly coupled to fourth stage (40) drivers 41-46. In the illustrated embodiment, clock signals output from the fourth stage are delivered to their destination (functional logic) that is indicated by loads 51-56. It should be recognized that the number of stages and the number of drivers within each stage is dependent upon the number of locations to which the clock signal need be delivered and the fanout ability of each driver, etc., as is generally known.

In accordance with the present invention, some or all of the drivers (11, 21-24, 31-36, 41-46) are configured such that they permit programmable shaping of their output clock signal. The drivers may be controlled individually, in sets (e.g., drivers 31-33, 34-36, 41-43 and 44-46 may each be considered a "set" of drivers), in stages or as otherwise desired by a circuit designer. It should be recognized that the provision of programmable clock signal shaping may be more critical in the latter stages of the clock tree (such as the third and fourth stages of Fig. 1) because the number of nearly simultaneous clock signal transitions is increased at these stages. It should also be recognized that staggering the timing or shape of the clock signals output from the second stage drivers 21-24 creates staggered clock signal transitions throughout clock tree 10.

The ability to program output clock signals is a function of the design of the drivers (as discussed in more detail below with reference to Fig. 2) and the delivery of appropriate control signals. While control signals may be delivered in many known manners (including tying inputs to a particular logic state, etc.), in a preferred embodiment, select lines 60 are provided that propagate signals from control logic 70. Control logic 70 preferably includes one

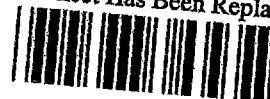
or more data registers and a processor that writes control/select bits to the data registers. The data registers hold the value of a clock driver selection signal as discussed below.

5 Referring to Fig. 2, a schematic block diagram of a clock signal driver circuit 100 in accordance with the present invention is shown. Each of the drivers 11, 21-24, 31-36, and 41-46 may be configured to include driver circuit 100. It is not necessary to configure driver 11
10 with programmable output characteristics if it is the only first stage buffer from source 8. It is preferred, however, that the other drivers or sets or subsets thereof are configured to provide programmable output characteristics.

15 Fig. 2 illustrates that driver circuit 100 has a plurality of CMOS transistors 110,120,130. Appropriate combinational logic, such as an AND gate or the like (111, 121,131), is coupled to the gate of the PMOS and NMOS transistors 112,122,132 and 113,123,133, respectively, to
20 control current flow therethrough. An input clock signal is delivered on line 105 to each of the AND gates. Another input to each of the AND gates is a select line such as one of the select lines 60 of Fig. 1. Each of select lines 60 preferably includes a plurality of individual transistor
25 control lines. Three control lines 161-163 are shown in Fig. 2. A three bit representative selection signal of "101" is indicated as being delivered by these lines. The value 101 (or other value delivered by the control lines) is stored, for example, in the data register of control
30 logic 70.

The output of each CMOS transistor is coupled to a common output line to which load 150 is coupled. The circuit or other componentry driven by driver circuit 100 is represented generally by load 150. Each load has an
35 appreciable capacitance associated therewith and this

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capacitance is represented in phantom lines by capacitor 151.

While clock signals propagating through drivers are often illustrated as having a crisp square wave form, in reality these clock signals have rounded corners or, from another perspective, curved or sloping transitions. The rounded corners and curved transitions are a result, at least in part, of the time constant created by inherent or parasitic resistance in the clock signals current path and capacitance 151 in the load.

Circuit 100 permits selection of the value of resistance in the clock signal's current path (within the driver) and this selected value in combination with the capacitance of the load creates a time constant that determines the shape of the output clock signal transitions. The provision of selectable time constants permits a circuit designer to soften and/or separate clock signal transitions. The softened and/or spaced clock signal transitions result in significantly reduced EMI and related noise.

Referring more specifically to the embodiment of Fig. 2, select/control lines 161-163 permit a user to selectively enable CMOS transistors 110,120,130. Each enabled CMOS transistor effectively functions as a voltage divider with the necessary resistive components being provided primarily by the surface area dependent resistance value of the gate(s). Accordingly, if the three CMOS transistors have the same size gates (i.e., the same resistive values), then a designer may select between three possible resistive values, those values provided by enable one, two or three of the transistors. Alternatively, the CMOS transistors may be configured such that one or more have differently sized gates. For example, if each of transistors 110,120,130 have a different sized gate, then a designer may select from amongst seven possible resistive

values for circuit 100. These include the following enabled CMOS transistor scenarios (which are followed by their selection signal as propagated on lines 161-163 in parentheses): 110 (101), 120 (010), 130 (001), 110+120
5 (110), 110+130 (101), 120+130 (011) and 110+120+130 (111).

It should also be recognized that while the present invention is shown in Figs. 2-3 in a CMOS embodiment, it may also be implemented in an NMOS or PMOS setting, either using selectable NMOS or PMOS transistors arranged
10 generally as discussed above or selectable NMOS or PMOS transistors in combination with resistors formed in the semiconductor material.

Referring to Fig. 3, a schematic block diagram of selection logic 231 for use in circuit 100 of Fig. 2 in
15 accordance with the present invention is shown. Logic 231 essentially takes the place of any or all of the AND gates of circuit 100. In Fig. 3, logic 231 is described as though it replaces gate 131, though it may understandably also replace gates 111,121.

20 Logic 231 provides an inverter 241, a NAND gate 242 and a NOR gate 243. The input clock signal on line 205 is propagated to the NAND and NOR gates. The select signal is propagated via line 263 to the NOR gate and through inverter 241 to the NAND gate. Logic 231 permits CMOS
25 transistor 230 (analogous to CMOS transistor 130) to be tri-stated such that a signal may be driven into the clock signal output 250.

While the invention has been described in connection with specific embodiments thereof, it will be understood
30 that it is capable of further modification, and this application is intended to cover any variations, uses, or adaptations of the invention following, in general, the principles of the invention and including such departures from the present disclosure as come within known or
35 customary practice in the art to which the invention

pertains and as may be applied to the essential features hereinbefore set forth, and as fall within the scope of the invention and the limits of the appended claims.

CLAIMS

1. A driver circuit (100), comprising:
a first MOS transistor (110) coupled between a
5 voltage supply and ground and having a first output;
a second MOS transistor (120) coupled between a
voltage supply and ground and having a second output,
said first output and said second output coupled together
to form a driver circuit output;
10 selection logic (111,121,231) coupled to said
first and second MOS transistors for selectably enabling
one or more of said transistors to produce an output
clock signal that transitions under the effects of a time
constant that includes a resistive component from said
15 selected one or more of said transistors.
2. The driver circuit of claim 1, wherein said
selection logic receives a clock signal (105), a first
transistor select signal (161) and a second transistor
20 select signal (162) and produces a first transistor
enable signal that is propagated to said first transistor
and a second transistor enable signal that is propagated
to said second transistor.
- 25 3. The driver circuit of claim 1, further
comprising control logic (70) coupled to said selection
logic (111,121,231) that produces said first transistor
select signal and said second transistor select signal.
- 30 4. The driver circuit of claim 1, wherein said

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first transistor (110) is present in a first transistor stage that includes a first PMOS transistor (112) and a first NMOS transistor (113), said first output being provided between said first PMOS and NMOS transistors.

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5. The driver circuit of claim 4, wherein said second transistor (120) is present in a second transistor stage that includes a second PMOS transistor (122) and a second NMOS transistor (123), said second output being
10 provided between said second PMOS and NMOS transistors.

6. The driver circuit of claim 5, further comprising a third transistor stage that includes a third PMOS transistor (132) and a third NMOS transistor
15 (133) and a third output provided between said PMOS and NMOS transistors and coupled to said first and second outputs.

7. The driver circuit of claim 1, wherein said
20 selection logic includes tri-state logic (231) for disabling one or more of said first and second transistors.

8. A clock signal driving apparatus (100),
25 comprising:
a clock signal input (9,105);
a clock signal buffer (21-24,31-36,41-46)
coupled to said clock signal input that buffers a clock
signal received from said input and produces a buffered
30 clock signal at an output thereof; and

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logic (70,111,121,231) that permits modification of the shape of the transitions of said buffered clock signal.

5 9. The apparatus of claim 8, wherein said buffer includes a selectable semiconductor resistive element (112,122).

10 10. The apparatus of claim 9, wherein said
10 selectable semiconductor resistive element is a MOS transistor (112,113,122,123) and said modification logic is capable of enabling or disabling said MOS transistor.

