PROCESS FOR FABRICATING A SUBSTRATE OF THE SILICON-ON-INSULATOR TYPE

Background of the invention

The present invention relates to the field of processes for fabricating what are called SOI (silicon on insulator) substrates.

Such an SOI substrate comprises a silicon dioxide (SiO_2) layer buried between a bulk silicon substrate and an active silicon layer.

These substrates are intended to be used in the fields of electronics, optics or optoelectronics.

The invention relates more particularly to the finishing steps of a process for fabricating SOI substrates, the thickness of the silicon active layer of which is less than 150 nanometers (150 nm).

Description of the prior art

An example of a process for fabricating an SOI substrate is already known from document US 2003/0181001.

That process involves simple implantation of hydrogen ions, or ions of another rare gas, into a surface-oxidized substrate so as to form therein a plane of weakness that forms the boundary between a surface layer and the remainder of the substrate. This substrate is then bonded to a support and then an annealing operation is carried out at temperatures between 400°C and 600°C so as to detach said surface active layer from this implanted substrate and transfer it onto the support.

To reduce the roughness of this active layer, a finishing annealing operation is then carried out in an atmosphere containing hydrogen, an inert gas or a mixture of the two gases, at a temperature between 1100°C and 1350°C.

The above document specifies that the aforementioned heat treatment may be carried out by a technique called "long annealing" for a time between 10 minutes and 8 hours, or by a technique known to those skilled in the art by the name RTA (rapid thermal annealing). In the latter case, this process is carried out in an RTA annealing apparatus that allows rates of temperature rise of greater than 10°C/s and relatively short annealing times, of around 30 seconds to 1 minute, to be achieved.

Finally, this annealing step is followed by a sacrificial oxidation step.

However, the process described in that document has several drawbacks, which will be explained below.

Annealing for several hours from the proposed temperature ranges, which may be up to 1350°C, results in at least partial dissolution of the buried silicon dioxide (SiO_2) layer, by diffusion of the oxygen forming the silicon dioxide and by evaporation of this oxygen at the surface of the active silicon layer. For high annealing temperatures, above about 1200°C, the dissolution phenomenon is also linked with the increase in solubility of oxygen in silicon and consequently its dissolution in the bulk substrate and the active silicon layer.

This effect is even more pronounced for silicon subsurface active layers with a thickness of 150 nanometers or less.

In addition, the diffusion of oxygen is not homogeneous through the active layer. Consequently, the SOI substrate obtained has a buried oxide layer of poorly controlled thickness, that is to say the thickness is both less than that normally expected in the absence of the aforementioned diffusion phenomenon and also not uniform over the entire surface of the substrate.

Tests have been carried out so as to measure these drawbacks.

The results are plotted in the appended figure 1, which shows on the y-axis the thickness $\mathbf{E_{SiO2}}$ of the buried silicon dioxide layer of an SOI substrate after thermal annealing and on the x-axis the average thickness $\mathbf{E_{Si}}$ of the active silicon layer before annealing. The thicknesses are expressed in nanometers.

Curves a, b and c represent the results obtained after annealing at temperatures of 1100°C, 1150°C and 1200°C, respectively.

Other complementary results are plotted in the appended figure 2, which represents on the y-axis the change in standard uniformity Δ_{SiO2} as a result of annealing this buried silicon dioxide layer and on the x-axis the thickness $\mathbf{E_{Si}}$ of the silicon active layer before annealing, expressed in nanometers.

Curves d, e and f represent the results obtained after annealing at temperatures of 1100°C, 1150°C and 1200°C, respectively.

An annealing operation at 1200°C for example is an operation during which the temperature gradually rises over several hours and is then held for 5 minutes at 1200°C.

As may be seen in figure 1, the higher the annealing temperature the smaller the thickness of the SiO_2 for a given thickness of the silicon active layer. Moreover, the smaller the thickness of the silicon active layer the greater is this effect, especially for annealing above 1100°C.

Thus, after annealing at 1200°C (see curve c) and for silicon active layer thicknesses greater than 200 nanometers, a reduction in the thickness of the SiO_2 of around 6 nanometers (compared with curve a) is observed and without the thickness uniformity of this layer being substantially degraded (see figure 2).

The term "thickness uniformity" denotes the maximum deviation in thickness of the buried SiO_2 layer within the SOI wafer. A uniformity of 1 to 1.5 nm for an SiO_2 layer with an average thickness of 145 nm is acceptable and commonplace. Moreover, the "change in thickness uniformity" on the final product corresponds to the change between the thickness uniformity values measured before and after the annealing, respectively.

The 0% value of the change in uniformity in figure 2 corresponds to the case in which there is no change in thickness uniformity. The uniformity remains the same as that of the SiO_2 layer before the annealing, that is to say of about 1 to 1.5 nm for an SiO_2 layer whose thickness before annealing was 145 nm.

However, for a silicon active layer with a thickness of 100 nanometers or less, the reduction in the thickness of the SiO_2 layer exceeds 10 nanometers (see figure 1) and the change in uniformity may be up to 500% of the initial uniformity value of 1 to 1.5 nm considered as being acceptable, as may be seen in curve f, that is to say this change may reach 5 to 7.5 nm.

Figure 2 also shows that this phenomenon, namely the loss of uniformity of the buried oxide thickness, is even greater for SOI substrates in which the silicon active surface layer is less than 60 nm.

In addition, it will be readily understood that this buried oxide dissolution phenomenon is more problematic the thinner the silicon dioxide (SiO_2) layer is.

Finally, the Applicant has found that such smoothing annealing carried out on a surface directly after it has been debonded is much less effective than annealing carried out after a prior thinning step. This constitutes a second drawback of the aforementioned process.

Also known, from document US 6 372 609, is a process for fabricating an SOI substrate that comprises steps of detaching and transferring a silicon layer that has been formed by the implantation of hydrogen ions.

According to the above process, the steps of finishing this substrate consist in carrying out, in succession, sacrificial oxidation, deoxidation of the sacrificial silicon layer and then heat treatment in a reducing atmosphere.

However, according to that document, the heat treatment in a reducing atmosphere is a treatment of the RTA (rapid thermal annealing) type carried out in a temperature range from 1000°C to 1300°C, for a very short time of 1 to 60 seconds.

However, in the case of rapid annealing, the oxide dissolution problem is not appreciable as the time during which the substrate is exposed to a high temperature is too short.

In addition, according to what was disclosed in that document, the rapid annealing treatment is applied to SOI substrates in which the silicon surface layer has a thickness of at least 230 nanometers. With such a relatively large thickness, and especially greater than 200 nanometers, the oxide dissolution problem does not arise.

Summary of the invention

The aim of the invention is to solve the aforementioned drawbacks of the prior art.

In particular, the subject of the invention is to provide a process for fabricating an SOI substrate in which the silicon surface layer has a thickness less than 150 nanometers and the buried oxide layer of which has the most uniform thickness possible and even more preferably this buried oxide layer is thin.

For this purpose, the invention relates to a process for fabricating a substrate of the SOI (silicon on insulator) type, comprising a silicon substrate covered with a silicon dioxide layer which is itself covered with what is called an "ultrathin" silicon layer, the thickness of said silicon layer being 150 nm or less, this process comprising the following steps:

- formation of a weakened zone within what is called a "donor" silicon substrate, this weakened zone forming therein the boundary between what is called a "thick" layer, the thickness of which is greater than 150 nm, and the remainder of the substrate;
- bonding of this donor substrate to what is called a "receiver" substrate, a silicon dioxide layer being interposed between the two;
- detachment from said remainder of the donor substrate, along the weakened zone, so as to obtain a semifinished SOI substrate comprising said silicon receiver substrate covered with said silicon dioxide layer, which is itself covered with said thick layer; and

- execution of finishing steps.

According to the invention, said finishing steps comprise the following successive steps:

a) thinning of said thick silicon layer so as to obtain what is called a "thin" silicon layer, the thickness of which is less than that of said thick layer but remains greater than 150 nm;

b) long annealing, in a gaseous atmosphere comprising hydrogen and/or argon, of said semifinished SOI substrate obtained from step a), and

c) thinning of said thin silicon layer so a to obtain said ultrathin silicon layer, the thickness of which is equal to 150 nm or less, and said finished substrate of the SOI (silicon on insulator) type.

According to other advantageous and nonlimiting features of the invention, taken individually or in combination:

- the long annealing is carried out in a temperature range from 950°C to 1350°C, preferably from 1100°C to 1250°C;
- the long annealing is carried out for a time of at least 10 minutes;
- the thinning of said thick silicon layer is carried out by sacrificial oxidation followed by deoxidation;
- the thinning of said thin silicon layer of step c) is carried out by chemical-mechanical polishing;
- the thinning of said thin silicon layer of step c) is carried out by sacrificial oxidation followed by deoxidation;
- said sacrificial oxidation is carried out under dry or wet conditions at a temperature between 700°C and 1100°C ;
- said weakened zone is formed by implantation of atomic or ionic species into said donor substrate;
- the process consists in forming the silicon dioxide layer by thermal oxidation of the donor substrate and/or of the receiver substrate and in bonding the two substrates to each other so that said silicon dioxide layer lies at the interface;
- said ultrathin silicon layer has, over its entire extent, an RMS surface roughness of less than 3 ångströms over a scanning area of 30 μm × 30 μm;
- the thickness of the buried silicon dioxide SiO_2 layer is 50 nanometers or less;
- the uniformity of the thickness of the buried silicon dioxide SiO_2 layer is equal to 1.8 nm or better; and

- the difference in uniformity of the thickness of the buried silicon dioxide (SiO_2) layer before and after the long smoothing annealing is less than 20%, preferably less than 10%.

Brief description of the drawings

Other features and advantages of the invention will become apparent from the description that will now be given, with reference to the appended drawings, which show, by way of indication but implying no limitation, one possible embodiment thereof.

In these drawings:

- figure 1 is a graph showing the thickness $\mathbf{E}_{SiO2}$ of the silicon dioxide layer of an SOI substrate after annealing as a function of the thickness $\mathbf{E}_{Si}$ of the silicon active layer before annealing, for heat treatments carried out at various temperatures and in accordance with the prior art;

- figure 2 is a graph showing the change in thickness uniformity Δ_{SiO2} as a result of the annealing of the silicon dioxide layer of an SOI substrate as a function of the thickness $\mathbf{E}_{Si}$ of the silicon active layer before annealing, for heat treatments carried out various temperatures and in accordance with the prior art;

- figures 3A to 3H are diagrams showing the various steps of the process according to the invention;

- figure 4 is a graph showing the values of the surface roughness **R** of two batches of SOI substrates obtained by a process of the prior art (A) and by the process according to the invention (B), respectively;

- figure 5 is a graph showing a parameter called "haze", meaning the "background noise", on the surface of two batches of SOI substrates obtained by a process of the prior art (A) and by the process according to the invention (B), respectively; and

- figure 6 is a graph showing the change in thickness uniformity Δ_{SiO2} for two batches of SOI substrates obtained by a process of the prior art (A) and by the process according to the invention (B), respectively.

Description of the preferred embodiments

This process will now be described in greater detail.

It comprises a first series of steps for the formation, detachment and transfer of a thin layer onto a donor substrate, illustrated in figures 3A to 3D, and a second series of steps for finishing, illustrated in figures 3E to 3H.

Figure 3A shows a donor substrate 1 made of preferably single-crystal silicon (Si) covered with a silicon dioxide (SiO_2) layer 2, the free surface of which bears the numerical reference 20.

The oxide layer 2 may result from thermal oxidation of the donor substrate 1 or may have been formed by deposition, conventionally by one of the chemical vapor deposition techniques known to those skilled in the art by the acronyms "CVD" (*Chemical Vapor Deposition*) and "LPCVD" (*Low Pressure Chimical Vapor Deposition*).

Figure 3A also shows a receiver substrate 3, made of single-crystal or polycrystalline silicon.

Figure 3B shows an alternative embodiment in which there is a weakened zone 10 within the donor substrate 1.

In this case, the donor substrate 1 is subjected to implantation of atomic or ionic species through the oxide layer 2.

The expression "implantation of atomic or ionic species" is understood to mean any bombardment by these species capable of introducing them into the donor substrate with a maximum concentration at a predetermined depth of the substrate with respect to the bombarded surface 20, for the purpose of creating therein said weakened zone 10. This type of implantation may be carried out for example using the process known by the name Smart-Cut®.

Further details concerning this process may be found in the document "*Silicon-on-insulator technology: materials to VLSI*", second edition, Jean-Pierre Colinge, Kluwer Academic Publishers, pages 50 and 51.

The weakened zone 10 forms the boundary between a layer 11 and the remainder 12 of the donor substrate 1.

The implantation of atomic or ionic species may be a single implantation, that is to say implantation of a single atomic species, such as for example an implantation of hydrogen, helium or another rare gas.

The implantation may also be a co-implantation of atomic or ionic species, that is to say successive implantation of at least two different species, such as for example co-implantation of hydrogen and helium.

The following implantation conditions may be used as an example:

- implantation of just hydrogen: the implantation dose is preferably between 4×10^{16} H^+/cm^2 and 7×10^{16} H^+/cm^2 and the implantation energy between 20 keV and 100 keV;

- co-implantation of helium and hydrogen: preferably, in the case of helium, the implantation dose is between 0.5×10^{16} He^+/cm^2 and 2×10^{16} He^+/cm^2 and the implantation energy between 20 keV and 100 keV, and in the case of hydrogen, the implantation dose is between 0.5×10^{16} H^+/cm^2 and 2×10^{16} H^+/cm^2 and the implantation energy between 20 keV and 100 keV.

In the case of co-implantation of hydrogen and helium, the helium is preferably implanted before the hydrogen.

This implantation or co-implantation is carried out so that the thickness of the layer 11 formed is at least 150 nm.

In the rest of the description and the claims, and for the purpose of simplification, this layer 11 is chosen to be referred to as "thick layer" even though it is simply of a thickness greater than 150 nm, as opposed to its state after subsequent thinning.

It would also be possible to produce the weakened zone 10 in the form of a porous zone, obtained by the process known to those skilled in the art as the ELTRAN process.

Figure 3C shows the step in which the receiver substrate 3 is brought into intimate contact via one of its faces, referenced 30, with the face 20 of the SiO_2 layer 2 of the donor substrate 1.

The bonding between the two substrates preferably, but not necessarily, takes place by molecular adhesion and the bonding interface bears the numerical reference 4.

Although this has not been shown in the figures, it would also be conceivable to form or deposit the SiO_2 layer 2 on the receiver substrate 3 and then to bond the assembly to a donor substrate 1 that has already undergone the implantation for forming the weakened zone 10. However, in this case, it would be preferable to form or deposit a protective insulation layer on the donor substrate 1 before carrying out the implantation, it being possible, optionally, for this protective layer to be removed before the bonding.

Figure 3D shows that the process then continues with the detachment of the remainder 12 of the donor substrate, along the weakened zone 10, so as to transfer the thick layer 11 onto the support substrate 3, more precisely onto the oxide layer 2.

Detachment may be accomplished by any appropriate technique known to those skilled in the art, for example by applying stresses of a thermal, mechanical or chemical origin.

Thus, a substrate of the SOI "semi-conductor on insulator" type, referenced 5, is obtained in the semifinished state.

The finishing steps will now be described.

According to the invention, these steps comprise at least:

- thinning of the thick layer 11 (for example by sacrificial oxidation followed by deoxidation); then
- long annealing in a gaseous atmosphere comprising hydrogen and/or argon; and
- thinning of the annealed thinned layer.

The sacrificial oxidation operation is carried out on the surface of the thick layer 11. This operation is made up of an oxidation step, shown in figure 3E, an optional heat treatment and then a deoxidation step shown in figure 3F.

The first step consisting of an oxidation is preferably carried out at a temperature between 700°C and 1100°C.

It may be carried out under dry conditions, for example by heating the SOI substrate in a gaseous atmosphere, or under wet conditions, for example by heating in an atmosphere containing water vapor.

Whether the oxidation is carried out under dry or wet conditions, the oxidation atmosphere may also be charged with hydrochloric acid.

The oxidation step results in the formation of a silicon dioxide (SiO_2) layer 111 on the surface of the thick silicon layer 11.

The optional heat treatment second step that follows may be carried out by increasing the temperature at a constant or varying rate until a temperature of above about 1000°C, and preferably between about 1100°C and 1200°C, is reached, in a nonoxidizing gaseous atmosphere. The gaseous atmosphere contains for example argon, nitrogen or other nonoxidizing gases, or a mixture of these gases. The heat treatment may also be carried out under a vacuum.

The duration of this heat treatment is typically about 2 hours.

It should be noted that this heat treatment may be carried out up to a temperature of 1200°C without any risk of the buried SiO_2 layer 2 dissolving, since the upper layer 110 of the silicon layer 11 is oxidized (reference 111), thereby preventing the phenomenon of transport to the surface and evaporation thereat.

Finally, the total deoxidation step shown in figure 3F allows the oxide layer 111 formed during the oxidation step to be removed. This step is for example carried out by immersing the SOI substrate for a few minutes in a solution of hydrofluoric acid (HF) diluted in water to 10 or 20% by volume, for example.

A few minutes of immersion of the substrate in this solution are sufficient for removing the silicon dioxide layer 111 formed beforehand, the thickness of which layer generally varies from about a hundred to a few hundred nanometers. This way, the thickness of silicon of the thick layer 11 that was damaged during detachment is removed.

Thus, the semifinished substrate 5' is obtained. The residual silicon layer bearing the numerical reference 112 is called hereafter "thin layer", as it is thinner than the thick layer 11.

Other techniques for thinning the thick layer 11 are also conceivable, such as for example dry etching or wet etching.

According to the invention, the thinning of the thick layer 11 is carried out so that said thin layer 112 still has a thickness of greater than 150 nm before the next step, thermal annealing, is carried out, this being shown in figure 3G.

This thermal annealing to smooth the SOI substrate is carried out in a gaseous atmosphere comprising hydrogen and/or argon, in the absence of oxygen, at a temperature between 950°C and 1350°C, preferably between 1000°C and 1250°C.

This annealing is called long annealing, that is to say the SOI substrate is held in the aforementioned temperature range for at least about 10 minutes and for a maximum time of a few hours, possibly even up to 8 hours. For a time of less than 10 minutes, the treatment is ineffective while for longer than 8 hours it is no longer economic in terms of production costs.

This annealing is carried out in a suitable furnace.

The finished SOI substrate obtained bears the reference 6.

The last step of the process, as shown in figure 3H, is an additional thinning of the thin silicon layer 112 which, once thinned, is called "ultrathin layer" and bears the reference 113.

The thinning is carried out so that the thickness of said ultrathin layer 113 is less than 150 nm.

The Applicant has carried out measurements and observed that by carrying out the finishing steps according to the invention it is possible,

surprisingly, to limit the roughness of the ultrathin layer 113 obtained and above all to considerably reduce the dissolution of the buried oxide (SiO_2) layer 2.

The results are plotted in figure 4, which shows, on the y-axis, the RMS roughness **R** of the silicon ultrathin layer 113 of various SOI substrates, expressed in ångstroms for a scanning area of 30 μm × 30 μm.

The aforementioned roughness is expressed by an RMS (*Root Mean Square*) value. It is measured by AFM (*Atomic Force Microscopy*), the tip of which scans an area expressed in square microns.

The measurements were made on the one hand on a first batch A of SOI substrates obtained by a process in which the finishing steps comprised only a long annealing operation, carried out immediately after the step of detaching and transferring the thick layer and, on the other hand, on a second batch B of SOI substrates obtained by a process in which the finishing steps were in accordance with the invention and included an oxidation step followed by a sacrificial deoxidation step before the detachment, and then a long annealing step.

By examining the results, it may be seen that the process according to the invention allows the roughness of the ultrathin layer 113 to be appreciably reduced. In addition, the RMS roughness values obtained are small, less than 5 or even 4 ångstroms for a scanning area of 30 μm × 30 μm, and are reproducible, as indicated by the low scatter in the values obtained for B.

Figure 5 illustrates the value of the mean haze, which is used to characterize the uniformity of the roughness over an entire area.

The measurements were carried out with batches A and B prepared as described above.

This haze value, measured in ppm, is obtained by a method using the optical reflectivity properties of the surface to be characterized, and corresponds to an optical "background noise" scattered by the surface, owing to its microroughness.

The haze value is correlated in particular with the roughness and the defectuosity of a surface. A low haze value H corresponds to a good surface finish.

The haze measurement is preferably carried out using an instrument of the Surfscan SP2 (registered trademark) type as sold by the company KLA TENCOR.

It may be seen in figure 5 that there is a substantial reduction in the average haze value H for the substrates of batch B.

Measurements were also made of the difference in thickness uniformity of the buried SiO_2 layer before and after the long annealing, this being shown in figure 3G.

The measurements were carried out on the batches of substrates A and B as defined above and the results are plotted in figure 6. The 0% change value corresponds to an SiO_2 thickness uniformity that is acceptable and commonplace (equivalent to the uniformity of the substrate before the long annealing), of around 1 to 1.5 nm, for an SiO_2 layer having an initial thickness of about 145 nm.

The results obtained for batch B show that, unlike batch A, the SiO_2 thickness uniformity on the product after annealing is close to the value of this uniformity before annealing. In addition, these good results are reproducible.

An illustrative example of the invention and a counter-example will be given below.

Example

A silicon donor substrate, covered with a 50 nanometer silicon dioxide layer, underwent a successive co-implantation of helium and then hydrogen with the parameters mentioned below:

- helium: dose = 1×10^{16} He^+/cm^2; energy = 50 keV;
- hydrogen: dose = 1×10^{16} H^+/cm^2 ; energy = 30 keV.

After said SiO_2 layer was bonded onto a silicon receiver substrate, the process of detaching and transferring the SiO_2 layer was carried out, resulting in a thick silicon layer with a thickness of about 200 nanometers.

This detachment step was carried out by annealing at a temperature of about 500°C.

The thick silicon layer then underwent a sacrificial oxidation step, that is to say dioxidation followed by deoxidation, so as to obtain on top of the buried silicon dioxide layer a thin silicon layer with a thickness of more than 150 nanometers.

Next, a thermal annealing operation was carried out for a time of 4 hours, at a temperature of 1200°C, in a gaseous atmosphere containing exclusively hydrogen and argon.

The RMS roughness of the surface of the thin silicon layer obtained was from 2 to 3 ångströms for an AFM scanning area of 30 μm × 30 μm.

Finally, an additional thinning step was carried out.

The thickness of the buried oxide (SiO_2) layer was around 50 nm and remained almost uniform over its entire surface. The measured thickness uniformity

of the final product was better than 1.8 nm, for an initial SiO_2 thickness of 50 nm, i.e. less than 20% greater than the acceptable and commonplace thickness uniformity mentioned in the introduction of the application.

Counter-example

A silicon donor substrate, covered with a 50 nanometer silicon dioxide layer, underwent a successive co-implantation of helium and hydrogen with the parameters mentioned below:

- helium: dose = 1×10^{16} He^+/cm^2; energy = 50 keV;
- hydrogen: dose = 1×10^{16} H^+/cm^2 ; energy = 30 keV.

After said SiO_2 layer was bonded onto a silicon receiver substrate, the process of detaching and transferring the SiO_2 layer was carried out, resulting in a thick silicon layer with a thickness of about 200 nanometers.

This detachment step was carried out by annealing at a temperature of about 500°C.

Next, a sacrificial oxidation step was carried out, but on a larger thickness, so as to obtain a thin silicon layer with a thickness of 100 nm.

Finally, the same thermal annealing operation as in the previous example was carried out.

This time it was found that the buried silicon dioxide (SiO_2) layer was no longer of uniform thickness. The measured thickness variations (i.e. the uniformity) reached 2.2 nm, which means that they were more than 50% higher than the aforementioned acceptable and commonplace thickness uniformity.

CLAIMS

1. A process for fabricating a substrate of the SOI (silicon on insulator) type, comprising a silicon substrate covered with a silicon dioxide layer which is itself covered with silicon layer called "ultrathin", the thickness of said silicon layer being 150 nm or less, this process comprising the following steps :

- formation of a weakened zone within a silicon substrate called a "donor substrate", this weakened zone forming therein the boundary between a layer called a "thick layer", the thickness of which is greater than 150 nm, and the remainder of the substrate;
- bonding of this donor substrate to a substrate called a "receiver substrate", a silicon dioxide layer being interposed between the two;

detachment from said remainder of the donor substrate, along the weakened zone, so as to obtain a semifinished SOI substrate comprising said silicon receiver substrate covered with said silicon dioxide layer, which is itself covered with said thick layer; and

- execution of finishing steps,

in which process said finishing steps comprise the following successive steps:

a) thinning of said thick silicon layer so as to obtain a silicon layer called "thin", the thickness of which is less than that of said thick layer but remains greater than 150 nm;

b) long annealing, in a gaseous atmosphere comprising hydrogen and/or argon, of said semifinished SOI substrate obtained from step a), and

c) thinning of said thin silicon layer so as to obtain said ultrathin silicon layer, the thickness of which is 150 nm or less, and said finished substrate of the SOI (silicon on insulator) type.

2. The process as claimed in claim 1, wherein the long annealing is carried out in a temperature range from 950°C to 1350°C.

3. The process as claimed in claim 2, wherein the long annealing is carried out in a temperature range from 1100° to 1250°C.

4. The process as claimed in one of the preceding claims, characterized in that the long annealing is carried out for a time of at least 10 minutes.

5. The process as claimed in one of the preceding claims, characterized in that the thinning of said thick silicon layer is carried out by sacrificial oxidation followed by deoxidization.

6. The process as claimed in one of the preceding claims, characterized in that the thinning of said thin silicon layer of step c) is carried out by chemical-mechanical polishing.

7. The process as claimed in one of the preceding claims, characterized in that the thinning of said thin silicon layer of step c) is carried out by sacrificial oxidation followed by deoxidization.

8. The process as claimed in claim 5 or 7, characterized in that said sacrificial oxidation is carried out under dry or wet conditions, at a temperature between 700°C and 1100°C.

9. The process as claimed in one of the preceding claims, characterized in that said weakened zone is formed by implanting atomic or ionic species in said donor substrate.

10. The process as claimed in one of the preceding claims, which consists in forming the silicon dioxide layer by thermal oxidation of the donor substrate and/or of the receiver substrate and in bonding the two substrates to each other so that said silicon dioxide layer lies at the interface.

11. The process as claimed in one of the preceding claims, wherein said ultrathin silicon layer has, over its entire extent, an RMS surface roughness of less than 3 ångströms over a scanning area of 30 μm × 30 μm.

12. The process as claimed in one of the preceding claims, characterized in that the thickness of the buried silicon dioxide (SiO_2) layer is 50 nanometers or less.

13. The process as claimed in one of the preceding claims, characterized in that the thickness uniformity of the buried silicon dioxide (SiO_2) layer is 1.8 nm or better.

14. The process as claimed in one of the preceding claims, characterized in that the difference in uniformity of the thickness of the buried silicon dioxide layer before and after the long smoothing annealing is less than 20%, preferably less than 10%.