ABSTRACT

STRUCTURE AND METHOD TO IMPLEMENT DUAL STRESSOR
LAYERS WITH IMPROVED SILICIDE CONTROL

An example embodiment for a method of fabrication of a semiconductor device comprises the following. We provide a substrate (10) with a first device region (12) and a second device region (14). We provide a first type FET transistor (48) in the first device region (12) and provide a second type FET transistor (46) in the second device region (14). We form an etch stop layer (65) over the first and second device regions (12, 14) and forming a first stressor layer (66) over the first device region (12). The first stressor layer (66) puts a first type stress on the substrate (10) in the first device region (12). We form a second stressor layer (71) over the second device region (14). The second stressor layer (71) puts a second type stress on the substrate (10) in the second device region (14). Another example embodiment is the structure of a dual stress layer device having an etch stop layer.

Fig. 4.

162162

G00002