Semiconductor Processing Methods, And Semiconductor Constructions

TECHNICAL FIELD

[0001] The invention pertains to semiconductor processing methods, and to semiconductor constructions.

BACKGROUND OF THE INVENTION

[0002] As the level of integration of integrated circuitry increases, it is becoming an ever greater challenge to maintain electrical isolation between adjacent electrical devices. For instance, the density of dynamic random access memory (DRAM) has been approximately quadrupled every three years by virtue of advances in DRAM technology. As the device dimensions scale down, it is becoming more and more challenging to maintain electrical isolation (especially cell-to-cell isolation) in the memory array region due to reduction of space for isolation structures. A common isolation structure is a trenched isolation structure (such as, for example, a shallow trench isolation structure), and it is becoming increasingly challenging to form and fill the trenches of such isolation structures within the ever-decreasing real estate available for the structures.

[0003] Cell-to-cell isolation is becoming a greater factor in causing failure of integrated circuitry, with such failure frequently being due to leakage around a trenched isolation region. Field implants have been utilized in an attempt to prevent leakage around trenched isolation structures, but such can create problems with refresh.

[0004] Cell-to-cell isolation is already problematically challenging, and is expected to become even more challenging for future generations of devices due to the tighter pitch and smaller space available for isolation structures of the future. Accordingly, it is desirable to develop new isolation structures. It would be particularly desirable for such isolation structures to be suitable for cell-to-cell isolation.

SUMMARY OF THE INVENTION

[0005] In one aspect, the invention includes a semiconductor processing method. A semiconductor material is provided, and an opening is formed to extend into the semiconductor material. An upper periphery of the opening is provided with a liner while at least a portion of a lower periphery of the opening is unlined. Etching is

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conducted through the unlined portion to form a bulbous extension of the opening, and such bulbous extension is substantially filled with insulative material.

[0006] In one aspect, the invention encompasses a semiconductor processing method. A semiconductor material is provided and an opening is formed to extend into the semiconductor material to a first depth. A periphery of the opening is lined with a protective liner, except for the lower region of the opening. Etching is conducted through the unlined lower region of the opening with an etch that is at least substantially isotropic to form a widened extension of the opening.

[0007] In one aspect, the invention encompasses a semiconductor processing method. A silicon-containing material is provided. An opening is formed to extend into the silicon-containing material. The opening has a bulbous bottom region and a stem region extending upwardly from the bottom region to a surface of the silicon-containing material. The opening is substantially filled with insulative material. A first transistor device is formed on one side of the opening, with the first transistor device having a pair of first source/drain regions extending into the silicon-containing material. A second transistor device is formed on an opposing side of the opening from the first transistor device, with the second transistor device having a pair of second source/drain regions extending into the silicon-containing material. The insulative material within the opening is utilized to provide electrical isolation between the first and second transistor devices.

[0008] In one aspect, the invention includes a semiconductor construction. The construction comprises a semiconductor material and an electrically insulative structure extending into the semiconductor material. The electrically insulative structure has a bulbous bottom region and a stem extending upwardly from the bottom region to a surface of the semiconductor material. The construction can further include a first transistor device on one side of the electrically insulative structure and a second transistor device on an opposing side of the electrically insulative structure, with the insulative material of the insulative structure providing electrical isolation between the first and second transistor devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

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[0010] Fig. 1 is a diagrammatic, cross-sectional view of a semiconductor wafer fragment at a preliminary processing stage of an exemplary aspect of the present invention.

[0011] Fig. 2 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 1.

[0012] Fig. 3 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 2.

[0013] Fig. 4 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 3.

[0014] Fig. 5 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 4.

[0015] Fig. 6 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 5.

[0016] Fig. 7 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 6.

[0017] Fig. 8 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 7.

[0018] Fig. 9 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 8.

[0019] Fig. 10 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 9.

[0020] Fig. 11 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 9 in accordance with an aspect alternative to that of Fig. 10.

[0021] Fig. 12 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 4 in accordance with an aspect of the invention alternative to that of Fig. 5.

[0022] Fig. 13 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 12.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0023] The invention includes processes in which bottom regions of openings or trenches are expanded. In particular aspects, the openings having expanded bottom regions are filled with insulative material to create trenched isolation structures. Such

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isolation structures can provide improvements relative to prior art isolation structures for cell-to-cell isolation in a memory array. Some specific applications of the invention utilize isolation structures formed in accordance with the invention to improve refresh and functionality of devices associated with a memory array relative to the refresh and functionality that would occur in prior art constructions. In some aspects of the invention, the expanded bowl (i.e., expanded bottom region) of an isolation region formed in accordance with the invention is kept relatively far away from channel regions of access devices so that operating parameters of the devices (for example, channel length and drive current) are not adversely impacted by the utilization of the isolation region of the present invention.

[0024] A particular aspect of the invention is described with reference to Figs. 1-10.

[0025] Referring to Fig. 1, a semiconductor construction 10 is illustrated at a preliminary processing stage. Construction 10 comprises a substrate 12. The substrate can comprise, consist essentially of, or consist of monocrystalline silicon lightly doped with suitable background dopant, and in particular aspects can comprise, consist essentially of, or consist of monocrystalline silicon lightly background doped with p-type dopant. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

[0026] Although silicon is one exemplary semiconductor material that can be incorporated into substrate 12, it is to be understood that the substrate can comprise other semiconductor materials, including, for example, germanium.

[0027] A layer 14 comprising, consisting essentially of, or consisting of silicon dioxide is formed over substrate 12; and a layer 16 comprising, consisting essentially of, or consisting of silicon nitride is formed over layer 14. The layers 14 and 16 are together patterned to form a hard mask over substrate 12. The patterned hard mask has an opening 18 extending therethrough to an upper surface of substrate 12. Layers 14 and 16 can be patterned through any suitable processing, including, for example, forming photolithographically patterned photoresist over layer 16, transferring a pattern

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from the photoresist to the underlying layers 14 and 16, and subsequently removing the photoresist.

[0028] Referring to Fig. 2, opening 18 is extended into semiconductor material of substrate 12. The opening is extended with a suitable anisotropic etch, and can be extended to any suitable depth within the substrate. For instance, if opening 18 is ultimately to be used in forming a trenched isolation region, the opening can be extended to a depth approximately equal to that conventionally utilized for trenched isolation regions. The opening can have any suitable shape, and in particular aspects can be a trench extending longitudinally into and out of the page relative to the cross-sectional view of Fig. 2.

[0029] The opening 18 has a maximum cross-sectional width 19 extending transversely across the opening at a widest portion of the opening within substrate 12. Such width can be any suitable width, and in particular aspects will be a width of less than or equal to about 100 nanometers.

[0030] Referring next to Fig. 3, a liner 20 is formed along a periphery of opening 18. The shown liner extends only along semiconductor material substrate 12, and not along masking materials 14 and 16. However, it is to be understood that the invention also encompasses some aspects (not shown) in which the liner extends along exposed surfaces of layers 14 and 16, as well as along exposed surfaces of semiconductor material substrate 12.

[0031] Liner 20 can comprise any material suitable for protecting surfaces of substrate 12 during a subsequent etch (discussed below). For instance, liner 20 can comprise, consist essentially of, or consist of silicon dioxide. In such aspects, the liner can be formed by depositing silicon dioxide within the opening, and/or can be formed by thermal oxidation of exposed surfaces of a silicon-containing substrate 12 within the opening. If substrate 12 comprises semiconductor materials other than silicon, the oxide formed within the opening as liner 20 can be an oxide other than silicon dioxide. The oxidation utilized to form liner 20 can, for example, comprise oxidation with an O_2 plasma, either *in situ* or *ex situ*, and in some aspects chlorine can also be incorporated into the oxidation chemistry.

[0032] In some aspects of the invention, liner 20 can comprise, consist essentially of, or consist of a polymeric organic material (or, in other words, an organic polymer). For instance, the liner can comprise, consist essentially of, or consist of a combination of carbon, hydrogen and fluorine. In such aspects, the polymer can be

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formed from one or more of CHF_3, CH_2F_2, CH_3F, CF_4, CH_4, C_2H_6, C_2H_4, NH_3, and HBr. If the liner comprises an organic polymer, such can be directly on semiconductor material of substrate 12 (as shown), or can be over an intervening layer, such as, for example, a thin layer of native oxide.

[0033] The deposition conditions utilized for forming liner 20 can comprise moderate to high pressure, and low bias voltage to uniformly deposit the liner within opening 18. If the liner comprises a polymeric organic material, the liner can be deposited over exposed surfaces of layers 14 and 16 in addition to being deposited along exposed surfaces of semiconductor material substrate 12 within opening 18.

[0034] Referring next to Fig. 4, liner 20 is subjected to an anisotropic etch which removes the liner from along a lower region of opening 18 while leaving the liner along an upper region of the opening. The liner 20 appears to be broken into two separate segments in the shown cross-sectional view of Fig. 4. It is to be understood, however, that opening 18 can have a continuous sidewall if viewed from above, and that liner 20 can thus extend all the way around a lateral periphery of the sidewall at the processing stage of Fig. 4.

[0035] In some aspects, opening 18 can be considered to have an upper periphery and a lower periphery, with the lower periphery including, but not being limited to, a bottom-most portion of the opening. The shown etch has removed the liner from over the bottom-most portion of the opening, and not removed liner from regions above the bottom-most portion. The delineation between the upper periphery of the opening and the lower periphery of the opening can occur at any location within the opening, with the general understanding being that the liner remaining at the processing stage of Fig. 4 protects an entirety of the upper periphery of the opening, and that at least a portion of the lower periphery of the opening is unlined. The unlined portion of the lower periphery can be the bottom-most portion of the lower periphery, can be a region proximate the bottom-most portion of the lower periphery, or can be some combination of the bottom-most portion of the opening and a region proximate the bottom-most portion of the opening.

[0036] The etch chemistry utilized to remove liner 20 from the lower periphery of the opening can be any suitable etch chemistry. For instance, if liner 20 comprises, consists essentially of, or consists of silicon dioxide or an organic polymer, the etch can utilize one or more of CF_4, CHF_3, CH_2F_2, HBr, and Cl_2; and would typically be conducted

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at low pressure and with a moderate to high bias. The bias can cause the etch to be highly anisotropic.

[0037] The construction of Fig. 4 can be considered to contain an opening 18 extending into semiconductor material of substrate 12, with an upper periphery of the opening protected by the liner 20 and at least a portion of a lower periphery of the opening being unlined. Alternatively, the unlined portion of the opening can be considered to be an unlined lower region of the opening, and the lined portion of the opening can be considered to be a lined upper region of the opening.

[0038] Referring next to Fig. 5, the liner 20 is utilized to protect sidewalls of opening 18 while the unlined portion of opening 18 is exposed to an etch. The etch is typically isotropic, substantially isotropic, or at least a transition etch between an anisotropic etch and an isotropic etch. The etch widens the lower portion of opening 18 to form a widened extension 30 of the opening. In the shown aspect of the invention, the widened extension 30 is a bulbous extension.

[0039] The etch utilized to form widened extension 30 can comprise any suitable etch chemistry, and in particular aspects will comprise substantially isotropic chemistry selective for semiconductor material of substrate 12 (such semiconductor material can be silicon, for example) relative to the silicon dioxide of layer 14, the silicon nitride of layer 16, and the material of liner 20. The etch chemistry can, for example, be based on NF_3 and/or SF_6, and can also include one or more of HBr, CHF_3, CH_2F_2 and O_2 as moderating agents (with such moderating agents being specifically included to suppress lateral etching so that the bowl 30 ends up being relatively circular in configuration rather than being overly-elongated in lateral directions). The etching can be accomplished utilizing either wet etch or dry etch processes.

[0040] Although the etching utilized to form the widened regions of the opening can be isotropic etching, it is to be understood that the etching would typically be substantially isotropic, rather than absolutely isotropic. In other words, the etch will typically have some minor anisotropic component either purposely or due to, for example, difficulties in creating an absolutely isotropic etch; but will be mostly isotropic. For purposes of interpreting this disclosure and the claims that follow, the phrase "at least substantially isotropic" is to be understood to comprise substantially isotropic conditions and absolutely isotropic conditions.

[0041] The cross-sectional configuration of Fig. 5 can be considered to comprise an opening 18 having a configuration of a narrow stem region 34 extending upwardly

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from a widened bottom region 30. The shown widened region 30 has relatively sharp corners 32 where the widened regions joins with the narrow region of the opening. The sharpness of the corners 32 can be modified by coupling an anisotropic first etch with an isotropic second etch during formation of widened region 30, as will be discussed in more detail with reference to Figs. 12 and 13 below. It is to be understood that the opening 18 can be in the shape of a trench extending longitudinally into and out of the page relative to the shown cross-sectional view of Fig. 5.

[0042] Referring to Fig. 6, liner 20 (Fig. 5) is removed from within the stem region 34 of opening 18. Such removal can be accomplished with any suitable etch chemistry.

[0043] The opening 18 of Fig. 6 can have any suitable dimensions. In some aspects, the stem region can have a maximum cross-sectional width 19 of less than about 100 nanometers, and in particular aspects will have a maximum cross-sectional width of from about 50 nanometers to about 100 nanometers. The widened region 30 can have a maximum cross-sectional width 36 that is at least 10 nanometers greater than the width 19, and in particular aspects can be from about 20 nanometers greater to about 80 nanometers greater than the width 19 in the shown cross-sectional view (in other words, can extend from about 10 nanometers to about 40 nanometers laterally outward on either side of the original most-laterally-outward sidewall edges of opening 18 in the shown cross-sectional view).

[0044] Referring to Fig. 7, opening 18 is filled with material 40. In particular aspects of the invention, opening 18 is ultimately utilized to form an electrical isolation region extending within substrate 12, and accordingly material 40 can correspond to an electrically insulative material. In such aspects, material 40 can comprise any suitable electrically insulative composition or combination of compositions, and can, for example, comprise, consist essentially of, or consist of silicon dioxide. Although the material 40 is shown filling an entirety of opening 18, it is to be understood that the invention encompasses other aspects (not shown) in which the material only fills a portion of opening 18. For instance, material 40 can substantially fill the bulbous extension 30 without entirely filling the rest of the opening, or can substantially fill the bulbous region 30 and also substantially fill the stem region 34 extending upwardly from the bulbous region.

[0045] Although the shown aspect of the invention has the liner removed from within the stem region, it is to be understood that the invention also encompasses

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aspects in which the liner remains within the stem region as opening 18 is filled with various materials. For instance, if the liner comprises silicon dioxide, and the stem region is ultimately going to be filled with silicon dioxide to form an isolation region, the silicon dioxide of the liner can remain within the stem region. However, it can be advantageous to clean the liner from within the stem region in order to remove contaminating materials that may have accumulated on the liner during the processing of forming the opening 30, regardless of whether or not the liner otherwise comprises a composition suitable for incorporation into materials that are going to be utilized to fill the opening.

[0046] Referring next to Fig. 8, construction 10 is subjected to polishing (such as, for example, chemical-mechanical polishing) to form a planarized upper surface 41 extending across layer 16 and across an upper surface of insulative material 40. The planarization can stop at about an uppermost surface of layer 16, or in some aspects can extend into layer 16.

[0047] Referring to Fig. 9, layers 14 and 16 (Fig. 8) are removed. The structure comprising insulative material 40 can, in some aspects, be an isolation structure, and can be considered to correspond to a trenched isolation structure. Such isolation structure has, in the shown cross-sectional view, the widened base 30 (which can also be referred to as a bulbous region or bowl region) and the stem 34 extending upwardly from such base. Circuit devices can be provided on opposing sides of the isolation structure, and the structure can then be utilized to provide electrical separation between the devices.

[0048] Fig. 10 illustrates an exemplary construction utilizing the isolation structure of material 40 to provide electrical isolation between a first transistor device 50 and a second transistor device 60. The first transistor device is formed on one side of the isolation structure, and the second transistor device is formed on an opposing side of the isolation structure. The first transistor device comprises a transistor gate 52 comprising a gate dielectric material 54, a conductive gate material 56, and an insulative cap 58. The gate dielectric can, for example, comprise, consist essentially of, or consist of silicon dioxide. The conductive gate material can comprise any suitable electrically conductive composition or combination of compositions, and in particular aspects will comprise one or more of various metals, metal compositions, and conductively-doped semiconductor material (such as, for example, conductively-doped silicon). Electrically insulative cap 58 can comprise any suitable electrically insulative composition or

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combination of compositions, and in particular aspects will comprise one or both of silicon nitride and silicon dioxide.

[0049] A pair of source/drain regions 57 are proximate gate 52, and are electrically coupled to one another through a channel region beneath gate 52 and controlled by gate 52. Source/drain regions 57 comprise conductively-doped diffusion regions extending into substrate 12, and can comprise one or both of p-type dopant and n-type dopant. The shown source/drain regions 57 comprise lightly-doped extensions 59 and heavily-doped regions 55, as will be recognized by persons of ordinary skill in the art.

[0050] Transistor device 50 is shown to comprise sidewall spacers 53 beside the gate 52. Such sidewall spacers can comprise any suitable composition or combination of compositions, and in particular aspects will comprise, consist essentially of, or consist of one or both of silicon nitride and silicon dioxide.

[0051] Transistor device 60 comprises a gate 62 containing gate dielectric 64, conductive gate material 66, and an insulative cap 68. The gate dielectric 64, conductive gate material 66 and insulative cap 68 can comprise the same compositions as discussed above for gate dielectric 54, conductive gate material 56, and insulative cap 58. Transistor device 60 also comprises source/drain diffusion regions 67 extending into substrate 12, and having lightly-doped extensions 69 and heavily-doped regions 65. In some aspects, source/drain regions 57 can be referred to as first source/drain regions, and source/drain region 67 can be referred to as second source/drain regions.

[0052] The second transistor device 60 comprises sidewall spacers 63 which are analogous to the sidewall spacers 53, and which can comprise the same compositions discussed previously for sidewall spacers 53.

[0053] The cross-sectional view of the construction of Fig. 10 has the source/drain regions 57 and 67 entirely above bulbous region 30, and spaced from bulbous region 30 by gaps 70 between the source/drain regions and the bulbous region. In some aspects of the invention, it can be advantageous to form isolation structure 40 with the bulbous region more shallow than that of Fig. 10 so that source/drain regions of adjacent transistor devices extend to the bulbous region. For instance, Fig. 11 shows a structure similar to Fig. 10, but with the source/drain regions of transistor devices 50 and 60 extending to bulbous region 30 of the isolation structure. The structures of Fig. 11 are labeled identically to the structures of Fig. 10.

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[0054] It can be advantageous to form the source/drain regions of adjacent transistor devices to extend down to the bulbous region 30 of isolation structure 40 to remove a source of junction leakage. Alternatively, it can be advantageous to form structures of the type shown in Fig. 10 where the source/drain regions are well above the bulbous region 30 of isolation structure 40 so that the bulbous region does not impact performance of adjacent transistor devices other than providing better electrical isolation between the devices than can be achieved with prior art isolation regions.

[0055] Although the isolation regions of Figs. 10 and 11 have the stem 34 extending upwardly above an uppermost surface of substrate 12, it is to be understood that the invention encompasses other aspects (not shown) in which the stem is further polished after removal of layers 14 and 16 (Fig. 8) so that the stem has an uppermost surface which is approximately coplanar with an uppermost surface of substrate 12.

[0056] The aspect of the invention discussed above with reference to Fig. 5 pertained to an embodiment of the invention in which an isotropic etch was conducted immediately after removing the liner from along a bottom portion of the opening 18 of Fig. 4. Another aspect of the invention comprises a first anisotropic etch through the unlined portion of the opening followed by the isotropic etch. Utilization of the first anisotropic etch can enable the corners adjacent the bulbous region (such as, for example, the corners 32 shown in Fig. 5) to have controlled sharpness. The aspect of utilizing the anisotropic etch/isotropic etch combination to control corner sharpness is described with reference to Figs. 12 and 13.

[0057] Referring initially to Fig. 12, construction 10 is shown at a processing stage subsequent to that of Fig. 4. Identical numbering is utilized in describing Fig. 12 as was used above in describing the embodiment of Fig. 4. Thus, the construction 10 is shown to comprise the layers 16 and 14 over substrate 12, and is shown to have the opening 18 extending into substrate 12. The processing stage of Fig. 12 has opening 18 extended to a greater depth than the opening is at the processing stage of Fig. 4 due to utilization of an anisotropic etch to extend the opening through the unlined portion of Fig. 4.

[0058] Referring to Fig. 13, an isotropic etch is subsequently utilized to form the bowl region 30 of opening 18. The aspect of Fig. 13 has smoother corners 32 where the bowl region meets the stem region 34 than did the aspect of Fig. 5. In some applications of the invention, NF_3 and HBr are utilized for the isotropic etching of Fig. 13 as well as for the anisotropic etching of Fig. 12, and the amount of downward direction

of the etch relative to sideward direction of the etch is controlled by the ratio of NF_3 to HBr. An isotropic etch will typically etch about 70% downward relative to the amount that it etches laterally, and an etch which does greater than 70% downward relative to the amount that it etches laterally is typically considered to be an anisotropic etch.

[0059] The smoothness of the transition between the bulbous region 30 and the stem region 34 of opening 18 of Fig. 13 can improve characteristics of an isolation structure formed within the opening relative to the embodiment of Fig. 5. In some aspects, the transition between the stem region and widened region 30 can be smoothed by thermal oxidation utilized during formation of insulative material within opening 18 in addition to, or alternatively to, utilization of the anisotropic etch through the unlined portion prior to the isotropic etch.

[0060] The various aspects to the invention discussed above with reference to Figs. 1-13 can be utilized for numerous applications. In some applications, the invention can be utilized for forming new trenched isolation structures (for example, shallow trenched isolation structures) for improving cell-to-cell isolation in memory arrays (for example, dynamic random access memory arrays). The invention incorporates a relatively minor change in standard trench isolation processes, and accordingly can be economically incorporated into conventional processes. By adjusting the isolation region depth, and by adjusting the size of the bowl formed at the bottom of the isolation region, cell side junction leakage can be reduced by shutting down part of a junction leakage path, which can help data retention. The structures of the present invention can be applicable for current and future DRAM generations, and can be incorporated into processing without adding new masks or complicated new processing levels.

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CLAIMS

The invention claimed is:

1. A semiconductor processing method, comprising:

providing a semiconductor material;

forming an opening extending into the semiconductor material;

protecting an upper periphery of the opening with a liner while leaving at least a portion of a lower periphery of the opening unlined;

while protecting the upper periphery, etching through the unlined portion to form a bulbous extension of the opening; and

substantially filling the bulbous extension with insulative material.

2. The method of claim 1 wherein the semiconductor material comprises silicon.

3. The method of claim 1 wherein the liner comprises carbon, hydrogen and fluorine.

4. The method of claim 1 wherein the liner comprises an oxide.

5. The method of claim 4 wherein the liner is formed by oxidation of the semiconductor material along the periphery of the opening.

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6. The method of claim 1 wherein the liner is formed by:

forming liner material over an entirety of both the lower periphery and the upper periphery of the opening; and

anisotropically etching the liner material to remove the liner material from said at least a portion of the lower periphery while leaving the liner material along said upper periphery of the opening as the liner protecting said upper periphery of the opening.

7. The method of claim 1 wherein the unlined portion of the opening include an entirety of a bottom of the opening.

8. The method of claim 1 wherein the etching utilizes an etch that is at least substantially isotropic.

9. The method of claim 1 wherein the etching utilizes an etch that is anisotropic, followed by an etch that is at least substantially isotropic.

10. A semiconductor processing method, comprising:

providing a semiconductor material;

forming an opening extending into the semiconductor material to a first depth;

lining a periphery of the opening with a liner comprising an organic polymer;

removing the liner from a lower region of the opening while leaving the liner along an upper region of the opening; and

etching through the unlined lower region of the opening with an etch that is at least substantially isotropic to form a widened extension of the opening.

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11. The method of claim 10 wherein the semiconductor material consists essentially of silicon.

12. The method of claim 10 wherein the removing the liner from the lower region of the opening comprises anisotropically etching the liner.

13. The method of claim 10 further comprising first etching through the unlined lower region of the opening with an etch that is anisotropic, and then etching through the unlined lower region of the opening with the etch that is at least substantially isotropic.

14. The method of claim 10 further comprising, after the etching, removing the polymeric organic lining and subsequently filling the opening with dielectric material.

15. The method of claim 10 wherein the polymeric organic lining comprises carbon, hydrogen and fluorine.

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16. A semiconductor processing method, comprising:

providing a silicon-containing material;

forming an opening extending into the silicon-containing material, the opening having a bulbous bottom region and a stem region extending upwardly from the bottom region to a surface of the silicon-containing material;

substantially filling the opening with insulative material;

forming a first transistor device on one side of the opening, the first transistor device having a pair of first source/drain regions extending into the silicon-containing material;

forming a second transistor device on an opposing side of the opening from the first transistor device, the second transistor device having a pair of second source/drain regions extending into the silicon-containing material; and

utilizing the insulative material within the opening to provide electrical isolation between the first and second transistor devices.

17. The method of claim 16 wherein the forming the opening comprises:

forming the stem region extending into the silicon-containing material;

forming a protective layer along sidewalls of the stem region; and

while the protective layer is along the sidewalls, forming the bulbous bottom region of the opening with an etch that is at least substantially isotropic.

18. The method of claim 17 wherein the protective layer comprises silicon dioxide.

19. The method of claim 17 wherein the protective layer comprises a polymeric organic material.

20. The method of claim 16 further comprising removing the protective layer prior to substantially filling the opening with the insulative material.

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21. The method of claim 16 wherein the protective layer remains within the opening as the opening is substantially filled with the insulative material.

22. The method of claim 16 wherein at least one of the first and second transistor devices is formed after the opening is substantially filled with the insulative material.

23. The method of claim 16 wherein the insulative material consists essentially of silicon dioxide.

24. The method of claim 16 wherein one of the first source/drain regions extends to the bulbous bottom region.

25. The method of claim 24 wherein one of the second source/drain regions extends to the bulbous bottom region.

26. The method of claim 16 wherein the first and second source/drain regions are entirely above the bulbous bottom region.

27. A semiconductor construction, comprising:

a semiconductor material; and

an electrically insulative material structure extending into the semiconductor material, the structure having a bulbous bottom region and a stem region extending upwardly from the bottom region to a surface of the semiconductor material.

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28. The construction of claim 27 wherein the semiconductor material comprises silicon.

29. The construction of claim 27 wherein the semiconductor material consists essentially of silicon.

30. The construction of claim 29 wherein the insulative material consists essentially of silicon dioxide.

31. The construction of claim 27 further comprising:

a first transistor device on one side of the electrically insulative structure, the first transistor device having a pair of first source/drain regions extending into the semiconductor material;

a second transistor device on an opposing side of the electrically insulative structure from the first transistor device, the second transistor device having a pair of second source/drain regions extending into the semiconductor material; and

the insulative material providing electrical isolation between the first and second transistor devices.

32. The construction of claim 31 wherein one of the first source/drain regions extends to the bulbous bottom region.

33. The construction of claim 32 wherein one of the second source/drain regions extends to the bulbous bottom region.

34. The construction of claim 31 wherein the first and second source/drain regions are entirely above the bulbous bottom region.