

A CMOS Device on Ultrathin SOI with a Deposited Raised Source/Drain, and a Method of Manufacture

ABSTRACT

A structure for a CMOS device comprises a silicon over insulator (SOI) wafer (20) over a buried oxide (BOX) substrate (10); a gate dielectric (25) over the SOI wafer (20); a shallow trench isolation (STI) region (35) over the BOX substrate (10) having a generally rounded corner; a gate structure (40) over the gate dielectric (25); an implant layer (50) over the SOI wafer (20); N-type (51) and P-type (52) dopant implantations in the SOI wafer (20) and the implant layer (50); source and drain regions (79a, 79b) from the implant layer (50) and the SOI wafer (20) having a thickness greater than the predetermined thickness of the SOI wafer (20); and the gate dielectric (25) is positioned lower than the STI region (35). A method for forming the structure is also disclosed.

Fig 15A.



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