CLAIMS

1. A semiconductor packaging method, comprising:

forming an encapsulating structure, the encapsulating structure comprising an encapsulation layer and a chip, the chip provided on a front side thereof with a plurality of bonding pads, the encapsulation layer covering at least a side face of the chip;

forming a rewiring layer on a side of the encapsulating structure close to the front side of the chip, the rewiring layer configured for external connection of the bonding pads on the chip;

forming a dielectric layer, the dielectric layer covering the rewiring layer, the dielectric layer provided therein with a through hole in which the rewiring layer is exposed; and

forming a pin layer on a side of the dielectric layer away from the chip, the pin layer electrically connected to the rewiring layer through the through hole,

wherein the rewiring layer comprises a plurality of rewiring structures which are spaced apart from one another and provided with hollows to reduce a contact area of the rewiring layer with the dielectric layer and prevent separation of the rewiring structures from the dielectric layer.

2. The semiconductor packaging method according to claim 1, wherein the pin layer comprises a plurality of conductive pillars which are spaced apart from one another and raised from the dielectric layer, and wherein after the pin layer is formed on the side of the dielectric layer away from the chip, the semiconductor packaging method further comprises:

forming a solder layer, the solder layer covering a surface of the conductive pillars raised from the dielectric layer.

3. The semiconductor packaging method according to claim 1, wherein the

pin layer comprises a plurality of conductive pillars which are spaced apart from one another and raised from the dielectric layer, and a conductive feature is provided in the through hole so that the pin layer is electrically connected to the rewiring layer by the conductive feature, wherein a recess is formed in the conductive feature in positional correspondence with the through hole, and wherein after the pin layer is formed on the side of the dielectric layer away from the chip, the semiconductor packaging method further comprises:

forming a solder layer, the solder layer covering a surface of the conductive pillars raised from the dielectric layer, the solder layer filling the recess.

4. The semiconductor packaging method according to claim 3, wherein a width-to-depth ratio of the through hole is greater than or equal to 1/3.

5. The semiconductor packaging method according to claim 4, wherein a depth of the through hole ranges from 60 μm to 100 μm, and a thickness of the conductive feature at a bottom of the through hole ranges from 10 μm to 50 μm.

6. The semiconductor packaging method according to claim 1, wherein the pin layer has a thickness greater than 30 μm.

7. The semiconductor packaging method according to claim 1, further comprising: forming a heat dissipation layer on the side of the dielectric layer away from the chip; after which the semiconductor packaging method further comprises: forming a solder layer, the solder layer covering a surface of the heat dissipation layer exposed from the dielectric layer.

8. A semiconductor packaging structure, comprising:

an encapsulating structure, the encapsulating structure comprising an encapsulation layer and a chip, the chip provided on a front side thereof with a

plurality of bonding pads, the encapsulation layer covering a backside and a side face of the chip;

a rewiring layer located on a side of the encapsulating structure close to the front side of the chip, the rewiring layer configured for external connection of the bonding pads on the chip;

a dielectric layer covering the rewiring layer, the dielectric layer provided therein with a through hole in which the rewiring layer is exposed; and

a pin layer located on a side of the dielectric layer away from the chip, the pin layer electrically connected to the rewiring layer through the through hole,

wherein the rewiring layer comprises a plurality of rewiring structures which are spaced apart from one another and provided with hollows to reduce a contact area of the rewiring layer with the dielectric layer and prevent separation of the rewiring structures from the dielectric layer.

9. The semiconductor packaging structure according to claim 8, wherein the pin layer comprises a plurality of conductive pillars which are spaced apart from one another and raised from the dielectric layer, and wherein the semiconductor packaging structure further comprises a solder layer, the solder layer covering a surface of the conductive pillars raised from the dielectric layer.

10. The semiconductor packaging structure according to claim 8, wherein the pin layer comprises a plurality of conductive pillars which are spaced apart from one another and raised from the dielectric layer, and a conductive feature is provided in the through hole so that the pin layer is electrically connected to the rewiring layer by the conductive feature, wherein a recess is formed in the conductive feature in positional correspondence with the through hole, and wherein the semiconductor packaging structure further comprises a solder layer, the solder layer covering a surface of the conductive pillars raised from a surface of the dielectric layer, the solder layer filling the recess.

11. The semiconductor packaging structure according to claim 10, wherein a width-to-depth ratio of the through hole is greater than or equal to 1/3.

12. The semiconductor packaging structure according to claim 11, wherein a depth of the through hole ranges from 60 μm to 100 μm, and a thickness of the conductive feature at a bottom of the through hole ranges from 10 μm to 50 μm.

13. The semiconductor packaging structure according to claim 8, wherein the pin layer has a thickness greater than 30 μm.

14. The semiconductor packaging structure according to claim 8, further comprising:

a protective layer formed on the front side of the chip, wherein the protective layer comprises openings in which the plurality of bonding pads are exposed; and

conductive structures formed in the openings in the protective layer, wherein the rewiring structures are electrically connected to the bonding pads by the conductive structures.

15. The semiconductor packaging structure according to claim 14, further comprising:

a heat dissipation layer located on the side of the dielectric layer away from the chip, wherein the pin layer comprises a plurality of conductive pillars which are spaced apart from one another and located around the heat dissipation layer.