

MCM ENCAPSULATION STRUCTURE AND MANUFACTURING METHOD THEREFOR

TECHNICAL FIELD

The present application relates to the field of chip packaging technology and, in particular, to multi-chip module (MCM) packages and methods of manufacturing them.

BACKGROUND

A packaging process often involves packaging dies of different functions into a single package, forming a multi-chip module (MCM) for performing a given task, which provides advantages including a small size, high reliability, high performance and diverse functionality.

In view of the demand for increasingly miniaturized electronics with lighter weights, structurally compact small-size chip packages would become more and more popular in the marketplace.

An MCM often incorporates chips with complex internal circuits, necessitating high wiring density in a rewiring layer. Due to a very limited chip surface area, wiring is a difficult task. In addition, extremely dense wiring requires the use of fine wires, which are vulnerable to short circuits and unfavorable to product yield. Further, service lives of chips are typically limited. In particular, when multiple wiring layers are needed, such high process complexity will make the fabrication process less controllable.

SUMMARY

In a first aspect of the present application, there is provided an MCM package, including: a first die assembly including at least a first die and a second die, the first die including a number of first bond pads provided on an active surface of the first die, the second die including a number of second bond pads provided on an active surface of the second die, the active surface of the second die covered by a second protective

layer, the second bond pads exposed from the second protective layer, the active surface of the first die and the active surface of the second die facing opposite to each other; a wiring substrate surrounding the first die assembly, the wiring substrate provided therein with wiring lines, the wiring lines including front-side electrical connection points and back-side electrical connection points, the front-side electrical connection points exposed on a front side of the wiring substrate, the back-side electrical connection points exposed on a back side of the wiring substrate; a plastic encapsulation layer encapsulating the first die assembly and the wiring substrate, the second protective layer, the second bond pads and the back side of the wiring substrate exposed on a back side of the plastic encapsulation layer and that the active surface of the first die and the front side of the wiring substrate are exposed on a front side of the plastic encapsulation layer; first conductive traces provided on the first bond pads, the front-side electrical connection points and the front side of the plastic encapsulation layer to electrically connect the first die to the wiring lines; second conductive traces provided on the second bond pads, the back-side electrical connection points and the back side of the plastic encapsulation layer to electrically connect the second die to the wiring lines; conductive bumps connected to the first conductive traces; a first dielectric layer embedding the first conductive traces and the first conductive bumps, the first conductive bumps exposed from the first dielectric layer; and a second dielectric layer embedding the second conductive traces.

In a second aspect of the present application, there is provided a method of manufacturing an MCM package, including: providing a carrier board and multiple objects to be packaged carried on the carrier board, wherein each of the objects to be packaged includes: a wiring substrate with a through opening, the wiring substrate provided therein with wiring lines, the wiring lines including front-side electrical connection points and back-side electrical connection points, the front-side electrical connection points exposed on a front side of the wiring substrate, the back-side electrical connection points exposed on a back side of the wiring substrate; and a first die assembly provided in the through opening, the first die assembly including at least a first die and a second die, the first die including a number of first bond pads provided

on an active surface of the first die, the second die including a number of second bond pads provided on an active surface of the second die, the active surface of the second die covered by a second protective layer, the active surface of the first die and the active surface of the second die facing opposite to each other, the front side of the wiring substrate and the active surface of the first die facing the carrier board; forming on a surface of the carrier board a plastic encapsulation layer embedded the objects to be packaged; thinning the plastic encapsulation layer until the second protective layer and the back sides of the wiring substrates are exposed; forming in the second protective layer second openings in which the second bond pads are exposed; forming second conductive traces on the second protective layer, the second bond pads, the back-side electrical connection points and the back side of the plastic encapsulation layer, which electrically connect the second dies to the wiring lines; forming a second dielectric layer embedding the second conductive traces; removing the carrier board, exposing the active surfaces of the first dies, the front sides of the wiring substrates and the front side of the plastic encapsulation layer; forming first conductive traces on the first bond pads, the front-side electrical connection points and the front side of the plastic encapsulation layer, which electrically connect the first dies to the wiring lines; forming first conductive bumps on the first conductive traces and a first dielectric layer embedding the first conductive traces and the conductive bumps, the first conductive bumps exposed from the first dielectric layer; and forming a plurality of the MCM packages by dicing, each of which includes one of the objects to be packaged.

In a third aspect of the present application, there is provided an MCM package, including: a die including a number of bond pads provided on an active surface of the die; a wiring substrate surrounding the die, the wiring substrate provided therein with wiring lines, the wiring lines including front-side electrical connection points and back-side electrical connection points, the front-side electrical connection points exposed on a front side of the wiring substrate, the back-side electrical connection points exposed on a back side of the wiring substrate; a plastic encapsulation layer encapsulating the die and the wiring substrate, the active surface of the die and the

front-side electrical connection points exposed on a front side of the plastic encapsulation layer; conductive traces provided on the bond pads, the front-side electrical connection points and the front side of the plastic encapsulation layer to electrically connect the die to the wiring lines; conductive bumps connected to the back-side electrical connection points; a first dielectric layer embedding the conductive traces; and a second dielectric layer embedding the conductive bumps, the conductive bumps exposed from the second dielectric layer.

In a fourth aspect of the present application, there is provided a method of manufacturing a MCM package, including: providing a carrier board and multiple objects to be packaged carried on the carrier board, wherein each of the objects to be packaged includes a wiring substrate with a through opening and a die provided in the through opening, the wiring substrate provided therein with wiring lines, the wiring lines including front-side electrical connection points and back-side electrical connection points, the front-side electrical connection points exposed on a front side of the wiring substrate, the back-side electrical connection points exposed on a back side of the wiring substrate, the die including a number of bond pads provided on an active surface of the die, the front side of the wiring substrate and the active surface of the die facing the carrier board; forming on a surface of the carrier board a plastic encapsulation layer embedded the objects to be packaged; thinning the plastic encapsulation layer until the back sides of the wiring substrates are exposed; removing the carrier board, exposing the active surfaces of the dies, the front sides of the wiring substrates and the front side of the plastic encapsulation layer; forming conductive traces on the bond pads, the front-side electrical connection points and the front side of the plastic encapsulation layer, which electrically connect the dies to the wiring lines; forming a first dielectric layer embedding the conductive traces; forming conductive bumps on the back-side electrical connection points and a second dielectric layer embedding the conductive bumps, the conductive bumps exposed from the second dielectric layer; and forming a plurality of the MCM packages by dicing, each of which includes one of the objects to be packaged.

The present application provides the following benefits:

First, wiring layers required to be formed over the active surfaces of the dies can be provided in the wiring substrate, and multiple complex circuits in the wiring substrate can be electrically connected to the bond pads on the dies' active surface and thereby embedded in the package, enhancing overall performance of the package. Second, providing fine wires in the wiring substrate instead of in a rewiring layer can make them less vulnerable to short circuits and can thus result in an increase in product yield. Moreover, the first conductive traces and/or second conductive traces are allowed to be arranged in a reduced number of layers, reducing process complexity. Third, the wiring substrate is pre-formed and can be tested before packaging, avoiding it from being put into use while being defective. Fourth, the pre-formed wiring substrate is fabricated separately from the packaging process, resulting in overall time savings in the packaging process.

Further, the die assembly with the oppositely facing active surfaces enables the MCM package to have a small size and a compact structure. For the die assembly with the oppositely facing active surfaces, the wiring substrate enables not only electrical connection of the first die and the second die but also wiring on both the front side and the back side of the plastic encapsulation layer. Compared to wiring only on a single surface, this allows higher wiring density and enables the MCM package to have more complex wiring and an even smaller size.

The details of one or more embodiments of this application are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the application will be apparent from the description and drawings, and from the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic cross-sectional view showing the structure of a multi-chip module (MCM) package according to a first embodiment of the present application;

Fig. 2 is a flowchart of a method of manufacturing the MCM package of Fig. 1;

Figs. 3 to 9 are schematic illustrations of intermediate structures formed in the process of Fig. 2;

Fig. 10 is a flowchart of a method of manufacturing an MCM package according to a second embodiment of the present application;

Figs. 11 and 12 are schematic illustrations of intermediate structures formed in the method of Fig. 10;

Fig. 13 is a schematic cross-sectional view showing the structure of an MCM package according to a third embodiment of the present application;

Fig. 14 is a schematic cross-sectional view showing the structure of an MCM package according to a fourth embodiment of the present application; and

Fig. 15 is a schematic cross-sectional view showing the structure of an MCM package according to a fifth embodiment of the present application.

DETAILED DESCRIPTION

In order that the above objects, features and advantages of the present application become more apparent, particular embodiments of the application will be described in detail below with reference to the accompanying drawings.

Fig. 1 is a schematic cross-sectional view showing the structure of a multi-chip module (MCM) package according to a first embodiment of the present application.

Referring to Fig. 1, the MCM package 1 includes:

a first die assembly 10 including at least a first die 11 and a second die 12, wherein the first die 11 includes a number of first bond pads 111, the first bond pads 111 are disposed on an active surface 11a of the first die 11, the second die 12 includes a number of second bond pads 121, the second bond pads 121 are disposed on an active surface 12a of the second die 12, the active surface 12a of the second die 12 is covered by a second protective layer 120, the second bond pads 121 are exposed from the second protective layer 120, the active surface 11a of the first die 11 and the active surface 12a of the second die 12 face opposite directions;

a wiring substrate 13 surrounding the first die assembly 10, wherein the wiring substrate 13 contains wiring lines 130, the wiring lines 130 have front-side electrical connection points 131 and back-side electrical connection points 132, the front-side electrical connection points 131 are exposed on a front side 13a of the wiring substrate

13, the back-side electrical connection points 132 are exposed on a back side 13b of the wiring substrate 13;

a plastic encapsulation layer 14 encapsulating the first die assembly 10 and the wiring substrate 13, the plastic encapsulation layer 14 has a back side 14b on which the second protective layer 120, the second bond pads 121 and the back side 13b of the wiring substrate 13 are exposed, the plastic encapsulation layer 14 has a front side 14a on which the active surface 11a of the first die 11 and the front side 13a of the wiring substrate 13 are exposed;

first conductive traces 15 residing on the first bond pads 111, the front-side electrical connection points 131 and the front side 14a of the plastic encapsulation layer 14 and configured to electrically connect the first die 11 to the wiring lines 130;

second conductive traces 16 residing on the second bond pads 121, the back-side electrical connection points 132 and the back side 14b of the plastic encapsulation layer 14 and configured to electrically connect the second die 12 to the wiring lines 130;

conductive bumps 17 connected to the first conductive traces 15;

a first dielectric layer 18 embedding the first conductive traces 15 and the conductive bumps 17, with the conductive bumps 17 being exposed therefrom; and

a second dielectric layer 19 embedding the second conductive traces 16.

The first die 11 and the second die 12 may be dies in need of electrical interconnection and are each not limited to having any particular function. In some embodiments, the first die 11 and the second die 12 may be, for example, power dies, memory dies, sensor dies, radio-frequency (RF) dies or associated control chips.

Referring to Fig. 1, the first die 11 includes the active surface 11a and a back side 11b opposite thereto. The first bond pads 111 are exposed on the active surface 11a. The first die 11 may include various devices formed on a semiconductor substrate and electrical interconnects electrically connected to the devices. The first bond pads 111 are connected to the electrical interconnects and configured to input/output electrical signals to or from the individual devices. It is to be noted that, as used herein, “/” denotes “or”.

The second die 12 includes the active surface 12a and a back side 12b opposite thereto. The second bond pads 121 are exposed on the active surface 12a. The second die 12 may include various devices formed on a semiconductor substrate and electrical interconnects electrically connected to the devices. The second bond pads 121 are connected to the electrical interconnects and configured to input/output electrical signals to or from the individual devices.

With continued reference to Fig. 1, in this embodiment, the first die assembly 10 is a die stack structure in which the first die 11 and the second die 12 are arranged back-to-back. In the back-to-back arrangement of the first die 11 and second die 12, the first die 11 and the second die 12 are bonded together at the back side 11b and the back side 12b.

In other embodiments, the first die assembly 10 may include one or more first dies 11 and may include one or more second dies 12. The first die 11 and the second die 12 may be arranged in a staggered manner, or even side by side. In this case, the back side 12b of the second die 12 may be also exposed on the front side 14a of the plastic encapsulation layer 14.

In this embodiment, the first die 11 has a larger area than the second die 12. In other embodiments, the area of the second die 12 may be alternatively larger than that of the first die 11.

In this embodiment, a first protective layer 110 is provided on the active surface 11a of the first die 11. In other embodiments, the first protective layer 110 on the active surface 11a of the first die 11 may be omitted.

The first protective layer 110 and/or the second protective layer 120 may each be an insulating material such as an organic polymeric insulating material, an inorganic insulating material or a composite material. Examples of the organic polymeric insulating material may include, among others, polyimide, epoxy resins, Ajinomoto Buildup Films (ABF), polybenzoxazole (PBO), organic polymer films and other organic materials with similar insulating properties. The inorganic insulating material may be, for example, at least one of silicon dioxide and silicon nitride. The composite material is an inorganic-organic composite material. It may be an inorganic-organic

polymer composite material such as, for example, a SiO₂/resin/polymer composite material.

The wiring substrate 13 includes the wiring lines 130 and insulating material layers between the wiring lines 130. Compared to forming a rewiring layer on a plastic encapsulation body of the first die 11 and the second die 12, the wiring substrate 13 according to this embodiment has the following advantages. First, providing fine wires in the wiring substrate 13 instead of in the rewiring layer can make them less vulnerable to short circuits and can thus result in an increase in product yield. Moreover, the first conductive traces 15 and/or second conductive traces 16 are allowed to be arranged in a reduced number of layers, reducing process complexity. Second, the wiring substrate 13 is pre-formed and can be tested before packaging, avoiding it from being put into use while being defective. Third, the pre-formed wiring substrate 13 is fabricated separately from the packaging process, resulting in overall time savings in the packaging process.

Further, wiring layers required to be formed over the active surfaces 11a, 12a of the dies can be provided in the wiring substrate 13, and multiple complex circuits in the wiring substrate 13 can be electrically connected to the bond pads 111, 121 on the dies' active surface 11a, 12a and thereby embedded in the package 1, enhancing overall performance of the package 1.

The wiring substrate 13 may either be a monolithic substrate surrounding the first die assembly 10, or consisting of multiple portions. In the latter case, the individual portions of the wiring substrate 13 may be electrically connected to the first die 11 by the first conductive traces 15 and/or electrically connect to the second die 12 by the second conductive traces 16.

The wiring substrate 13 may include the front side 13a and the back side 13b, which oppose each other. In this embodiment, the front side 13a of the wiring substrate 13 is flush with the first protective layer 110, and the back side 13b of the wiring substrate 13 is flush with the second protective layer 120. There may be a plurality of front-side electrical connection points 131 exposed on the front side 13a of the wiring substrate and a plurality of back-side electrical connection points 132 exposed on the

back side 13b of the wiring substrate.

The plastic encapsulation layer 14 may be made of, for example, one or more of an epoxy resin, a polyimide resin, a benzocyclobutene resin, a polybenzoxazole resin, polybutylene terephthalate, polycarbonate, polyethylene terephthalate, polyethylene, polypropylene, polyolefin, polyurethane, polyolefin, polyethersulfone, polyamide, polyurethane, an ethylene-vinyl acetate copolymer, polyvinyl alcohol, etc. Alternatively, the plastic encapsulation layer 14 may be formed of any of various polymers or resin/polymer composite materials.

The plastic encapsulation layer 14 includes the front side 14a and the back side 14b, which oppose each other. In this embodiment, the first protective layer 110, the first bond pads 111 and the front side 13a of the wiring substrate 13 are exposed on the front side 14a of the plastic encapsulation layer 14, and the second protective layer 120, the second bond pads 121 and the back side 13b of the wiring substrate 13 are exposed on the back side 14b of the plastic encapsulation layer 14.

In the embodiment shown in Fig. 1, the first conductive traces 15 include a pattern of a number of metal blocks 15a. That is, the first conductive traces include a layer of metal blocks that form a pattern. Some of the metal blocks 15a are selectively electrically connected to some of the front-side electrical connection points 131 and the first bond pads 111, thus electrically connecting the wiring substrate 13 to the first die 11. Yet, some of the metal blocks 15a are selectively electrically connected to some of the front-side electrical connection points 131, thereby enabling external electrical connection of these front-side electrical connection points 131 via the conductive bumps 17. Still yet, some of the metal blocks 15a may be selectively electrically connected to multiple of the front-side electrical connection points 131 to achieve a circuit layout of or electrical conduction through these front-side electrical connection points 131. Still yet, some of the metal blocks 15a may be selectively electrically connected to multiple of the first bond pads 111 to achieve a circuit layout of or electrical conduction through these first bond pads 111.

A layout of the first conductive traces 15 may depend on a predetermined circuit layout.

In some embodiments, the first conductive traces 15 may be arranged into two or more layers. That is, there are two or more layers of metal blocks of respective patterns.

In the embodiment shown in Fig. 1, the second conductive traces 16 include a pattern of a number of metal blocks 16a. That is, the second conductive traces include a layer of metal blocks that form a pattern. Some of the metal blocks 16a are selectively electrically connected to some of the back-side electrical connection points 132 and the second bond pads 121, thus electrically connecting the wiring substrate 13 to the second die 12. Yet, some of the metal blocks 16a may be selectively electrically connected to multiple of the back-side electrical connection points 132 to achieve a circuit layout of or electrical conduction through these back-side electrical connection points 132. Still yet, some of the metal blocks 16a may be selectively electrically connected to multiple of the second bond pads 121 to achieve a circuit layout of or electrical conduction through these second bond pads 121.

The second conductive traces 16 may be laid out depending on a predetermined circuit layout.

In some embodiments, the second conductive traces 16 may be arranged into two or more layers. That is, there are two or more layers of metal blocks of respective patterns.

Referring to Fig. 1, in this embodiment, the conductive bumps 17 on the first conductive traces 15 serve as external connection terminals for the MCM package 1.

In some embodiments, there may be an anti-oxidation layer overlying the conductive bumps 17.

The anti-oxidation layer may include b1) a tin layer, or b2) a nickel layer and a gold layer, which are sequentially stacked from the bottom upward in this order, or b3) a nickel layer, a palladium layer and a gold layer, which are sequentially stacked from the bottom upward in this order. The conductive bumps 17 may be fabricated from copper, and the anti-oxidation layer may serve to prevent oxidation of the copper, which may degrade electrical connection performance.

In some embodiments, the conductive bumps 17 may be provided thereon with

solder balls configuration for flip-chip packaging of the MCM package 1.

The first dielectric layer 18 and the second dielectric layer 19 may each be made of, for example, an organic polymeric insulating material, an inorganic insulating material or a composite material. The organic polymeric insulating material may be one or more of polyimide, an epoxy resin, an ABF, PBO, an organic polymer film and another organic material with similar insulating properties. The composite material may be, for example, an inorganic-organic composite material. Alternatively, it may be an inorganic-organic polymer composite material such as, for example, a SiO₂/resin/polymer composite material. The inorganic insulating material may be, for example, at least one of silicon dioxide and silicon nitride. Compared to the inorganic insulating material, the organic polymeric insulating material and the composite material suffer from less tensile stress and can prevent surface warpage of the MCM package 1.

In the MCM package 1, on the one hand, the first die assembly 10 with the oppositely facing active surfaces enables the MCM package 1 to have a small size and a compact structure. On the other hand, the wiring substrate 13 enables not only electrical connection of the first die 11 and the second die 12 but also wiring on both the front side 14a and the back side 14b of the plastic encapsulation layer 14. Compared to wiring only on a single surface, this allows higher wiring density and enables the MCM package 1 to have more complex wiring and an even smaller size.

One embodiment of the present application provides a method for manufacturing the MCM package 1 of Fig. 1. Fig. 2 shows a flowchart of this method. Figs. 3 to 9 are schematic diagrams showing intermediate structures formed during the process of Fig. 2.

Reference is first made to step S1 in Fig. 2, as well as to Figs. 3 and 4. A carrier board 2 and multiple objects 3 to be packaged carried on the carrier board 2. Each object 3 to be packaged includes a wiring substrate 13 with a through opening 133 and a first die assembly 10 disposed within the through opening 133. The wiring substrate 13 contains wiring lines 130 with front-side electrical connection points 131 and back-side electrical connection points 132. The front-side electrical connection points

131 are exposed on a front side 13a of the wiring substrate 13, and the back-side electrical connection points 132 are exposed on a back side 13b of the wiring substrate 13. The first die assembly 10 includes at least a first die 11 and a second die 12. The first die 11 includes a number of first bond pads 111 disposed on an active surface 11a of the first die 11, and the second die 12 includes a number of second bond pads 121 disposed on an active surface 12a of the second die 12. The active surface 12a of the second die 12 is covered by a second protective layer 120. The active surface 11a of the first die 11 and the active surface 12a of the second die 12 face opposite directions. The front side 13a of the wiring substrate 13 and the active surface 11a of the first die 11 face toward the carrier board 2. Fig. 3 is a top view of the carrier board and the multiple objects to be packaged. Fig. 4 is a cross-sectional view taken along line AA in Fig. 3.

The first die 11 and the second die 12 may be dies in need of electrical interconnection and are each not limited to having any particular function. In some embodiments, the first die 11 and the second die 12 may be, for example, power dies, memory dies, sensor dies, RF dies or associated control chips.

Referring to Fig. 4, the first die 11 includes the active surface 11a and a back side 11b opposite thereto. The first die 11 may include various devices formed on a semiconductor substrate and electrical interconnects electrically connected to the devices. The first bond pads 111 exposed on the active surface 11a of the first die 11 are connected to the electrical interconnects and configured to input/output electrical signals to or from the individual devices.

The second die 12 includes the active surface 12a and a back side 12b opposite thereto. The second bond pads 121 are exposed on the active surface 12a. The second die 12 may also include various devices formed on a semiconductor substrate and electrical interconnects electrically connected to the devices. The second bond pads 121 exposed on the active surface 12a of the second die 12 are connected to the electrical interconnects and configured to input/output electrical signals to or from the individual devices.

With continued reference to Fig. 4, in this embodiment, the first die assembly 10

is a die stack structure in which the first die 11 and the second die 12 are arranged back-to-back. In other embodiments, the first die assembly 10 may include one or more first dies 11 and may include one or more second dies 12. The first die 11 and second die 12 may be arranged in a staggered manner, or even side by side. In this case, the back side of the second die may be also exposed on the front side of the plastic encapsulation layer.

In this embodiment, the first die 11 has a larger area than the second die 12. In other embodiments, the area of the second die 12 may be alternatively larger than that of the first die 11.

The second protective layer 120 covers the second bond pads 121 in order to protect the second bond pads 121 during thinning of the plastic encapsulation layer 14.

In this embodiment, the active surface 11a of the first die 11 may also be provided thereon with a first protective layer 110 for relieving stress in the first bond pads 111 during thinning of the plastic encapsulation layer 14. In some embodiments, the first protective layer 110 on the active surface 11a of the first die 11 may also be omitted.

The first die 11 and the second die 12 are formed by dicing wafers. Taking the first die 11 as an example, the wafer has an active surface and a back side. The first bond pads 111 and an insulating layer (not shown) for protecting the first bond pads 111 are exposed on the active surface of the wafer. The first die 11 is formed by dicing the wafer. Accordingly, the first die 11 includes the active surface 11a and the back side 11b, and the first bond pads 111 and the insulating layer between adjacent first bond pads 111 are exposed on the active surface 11a.

The first protective layer 110 is applied to the active surface 11a of the first die 11. The application of the first protective layer 110 may include: applying the first protective layer 110 to the active surface of the wafer before the wafer is diced to form the first die 11; and dicing the wafer with the first protective layer 110 to form the first die 11 with the first protective layer 110. Alternatively, the application of the first protective layer 110 may include, after the first die 11 is obtained by dicing the wafer, applying the first protective layer 110 to the active surface 11a of the first die 11.

The first protective layer 110 and/or the second protective layer 120 may each be

an insulating material such as an organic polymeric insulating material or an inorganic insulating material. Examples of the organic polymeric insulating material may include, among others, polyimide, epoxy resins, ABF, PBO, organic polymer films, organic polymer composite materials and other organic materials with similar insulating properties.

The organic polymeric insulating material may be a) laminated on the first bond pads 111 and the insulating layer between adjacent first bond pads 111/the second bond pads 121 and an insulating layer between adjacent second bond pads 121, or b) coated or printed and then cured on the first bond pads 111 and the insulating layer between adjacent first bond pads 111/the second bond pads 121 and the insulating layer between adjacent second bond pads 121, or c) molded on the first bond pads 111 and the insulating layer between adjacent first bond pads 111/the second bond pads 121 and the insulating layer between adjacent second bond pads 121.

In case of the first protective layer 110 and/or the second protective layer 120 each being formed of an inorganic material such as silicon dioxide, silicon nitride or the like, the material may be deposited on the first bond pads 111 and the insulating layer between adjacent first bond pads 111/the second bond pads 121 and the insulating layer between adjacent second bond pads 121.

One or more such first protective layers 110 and/or second protective layers 120 may be included.

Before the dicing, the wafer and hence the first die 11 and/or second die 12 may be thinned from the back side of the wafer.

The wiring substrate 13 includes the wiring lines 130 and an insulating material filled between the wiring lines 130.

The wiring substrate 13 may either be a monolithic substrate surrounding the first die assembly 10, or consisting of multiple portions.

In this embodiment, referring to Fig. 3, the wiring substrates 13 in the objects 3 to be packaged are separate from one another. In some embodiments, the wiring substrates 13 in the objects 3 to be packaged may be joined together.

The carrier board 2 is a hard board. Examples thereof may include plastic plates,

glass plates, ceramic plates, metal plates, etc.

In some embodiments, a thickness of the wiring substrates 13 is less than a thickness of the die stack structures.

One embodiment of arranging the multiple objects 3 to be packaged on a surface of the carrier board 2 may include the steps as follows.

a) With the front sides of the wiring substrates 13 being oriented toward the carrier board 2, place the wiring substrates 13 onto the carrier board 2. In particular, an adhesive layer may be coated on the entire surface of the carrier board 2, and the wiring substrates 13 may be placed on the adhesive layer.

b) With the first protective layer 110 on the first dies 11 being oriented toward a first carrier board, place the first dies 11 onto the first carrier board, and with the second protective layer 120 on the second dies 12 being oriented toward a second carrier board, place the second dies 12 onto the second carrier board. In particular, adhesive layers may be coated on surfaces of the first and second carrier board, and adhesive layers may be provided on the back sides 11b of the first dies 11 and/or the back sides 12b of the second dies 12. The first and second carrier boards may be aligned and the back sides 11b of the first dies 11 may be bonded to the back sides 12b of the second dies 12, forming the die stack structures. The first carrier board may be then removed.

c) With the die stack structures being oriented toward the through openings 133 in the wiring substrates 13, align the second carrier board with the carrier board 2, attach the die stack structures to the carrier board 2 at the bottom of the through openings 133, and remove the second carrier board.

Steps a) and b) may be performed in any order, or simultaneously. The first and second carrier boards differ from the carrier board 2.

The adhesive layers coated on the surfaces of the carrier boards may be formed of materials allowing the carrier boards to be easily stripped away, such as thermally separable materials that lose their adhesiveness when heated, or UV separable materials that lose their adhesiveness when irradiated by ultraviolet (UV) light.

In another embodiment, step a) is performed prior to step b). In this case, first of

all, with the first dies 11 being oriented so that the first protective layer 110 thereon face toward the through openings 133 in the wiring substrates 13, the first dies 11 are attached to the carrier board 2. Subsequently, the second carrier board with the second dies 12 carried thereon is aligned with the carrier board 2, and the back sides 11b of the first dies 11 are bonded to the back sides 12b of the second dies 12, forming the die stack structures. The second carrier board carrying the second dies 12 is then removed.

In yet another embodiment, first of all, with the first dies 11 being oriented so that the first protective layer 110 thereon face toward the carrier board 2, the first dies 11 are placed on the carrier board 2. Subsequently, with the wiring substrates 13 oriented with their front sides 13a facing the carrier board 2, the wiring substrates 13 are aligned with the first dies 11 so that the through opening 133 of each wiring substrate 13 is aligned with a respective one of the first dies 11, and then placed on the carrier board 2. Afterward, the second carrier board with the second dies 12 carried thereon is aligned with the carrier board 2, and the back sides 11b of the first dies 11 are bonded to the back sides 12b of the second dies 12, forming the die stack structures. The second carrier board with the second dies 12 carried thereon is then removed.

In some embodiments, the thickness of the wiring substrates 13 is greater than the thickness of the die stack structures. In this case, one embodiment of arranging the multiple objects 3 to be packaged on the surface of the carrier board 2 may include: performing steps a) and b); and in step c), with the through openings 133 in the wiring substrates 13 being oriented toward the die stack structures, aligning the second carrier board with the carrier board 2, attaching the wiring substrates 13 to the second carrier board, and removing the carrier board 2.

In order to facilitate the subsequent dicing operation, each object 3 to be packaged is arranged on a distinct surface portion of the carrier board 2. Attaching multiple objects 3 to be packaged onto the surface of the carrier board 2 allows simultaneous fabrication of the same number of MCM packages 1, i.e., batch production thereof. This can lead to a reduction in cost.

After that, referring to step S2 in Fig. 2 and to Fig. 5, a plastic encapsulation layer 14 is formed on the surface of the carrier board 2 so as to embed the objects 3 to be

packaged. Referring to Fig. 6, the plastic encapsulation layer 14 is thinned until the second protective layer 120 and the back sides 13b of the wiring substrates 13 are exposed.

The plastic encapsulation layer 14 may be made of, for example, one or more of an epoxy resin, a polyimide resin, a benzocyclobutene resin, a polybenzoxazole resin, polybutylene terephthalate, polycarbonate, polyethylene terephthalate, polyethylene, polypropylene, polyolefin, polyurethane, polyolefin, polyethersulfone, polyamide, polyurethane, an ethylene-vinyl acetate copolymer, polyvinyl alcohol, etc. Alternatively, the plastic encapsulation layer 14 may be formed of any of various polymers or resin/polymer composite materials. Correspondingly, the packaging process may involve filling a liquid plastic encapsulation material between the first die assemblies 10 and the wiring substrates 13 and curing the material within a plastic encapsulation mold at a high temperature. In some embodiments, the plastic encapsulation layer 14 may be alternatively formed by a molding method suitable for plastic materials, such as thermal compression molding, transfer molding or the like.

The plastic encapsulation layer 14 may include a front side 14a and an opposing backside 14b.

Referring to Fig. 6, the plastic encapsulation layer 14 is thinned from the back side 14b, and the thinning may be accomplished mechanically, for example, with a grinding wheel.

Specifically, during the thinning of the plastic encapsulation layer 14, when the thickness of the wiring substrates 13 is less than the thickness of the first die assemblies 10, the second protective layer 120 will have been partially removed upon the exposure of the back sides 13b of the wiring substrates 13. When the thickness of the wiring substrates 13 is greater than the thickness of the first die assemblies 10, the wiring substrates 13 will have been partially removed from the back side 13b upon the exposure of the second protective layer 120.

During the formation and thinning of the plastic encapsulation layer 14, the second protective layer 120 can protect the second bond pads 121 and the electrical interconnects and devices in the second dies 12 and the first dies 11 against damage,

and the first protective layer 110 can relieve stress in the first bond pads 111.

As a result of this step, plastic encapsulation bodies for the objects 3 to be packaged are formed.

Next, referring to step S3 in Fig. 2 and to Fig. 7, in the second protective layer 120, second openings 120a are formed, in which the second bond pads 121 are exposed. Moreover, second conductive traces 16 are formed on the second protective layer 120, the second bond pads 121, the back-side electrical connection points 132 and the back side 14b of the plastic encapsulation layer 14 to electrically connect the second dies 12 to the wiring lines 130. Further, a second dielectric layer 19 embedding the second conductive traces 16 is formed.

In this embodiment, the second conductive traces 16 are formed in a single layer. The formation of the second conductive traces 16 for each of the multiple objects 3 to be packaged includes steps S31 to S38 below.

Step S31: Form a photoresist layer on the second protective layer 120 of the second dies 12, the back sides 13b of the wiring substrates 13 and the back side 14b of the plastic encapsulation layer 14.

In step S31, in one optional embodiment, the photoresist layer formed may be a photosensitive film. The photosensitive film may be torn from a tape and attached to the second protective layer 120 on the second dies 12, the back sides 13b of the wiring substrates 13 and the back side 14b of the plastic encapsulation layer 14. In other optional embodiments, the photoresist layer may be formed by thermally curing applied liquid photoresist.

Step S32: Pattern the photoresist layer by exposing and developing it.

In step S32, the photoresist layer is patterned. In other optional embodiments, the photoresist layer may be replaced with another easily removable sacrificial material.

Step S33: With the patterned photoresist layer serving as a mask, the second openings 120a in which the second bond pads 121 are partially exposed are formed by performing a dry or wet etching process on the second protective layer 120. In each second opening 120a, a respective one of the second bond pads 121 may be partially exposed. In other embodiments, in each second opening 120a, two or more of the

second bond pads 121 may be partially exposed.

The second protective layer 120 may be formed of a laser reactive material, such as an epoxy resin. In this case, the second openings 120a may be formed by denaturalization induced by laser irradiation. The second protective layer 120 may also be formed of a photosensitive material such as polyimide. In this case, the second openings 120a may be formed by exposure and subsequent development. The second protective layer 120 may be formed of a material suitable to be treated by dry or wet etching, such as silicon dioxide or silicon nitride. In this case, the second openings 120a may be formed by dry or wet etching.

Step S34: Remove the remainder of the photoresist layer by ashing.

Step S35: Form another photoresist layer on the second protective layer 120 on the second dies 12, the second bond pads 121 exposed from the second protective layer 120, the back sides 13b of the wiring substrates 13 and the back side 14b of the plastic encapsulation layer 14.

Reference can be made to the above description in connection with the formation of the photoresist layer in step S31 for details of the formation of this photoresist layer.

Step S36: Expose and develop the photoresist layer so that a first predefined portion of the photoresist layer which is complementary to a pattern of metal blocks 16a of the second conductive traces 16 being fabricated is retained.

Step S37: Fill a metal layer in the remainder that is complementary to the first predefined portion, resulting in the formation of the metal blocks of the second conductive traces 16.

Some of the metal blocks 16a are positioned so as to enable electrical connection of the back-side electrical connection points 132 with the second bond pads 121 and hence electrical connection of the wiring substrates 13 with the second dies 12. Some of the metal blocks 16a are positioned so as to enable electrical connection of multiple of the back-side electrical connection points 132 and hence a circuit layout of or electrical conduction through these back-side electrical connection points 132. Yet, some of the metal blocks 16a may be positioned so as to enable electrical connection of multiple of the second bond pads 121 and hence a circuit layout of or electrical

conduction through these second bond pads 121.

Step S37 may be accomplished using an electroplating process. Electroplating of copper or aluminum is an established technique.

In particular, before the photoresist layer is formed in step S35, a seed layer may be formed over the second protective layer 120 on the second dies 12, the second bond pads 121 exposed from the second protective layer 120, the back sides 13b of the wiring substrates 13 and the back side 14b of the plastic encapsulation layer 14 by physical or chemical vapor deposition. The seed layer may serve to supply power to the electroplating of copper or aluminum.

The electroplating process may be an electrolytic plating process or an electroless plating process. In the former case, with the article to be plated serving as a cathode, an electrolyte is electrolyzed to form a metal layer on the article to be plated. In the latter case, metal ions in a solution are reduced and precipitate to form a metal layer on the object to be plated. In some embodiments, the metal blocks 16a may be alternatively formed by sputtering and subsequent etching.

Step S38: Remove the remaining first predefined portion of the photoresist layer by ashing.

After the ashing, a portion of the seed layer corresponding to the first predefined region is removed using a dry or wet etching process.

Upper surfaces of the metal blocks 16a of the second conductive traces 16 may be planarized using a polishing process, such as a chemical mechanical polishing (CMP) process.

It is to be noted that, in step S3, the metal blocks 16a of the second conductive traces 16 may be arranged according to the design requirements. The second conductive traces 16 may be arranged in the same manner or not in different objects 3 to be packaged.

Further, in some embodiments, the second conductive traces 16 may be arranged in two or more layers. That is, there are two or more layers of metal blocks of respective patterns.

In the step in which the second dielectric layer 19 is formed, in order to prevent

the plastic encapsulation layer 14 from being scratched in the processes used, the second dielectric layer 19 may be so formed as to also cover the back side 14b of the plastic encapsulation layer 14.

The second dielectric layer 19 may be formed of an insulating material such as, for example, an organic polymeric insulating material or an inorganic insulating material. Examples of the organic polymeric insulating material may include, among others, polyimide, epoxy resins, ABF, PBO, organic polymer films, organic polymer composite materials and other organic materials with similar insulating properties.

The organic polymeric insulating material may be a) laminated on the second conductive traces 16, the second protective layer 120 uncovered by the second conductive traces 16, the back sides 13b of the wiring substrates 13 and the back side 14b of the plastic encapsulation layer 14, or b) coated and then cured on the second conductive traces 16, the second protective layer 120 uncovered by the second conductive traces 16, the back sides 13b of the wiring substrates 13 and the back side 14b of the plastic encapsulation layer 14, or c) molded on the second conductive traces 16, the second protective layer 120 uncovered by the second conductive traces 16, the back sides 13b of the wiring substrates 13 and the back side 14b of the plastic encapsulation layer 14.

In case of the second dielectric layer 19 being formed of an inorganic material such as silicon dioxide, silicon nitride or the like, the material may be deposited on the second conductive traces 16, the second protective layer 120 uncovered by the second conductive traces 16, the back sides 13b of the wiring substrates 13 and the back side 14b of the plastic encapsulation layer 14.

Compared to the inorganic insulating material, the organic polymeric insulating material suffers from less tensile stress and can prevent surface warpage of the plastic encapsulation body that may occur due to a large area of the second dielectric layer 19.

One or more of such second dielectric layers 19 may be formed.

Subsequently, referring to step S4 in Fig. 2 and to Fig. 8, the carrier board 2 is removed, and the active surfaces 11a of the first dies 11, the front sides 13a of the wiring substrates 13 and the front side 14a of the plastic encapsulation layer 14 are

thus exposed. Additionally, first conductive traces 15 are formed on the first bond pads 111, the front-side electrical connection points 131 and the front side 14a of the plastic encapsulation layer 14 to electrically connect the first dies 11 to the wiring lines 130.

Referring to Fig. 8, after the carrier board 2 is removed, a first support board 4 may be provided on the second dielectric layer 19.

The removal of the carrier substrate 2 may be accomplished, for example, by laser lift-off or UV irradiation.

The first support board 4 may be formed during the subsequent formation of the first conductive traces 15, and/or the conductive bumps 17 and/or the first dielectric layers 18 to provide support.

The first support board 4 is a hard board. Examples thereof may include glass plates, ceramic plates, metal plates, etc.

In this embodiment, as the active surfaces 11a of the first dies 11 are provided thereon with the first protective layer 110, as a result of removing the carrier board 2, the first protective layer 110 is exposed. Prior to the formation of the first conductive traces 15, first openings 110a in which the first bond pads 111 are exposed are formed in the first protective layer 110.

The first protective layer 110 may be formed of a laser reactive material, such as an epoxy resin. In this case, the first openings 110a may be formed by denaturalization induced by laser irradiation. The first protective layer 110 may also be formed of a photosensitive material such as polyimide. In this case, the first openings 110a may be formed by exposure and subsequent development. The first protective layer 110 may be formed of a material suitable to be treated by dry or wet etching, such as silicon dioxide or silicon nitride. In this case, the first openings 110a may be formed by dry or wet etching.

In some embodiments, in the first die assemblies 10 in the objects 3 to be packaged in step S1, the first protective layer 110 may have been provided therein with the first openings 110a in which the first bond pads 111 are exposed.

Reference can be made to the above description in connection with the formation of the metal blocks 16a of the second conductive traces 16 for details of the formation

of a pattern of metal blocks 15a of the first conductive traces 15. A layout of the first conductive traces 15 may depend on a predetermined layout.

In this embodiment, first conductive traces 15 are arranged in a single layer.

Some of the metal blocks 15a are selectively electrically connected to some of the front-side electrical connection points 131 and the first bond pads 111, thus electrically connecting the wiring substrates 13 to the first dies 11. Yet, some of the metal blocks 15a are selectively electrically connected to some of the front-side electrical connection points 131, thereby enabling external electrical connection of these front-side electrical connection points 131 via the conductive bumps 17. Still yet, some of the metal blocks 15a may be selectively electrically connected to multiple of the front-side electrical connection points 131 to achieve a circuit layout of or electrical conduction through these front-side electrical connection points 131. Still yet, some of the metal blocks 15a may be selectively electrically connected to multiple of the first bond pads 111 to achieve a circuit layout of or electrical conduction through these first bond pads 111.

In other embodiments, the first conductive traces 15 may include two or more layers of metal blocks of respective patterns.

Next, referring to step S5 in Fig. 2 and to Fig. 8, conductive bumps 17 are formed on the first conductive traces 15 and a first dielectric layer 18 is formed so as to embed the first conductive traces 15 and part of the conductive bumps 17, with the rest of the conductive bumps 17 being exposed from the first dielectric layer 18.

Step S5 may include steps S51 to S55 below.

Step S51: Form a photoresist layer on the metal blocks 15a, an insulating material layer exposed on the front sides 13a of the wiring substrates 13 and the front side 14a of the plastic encapsulation layer 14.

In step S51, in one optional embodiment, the photoresist layer formed may be a photosensitive film. The photosensitive film may be torn from a tape and attached to the metal blocks 15a, the insulating material layer exposed on the front sides 13a of the wiring substrates 13 and the front side 14a of the plastic encapsulation layer 14. In other optional embodiments, the photoresist layer may be formed by thermally curing

applied liquid photoresist.

Step S52: Expose and develop the photoresist layer so that a second predefined portion of the photoresist layer which is complementary to the conductive bumps 17 being fabricated is retained.

In step S52, the photoresist layer is patterned. In other optional embodiments, the photoresist layer may be replaced with another easily removable sacrificial material.

Step S53: Form the conductive bumps 17 by filling a metal layer in the remainder that is complementary to the second predefined portion.

Step S53 may be accomplished using an electroplating process. Electroplating of copper or aluminum is an established technique. Prior to the electroplating of copper or aluminum, a seed layer for supplying power may be formed by physical or chemical vapor deposition.

Step S54: Remove the remaining second predefined portion of the photoresist layer by ashing.

Upper surfaces of the conductive bumps 17 may be planarized using a polishing process, such as a CMP process.

Step S55: Referring to Fig. 8, form the first dielectric layer 18 over the conductive bumps 17, the metal blocks 15a, the insulating material layer exposed on the front sides 13a of the wiring substrates 13 and the front side 14a of the plastic encapsulation layer 14 and thin the first dielectric layer 18 until the conductive bumps 17 are exposed.

Reference can be made to the above description in connection with the material and formation of the second dielectric layer 19 for details of the material and formation of the first dielectric layer 18.

In the step in which the first dielectric layer 18 is formed, in order to prevent the plastic encapsulation layer 14 from being scratched in the processes used, the first dielectric layer 18 may be so formed as to also cover the front side 14a of the plastic encapsulation layer 14 between adjacent objects 3 to be packaged.

The first dielectric layer 18 may be thinned by polishing until the conductive bumps 17 embedded therein are exposed.

One or more first dielectric layers 18 may be formed.

After the conductive bumps 17 are formed, in a first optional embodiment, referring to Fig. 8, the conductive bumps 17 serve for external connection of the MCM packages 1.

In a second optional embodiment, an anti-oxidation layer is further formed over the exposed conductive bumps 17.

The anti-oxidation layer may include, for example, b1) a tin layer, or b2) a nickel layer and a gold layer, which are sequentially stacked from the bottom upward in this order, or b3) a nickel layer, a palladium layer and a gold layer, which are sequentially stacked from the bottom upward in this order. The anti-oxidation layer may be formed by an electroplating process. The conductive bumps 17 may be fabricated from copper, and the anti-oxidation layer may serve to prevent oxidation of the copper, which may degrade electrical connection performance.

In a third optional embodiment, solder balls configuration for flip-chip packaging of the MCM packages 1 (see Fig. 1) are further formed on the exposed conductive bumps 17.

After the conductive bumps 17 are formed, referring to Fig. 9, the first support board 4 is removed.

The removal of the first support board 4 may be accomplished, for example, by laser lift-off or UV irradiation.

Afterwards, referring to step S6 in Fig. 2 and to Figs. 9 and 1, multiple MCM packages 1 are obtained by performing a dicing operation, each including one of the objects 3 to be packaged.

In the embodiment with the wiring substrates 13 in the individual objects 3 to be packaged being joined together, the wiring substrates 13 are separated as a result of the dicing operation in step S6.

In each of the MCM packages 1 resulting from the above steps, on the one hand, the first die assembly 10 with the oppositely facing active surfaces enables the MCM package 1 to have a small size and a compact structure. On the other hand, the wiring substrate 13 enables not only electrical connection of the first die 11 and the second

die 12 but also wiring on both the front side 14a and the back side 14b of the plastic encapsulation layer 14. Compared to wiring only on a single surface, this allows higher wiring density and enables the MCM package 1 to have more complex wiring and an even smaller size.

The use of the wiring substrate 13 provides the following advantages. First, providing fine wires in the wiring substrate 13 instead of in a rewiring layer can make them less vulnerable to short circuits and can thus result in an increase in product yield. Moreover, the first conductive traces 15 and/or second conductive traces 16 are allowed to be arranged in a reduced number of layers, reducing process complexity. Second, the wiring substrate 13 is pre-formed and can be tested before packaging, avoiding it from being put into use while being defective. Third, the pre-formed wiring substrate 13 is fabricated separately from the packaging process, resulting in overall time savings in the packaging process.

Further, wiring layers required to be formed over the active surfaces 11a, 12a of the dies can be provided in the wiring substrate 13, and multiple complex circuits in the wiring substrate 13 can be electrically connected to the bond pads 111, 121 on the active surface 11a, 12a and thereby embedded in the package 1, enhancing overall performance of the package 1.

In a second embodiment of the present application, there is provided another method for manufacturing the MCM package 1 of Fig. 1. Fig. 10 shows a flowchart of this method. Figs. 11 and 12 are schematic diagrams showing intermediate structures formed during the process of Fig. 10.

As shown Figs. 10 to 12, the method of this embodiment is substantially similar to that of the embodiment shown in Fig. 2 except for the differences noted below.

In step S2', with reference to Fig. 5, the plastic encapsulation layer 14 is formed on the surface of the carrier board 2 so as to embed the objects 3 to be packaged.

In step S3', with reference to Fig. 11, the carrier board 2 is removed, exposing the active surfaces 11a of the first dies 11, the front sides 13a of the wiring substrates 13 and the front side 14a of the plastic encapsulation layer 14. Additionally, the first conductive traces 15 are formed on the first bond pads 111, the front-side electrical

connection points 131 and the front side 14a of the plastic encapsulation layer 14, electrically connecting the first dies 11 to the wiring lines 130.

In step S4', with reference to Fig. 11, the conductive bumps 17 are formed on the first conductive traces 15, and the first dielectric layer 18 is formed so as to embed the first conductive traces 15 and part of the conductive bumps 17, with the rest of the conductive bumps 17 being exposed from the first dielectric layer 18.

In step S5', with reference to Fig. 12, the plastic encapsulation layer 14 is thinned until the second protective layer 120 and the back side 13b of the wiring substrate 13 are exposed. The second openings 120a in which the second bond pads 121 are exposed are then formed in the second protective layer 120. The second conductive traces 16 are formed on the second protective layer 120, the second bond pads 121, the back-side electrical connection points 132 and the back side 14b of the plastic encapsulation layer 14, electrically connecting the second dies 12 to the wiring lines 130. The second dielectric layer 19 is formed so as to embed the second conductive traces 16.

Reference can be made to the above description in connection with the formation of the plastic encapsulation layer in step S2 of the above embodiment for details of step S2', step S4 for step S3', step S5 for step S4', and the thinning of the plastic encapsulation layer in step S2 and step S3 for step S5'.

Specifically, in step S3', with reference to Figs. 11 and 12, the first support board 4 may be provided on the back side 14b of the plastic encapsulation layer 14 after the carrier board 2 is removed and removed at the end of step S4', and a second support board 5 may be provided on the conductive bumps 17 and the first dielectric layer 18 and removed at the end of step S5'.

In other words, the carrier board 2 is removed and the first conductive traces 15, the conductive bumps 17 and the first dielectric layer 18 embedding the first conductive traces 15 and the conductive bumps 17 are formed, followed by the provision of the second support board 5 on the first dielectric layer 18 and the conductive bumps 17, thinning of the plastic encapsulation layer 14 and formation of the second conductive traces 16 and the second dielectric layer 19.

In some embodiments, the plastic encapsulation layer 14 may also be thinned in step S2'.

Fig. 13 is a schematic cross-sectional view showing the structure of an MCM package according to a third embodiment of the present application. Referring to Fig. 13, the MCM package 6 of this embodiment is substantially similar to the MCM package 1 of the forgoing embodiment, except that the first protective layer 110 is omitted, that on the active surfaces 11a of the first dies 11, the front sides 13a of the wiring substrates 13 and the front side 14a of the plastic encapsulation layer 14, a third dielectric layer 20 is provided with third openings 20a therein in which the first bond pads 111 and the front-side electrical connection points 131 are exposed, and that the first conductive traces 15 are provided on the first bond pads 111, the front-side electrical connection points 131 and the third dielectric layer 20.

A corresponding fabrication method differs from those of the above two embodiments in removal of the carrier board 2 and thus exposure of the active surfaces 11a of the first dies 11, the front sides 13a of the wiring substrates 13 and the front side 14a of the plastic encapsulation layer 14, formation of the third dielectric layer 20 on the exposed active surfaces 11a of the first dies 11, front sides 13a of the wiring substrates 13 and front side 14a of the plastic encapsulation layer 14, formation in the third dielectric layer 20 of the third openings 20a in which the first bond pads 111 and the front-side electrical connection points 131 are exposed and subsequent formation of the first conductive traces 15 on the first bond pads 111, the front-side electrical connection points 131 and the third dielectric layer 20 in step S4/S3'.

Reference can be made to the above description in connection with the materials of the first dielectric layer 18 and the second dielectric layer 19 for details of the material of the third dielectric layer 20.

The third dielectric layer 20 may be formed of a laser reactive material, such as an epoxy resin. In this case, the third openings 20a may be formed by denaturalization induced by laser irradiation. The third dielectric layer 20 may also be formed of a photosensitive material such as polyimide. In this case, the third openings 20a may be formed by exposure and subsequent development. The third dielectric layer 20 may be

formed of a material suitable to be treated by dry or wet etching, such as silicon dioxide or silicon nitride. In this case, the third openings 20a may be formed by dry or wet etching.

Fig. 14 is a schematic cross-sectional view showing the structure of an MCM package according to a fourth embodiment of the present application. Referring to Fig. 14, the MCM package 7 of this embodiment is substantially similar to the MCM packages 1, 6 of the foregoing embodiments, except that the conductive bumps 17 are provided on the second conductive traces 16 and correspondingly the second dielectric layer 19 embeds the second conductive traces 16 and part of the conductive bumps 17, with the rest of the conductive bumps 17 being exposed from the second dielectric layer 19. Moreover, the first dielectric layer 18 embeds the first conductive traces 15.

A corresponding fabrication method differs from those of the above three embodiments in formation of the conductive bumps 17 on the second conductive traces 16 and the second dielectric layer 19 embedding the second conductive traces 16 and part of the conductive bumps 17, with the rest of the conductive bumps 17 being exposed from the second dielectric layer 19, following the formation of the second conductive traces 16, in step S3/S5', and in forming the first dielectric layer 18 embedding the first conductive traces 15 in step S5/S4'.

Fig. 15 is a schematic cross-sectional view showing the structure of an MCM package according to a fifth embodiment of the present application. Referring to Fig. 15, the MCM package 8 of this embodiment is substantially similar to the MCM packages 1, 6, 7 of the foregoing embodiments, except that the first die assemblies 10 are replaced with dies, for example, the first dies 11. Correspondingly, the conductive bumps 17 are provided on the back-side electrical connection points 132 so as to be exposed from the second dielectric layer 19, and the first dielectric layer 18 encapsulates the conductive traces 15.

In other embodiments, the first die assemblies 10 may also be replaced with the second dies 12 or second die assemblies each including a plurality of first dies 11 or a plurality of second dies 12. In other words, in the second die assemblies, all the dies are oriented with their active surfaces facing toward the same direction.

Although the present application has been disclosed above, it is in no way limited to the foregoing description. Any person skilled in the art can make various changes and modifications without departing from the spirit and scope of the application. Accordingly, the scope of protection of this application is intended to be defined by the appended claims.

Claims

1. A multi-chip module (MCM) package, comprising:

a first die assembly comprising at least:

a first die comprising a number of first bond pads provided on an active surface of the first die, and

a second die comprising a number of second bond pads provided on an active surface of the second die, the active surface of the second die covered by a second protective layer, the second bond pads exposed from the second protective layer, the active surface of the first die and the active surface of the second die facing opposite to each other;

a wiring substrate surrounding the first die assembly, the wiring substrate provided therein with wiring lines, the wiring lines comprising front-side electrical connection points and back-side electrical connection points, the front-side electrical connection points exposed on a front side of the wiring substrate, the back-side electrical connection points exposed on a back side of the wiring substrate;

a plastic encapsulation layer encapsulating the first die assembly and the wiring substrate, the second protective layer, the second bond pads and the back side of the wiring substrate exposed on a back side of the plastic encapsulation layer and that the active surface of the first die and the front side of the wiring substrate are exposed on a front side of the plastic encapsulation layer;

first conductive traces provided on the first bond pads, the front-side electrical connection points and the front side of the plastic encapsulation layer to electrically connect the first die to the wiring lines;

second conductive traces provided on the second bond pads, the back-side electrical connection points and the back side of the plastic encapsulation layer to electrically connect the second die to the wiring lines;

first conductive bumps connected to the first conductive traces;

a first dielectric layer embedding the first conductive traces and the first conductive bumps, the first conductive bumps exposed from the first dielectric layer;

and

a second dielectric layer embedding the second conductive traces.

2. The MCM package according to claim 1, wherein the first die assembly is a die stack structure.

3. The MCM package according to claim 1 or 2, wherein the first conductive bumps connected to the first conductive traces are replaced with second conductive bumps connected to the second conductive traces and, correspondingly, the second dielectric layer embeds the second conductive traces and the second conductive bumps, the second conductive bumps exposed from the second dielectric layer and the first dielectric layer embeds the first conductive traces.

4. The MCM package according to claim 1, further comprising a third dielectric layer provided on the active surface of the first die, the front side of the wiring substrate and the front side of the plastic encapsulation layer, the first bond pads and the front-side electrical connection points exposed from the third dielectric layer, wherein the first conductive traces are provided on the first bond pads, the front-side electrical connection points and the third dielectric layer.

5. The MCM package according to claim 1, further comprising a first protective layer covering the active surface of the first die, the first bond pads exposed from the first protective layer, wherein the first protective layer and the first bond pads are exposed on the front side of the plastic encapsulation layer.

6. The MCM package according to claim 1, wherein

the second protective layer is made of a material which is one of an organic polymeric insulating material, an inorganic insulating material or a composite material; and/or

the first dielectric layer is made of a material which is one of an organic polymeric insulating material, an inorganic insulating material or a composite material; and/or

the second dielectric layer is made of a material which is one of an organic polymeric insulating material, an inorganic insulating material or a composite material.

7. A method of manufacturing a multi-chip module (MCM) package, comprising:

providing a carrier board and multiple objects to be packaged carried on the carrier board, wherein each of the objects to be packaged comprises:

a wiring substrate with a through opening, the wiring substrate provided therein with wiring lines, the wiring lines comprising front-side electrical connection points and back-side electrical connection points, the front-side electrical connection points exposed on a front side of the wiring substrate, the back-side electrical connection points exposed on a back side of the wiring substrate, and

a first die assembly provided in the through opening, the first die assembly comprising at least a first die and a second die, the first die comprising a number of first bond pads provided on an active surface of the first die, the second die comprising a number of second bond pads provided on an active surface of the second die, the active surface of the second die covered by a second protective layer, the active surface of the first die and the active surface of the second die facing opposite to each other, the front side of the wiring substrate and the active surface of the first die facing the carrier board;

forming on a surface of the carrier board a plastic encapsulation layer embedded the objects to be packaged; thinning the plastic encapsulation layer until the second protective layer and the back sides of the wiring substrates are exposed;

forming in the second protective layer second openings in which the second bond pads are exposed; forming second conductive traces on the second protective layer, the second bond pads, the back-side electrical connection points and the back side of the plastic encapsulation layer, which electrically connect the second dies to the wiring lines; forming a second dielectric layer embedding the second conductive traces;

removing the carrier board, exposing the active surfaces of the first dies, the front sides of the wiring substrates and the front side of the plastic encapsulation layer; forming first conductive traces on the first bond pads, the front-side electrical connection points and the front side of the plastic encapsulation layer, which electrically connect the first dies to the wiring lines;

forming first conductive bumps on the first conductive traces and a first dielectric layer embedding the first conductive traces and the conductive bumps, the first

conductive bumps exposed from the first dielectric layer; and

forming a plurality of the MCM packages by dicing, each of which comprises one of the objects to be packaged.

8. The method according to claim 7, wherein after the second conductive traces are formed, second conductive bumps on the second conductive traces and a second dielectric layer embedding the second conductive traces and the second conductive bumps, the second conductive bumps exposed from the second dielectric layer are formed, and wherein forming the first conductive bumps on the first conductive traces and the first dielectric layer embedding the first conductive traces and the conductive bumps, the first conductive bumps exposed from the first dielectric layer is replaced with forming the first dielectric layer embedding the first conductive traces.

9. The method according to claim 7, wherein after the carrier board is removed and the first conductive traces, the first conductive bumps and the first dielectric layer embedding the first conductive traces and the first conductive bumps are formed, a support board is provided on the first dielectric layer and the first conductive bumps, the plastic encapsulation layer is thinned, and the second conductive traces and the second dielectric layer are formed.

10. The method according to claim 7, wherein after the carrier board is removed, a third dielectric layer is formed on the exposed active surfaces of the first dies, front sides of the wiring substrates and front side of the plastic encapsulation layer, a plurality of third openings in which the first bond pads and the front-side electrical connection points are exposed are formed in the third dielectric layer, and the first conductive traces is formed on the first bond pads, the front-side electrical connection points and the third dielectric layer.

11. The method according to claim 7, wherein in the first die assembly, the active surface of the first die is covered by a first protective layer, which faces the carrier board and is provided therein with first openings in which the first bond pads are exposed.

12. The method according to claim 7, wherein in the first die assembly, the active surface of the first die is covered by a first protective layer facing the carrier board,

and wherein after the carrier board is removed and before the first conductive traces are formed, first openings in which the first bond pads are exposed are formed in the first protective layer.

13. The method according to any of claims 7 to 12, wherein the wiring substrates of the objects to be packaged are joined together and separated as a result of forming the plurality of the MCM packages by dicing.

14. A multi-chip module (MCM) package, comprising:

a die comprising a number of bond pads provided on an active surface of the die;

a wiring substrate surrounding the die, the wiring substrate provided therein with wiring lines, the wiring lines comprising front-side electrical connection points and back-side electrical connection points, the front-side electrical connection points exposed on a front side of the wiring substrate, the back-side electrical connection points exposed on a back side of the wiring substrate;

a plastic encapsulation layer encapsulating the die and the wiring substrate, the active surface of the die and the front-side electrical connection points exposed on a front side of the plastic encapsulation layer;

conductive traces provided on the bond pads, the front-side electrical connection points and the front side of the plastic encapsulation layer to electrically connect the die to the wiring lines;

conductive bumps connected to the back-side electrical connection points;

a first dielectric layer embedding the conductive traces; and

a second dielectric layer embedding the conductive bumps, the conductive bumps exposed from the second dielectric layer.

15. The MCM package according to claim 14, wherein the die is replaced with a second die assembly comprising a plurality of dies oriented with their active surfaces facing the same direction.

16. A method of manufacturing a multi-chip module (MCM) package, comprising:

providing a carrier board and multiple objects to be packaged carried on the carrier board, wherein each of the objects to be packaged comprises:

a wiring substrate with a through opening, the wiring substrate provided therein with wiring lines, the wiring lines comprising front-side electrical connection points and back-side electrical connection points, the front-side electrical connection points exposed on a front side of the wiring substrate, the back-side electrical connection points exposed on a back side of the wiring substrate, and

a die provided in the through opening, the die comprising a number of bond pads provided on an active surface of the die, the front side of the wiring substrate and the active surface of the die facing the carrier board;

forming on a surface of the carrier board a plastic encapsulation layer embedded the objects to be packaged; thinning the plastic encapsulation layer until the back sides of the wiring substrates are exposed;

removing the carrier board, exposing the active surfaces of the dies, the front sides of the wiring substrates and the front side of the plastic encapsulation layer; forming conductive traces on the bond pads, the front-side electrical connection points and the front side of the plastic encapsulation layer, which electrically connect the dies to the wiring lines; forming a first dielectric layer embedding the conductive traces;

forming conductive bumps on the back-side electrical connection points and a second dielectric layer embedding the conductive bumps, the conductive bumps exposed from the second dielectric layer; and

forming a plurality of the MCM packages by dicing, each of which comprises one of the objects to be packaged.

17. The method of claim 16, wherein the die is replaced with a second die assembly comprising a plurality of dies oriented with their active surfaces facing the same direction.