Claims

1. A 3D integrated circuit, the circuit comprising:

a first wafer comprising a first crystalline substrate, a plurality of first transistors, and first copper interconnecting layers,

wherein said first copper interconnecting layers at least interconnect said plurality of first transistors; and

a second wafer comprising a second crystalline substrate, a plurality of second transistors, and second copper interconnecting layers,

wherein said second copper interconnecting layers at least interconnect said plurality of second transistors,

wherein said second wafer is bonded face-to-face on top of said first wafer,

wherein said bonded comprises copper to copper bonding, and

wherein said second crystalline substrate has been thinned to a thickness of less than 5 micro-meters.

2. The 3D integrated circuit of claim 1, further comprising:

a via through said second crystalline substrate,

wherein said via has a radius of less than 1 micro-meter.

3. The 3D integrated circuit of claim 1,

wherein said second crystalline substrate does not comprise a built-in oxide layer.

4. The 3D integrated circuit of claim 1,

wherein said face-to-face bonding comprises hybrid bonding.

5. The 3D integrated circuit of claim 1,

wherein said first wafer comprises memory control circuits and said second wafer comprises a plurality of memory cells, or said second wafer comprises memory control circuits and said first wafer comprises a plurality of memory cells.

6. The 3D integrated circuit of claim 1, further comprising:

vias through said second crystalline substrate,

wherein at least one of said vias is used to connect said 3D integrated circuit to an external device.

7. The 3D integrated circuit of claim 1,

wherein said first wafer comprises a plurality of self-aligned memory levels.

8. A 3D integrated circuit, the circuit comprising:

a first wafer comprising a first crystalline substrate, a plurality of first transistors, and first copper interconnecting layers,

wherein said first copper interconnecting layers at least interconnect said plurality of first transistors;

a second wafer comprising a second crystalline substrate, a plurality of second transistors, and second copper interconnecting layers,

wherein said second copper interconnecting layers at least interconnect said plurality of second transistors,

wherein said second wafer is bonded face-to-face on top of said first wafer, and

wherein said bonded comprises copper to copper bonding; and

vias through said second crystalline substrate,

wherein said vias have a radius of less than 1 micro-meter, and

wherein at least one of said vias is used to connect said 3D integrated circuit to an external device.

9. The 3D integrated circuit of claim 8,

wherein said bonded comprises copper to copper bonding, and

wherein said second crystalline substrate has been thinned to a thickness of less than 5 micro-meters.

10. The 3D integrated circuit of claim 8,

wherein said second crystalline substrate does not comprise a built-in oxide layer.

11. The 3D integrated circuit of claim 8,

wherein said face-to-face bonding comprises hybrid bonding.

12. The 3D integrated circuit of claim 8,

wherein said first wafer comprises memory control circuits and said second wafer comprises a plurality of memory cells, or said second wafer comprises memory control circuits and said first wafer comprises a plurality of memory cells .

13. The 3D integrated circuit of claim 8,

wherein said first wafer comprises memory control circuits and said second wafer comprises a plurality of DRAM cells, or said second wafer comprises memory control circuits and said first wafer comprises a plurality of DRAM cells.

14. The 3D integrated circuit of claim 8,

wherein said first wafer comprises a plurality of self-aligned memory levels.

15. A 3D integrated circuit, the circuit comprising:

a first wafer comprising a first crystalline substrate, a plurality of first transistors, and first copper interconnecting layers,

wherein said first copper interconnecting layers at least interconnect said plurality of first transistors;

a second wafer comprising a second crystalline substrate, a plurality of second transistors, and second copper interconnecting layers,

wherein said second copper interconnecting layers at least interconnect said plurality of second transistors,

wherein said second wafer is bonded face-to-face on top of said first wafer, and

wherein said bonded comprises copper to copper bonding; and

first vias through said second crystalline substrate,

wherein at least one of said first vias is used to connect said 3D integrated circuit to an external device, and

wherein said first wafer comprises a plurality of self-aligned memory levels.

16. The 3D integrated circuit of claim 15,

wherein bonded comprises hybrid bonding, and

wherein said second crystalline substrate has a thickness of less than 5 micro-meters.

17. The 3D integrated circuit of claim 15,

wherein said second crystalline substrate does not comprise a built-in oxide layer.

18. The 3D integrated circuit of claim 15,

wherein said face-to-face bonding comprises hybrid bonding.

19. The 3D integrated circuit of claim 15, further comprising:

second vias through said first crystalline substrate.

20. The 3D integrated circuit of claim 15,

wherein said second wafer comprises memory control circuits and said first wafer comprises a plurality of non-volatile memory cells.