(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 October 2008 (09.10.2008)

PCT

(10) International Publication Number
WO 2008/121659 A1

(51) International Patent Classification:
H01L 21/20 (2006.01)

(21) International Application Number:
PCT/US2008/058325

(22) International Filing Date: 26 March 2008 (26.03.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/729,189 28 March 2007 (28.03.2007) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),

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(54) Title: SEMICONDUCTOR DEVICE HAVING SELF-ALIGNED EPITAXIAL SOURCE AND DRAIN EXTENSIONS

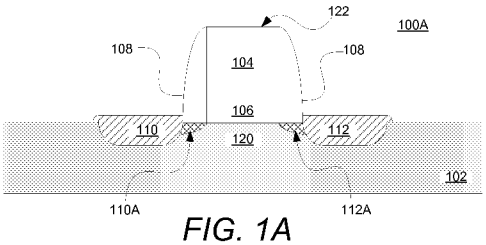


FIG. 1A

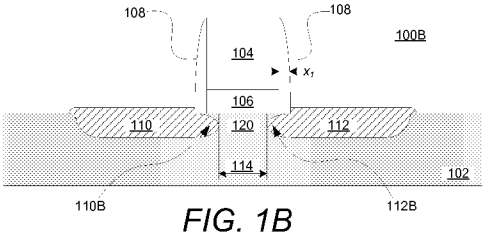


FIG. 1B

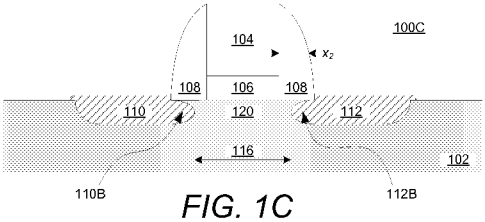


FIG. 1C

(57) Abstract: A method of forming a transistor with self-aligned source and drain extensions in close proximity to a gate dielectric layer of the transistor comprises forming a gate stack on a substrate, implanting a dopant into regions of the substrate adjacent to the gate stack, wherein the dopant increases the etch rate of the substrate and defines the location of the source and drain extensions, forming a pair of spacers on laterally opposite sides of the gate stack that are disposed atop the doped regions of the substrate, etching the doped regions of the substrate and portions of the substrate subjacent to the doped regions, wherein an etch rate of the doped regions is higher than an etch rate of the portions of the substrate subjacent to the doped regions, and depositing a silicon-based material in the etched portions of the substrate.

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European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*