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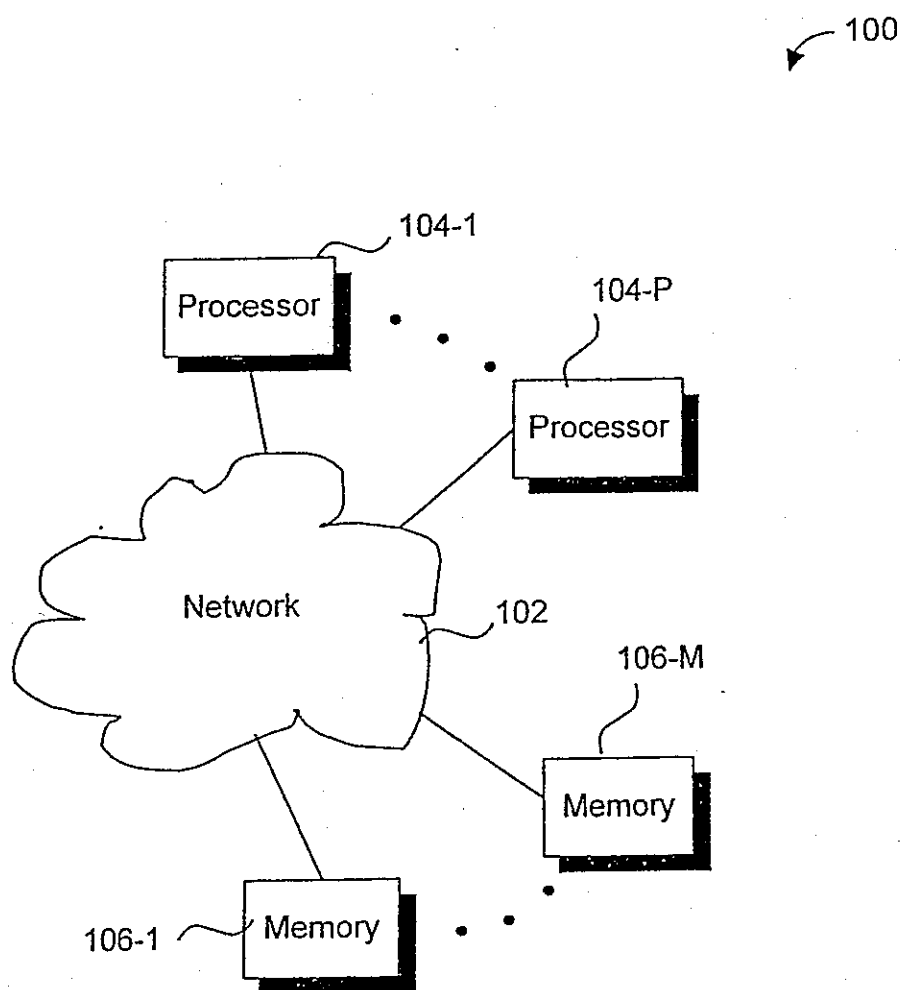


FIG. 1

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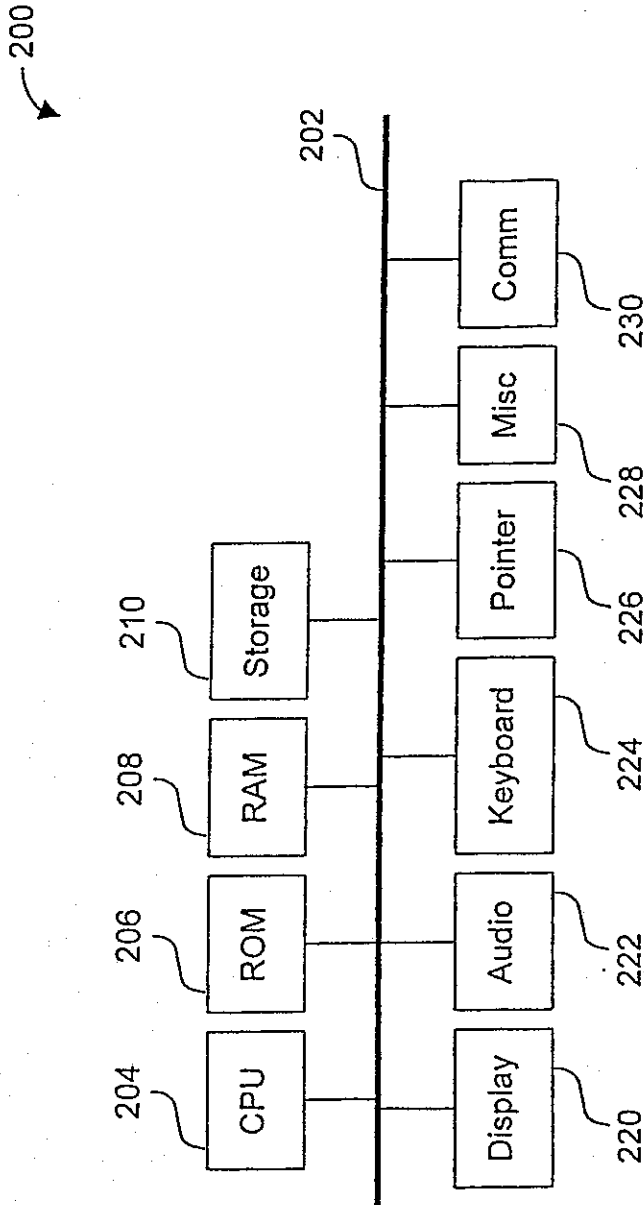


FIG. 2

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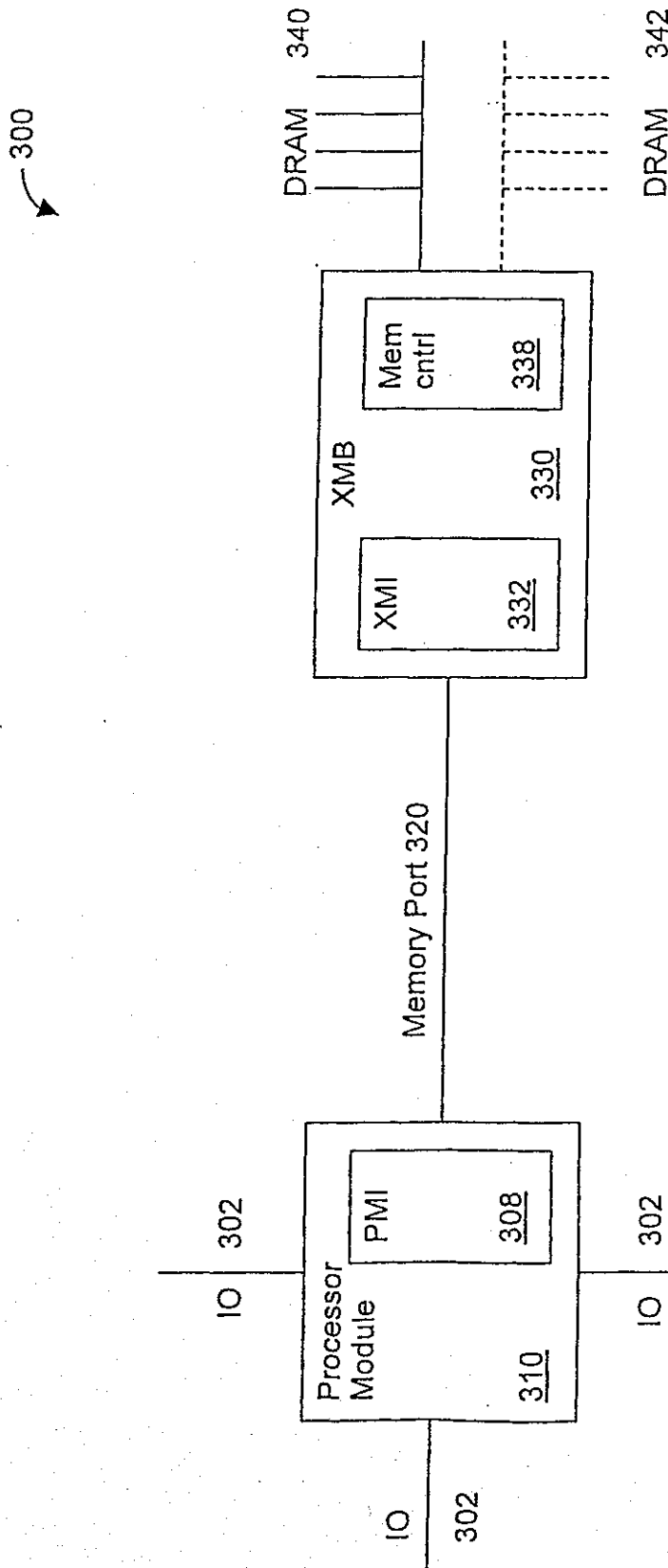


FIG. 3

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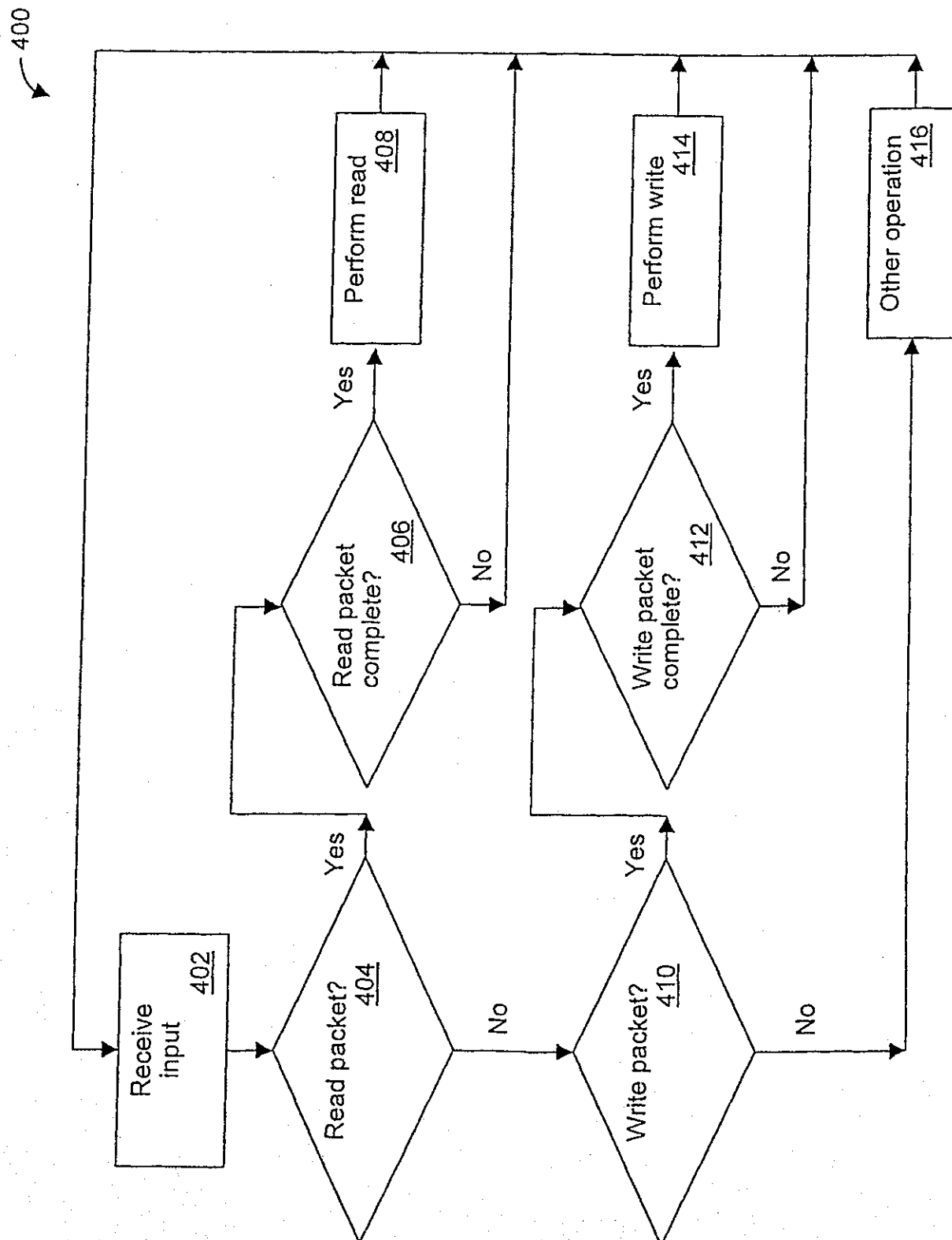


FIG. 4A

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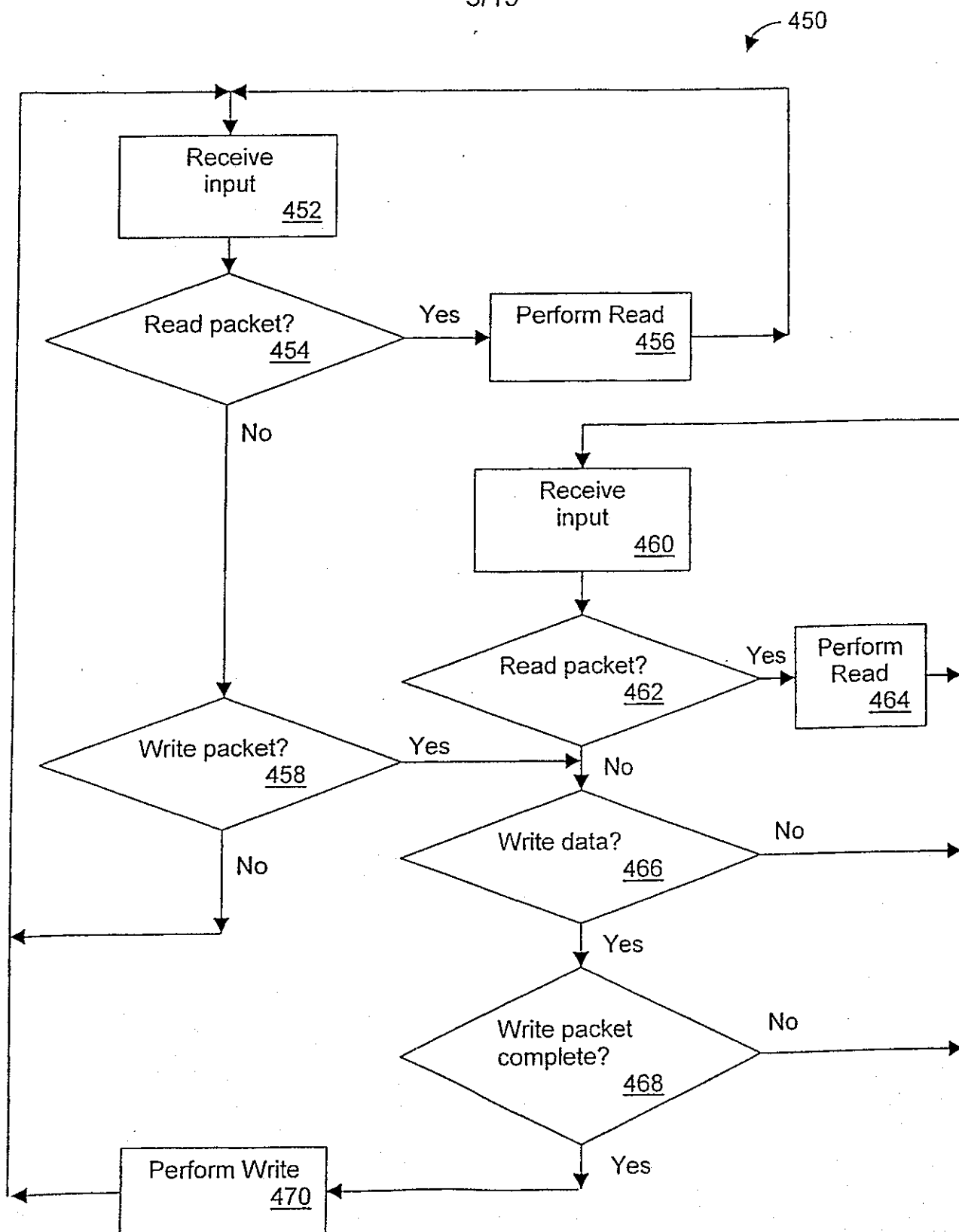
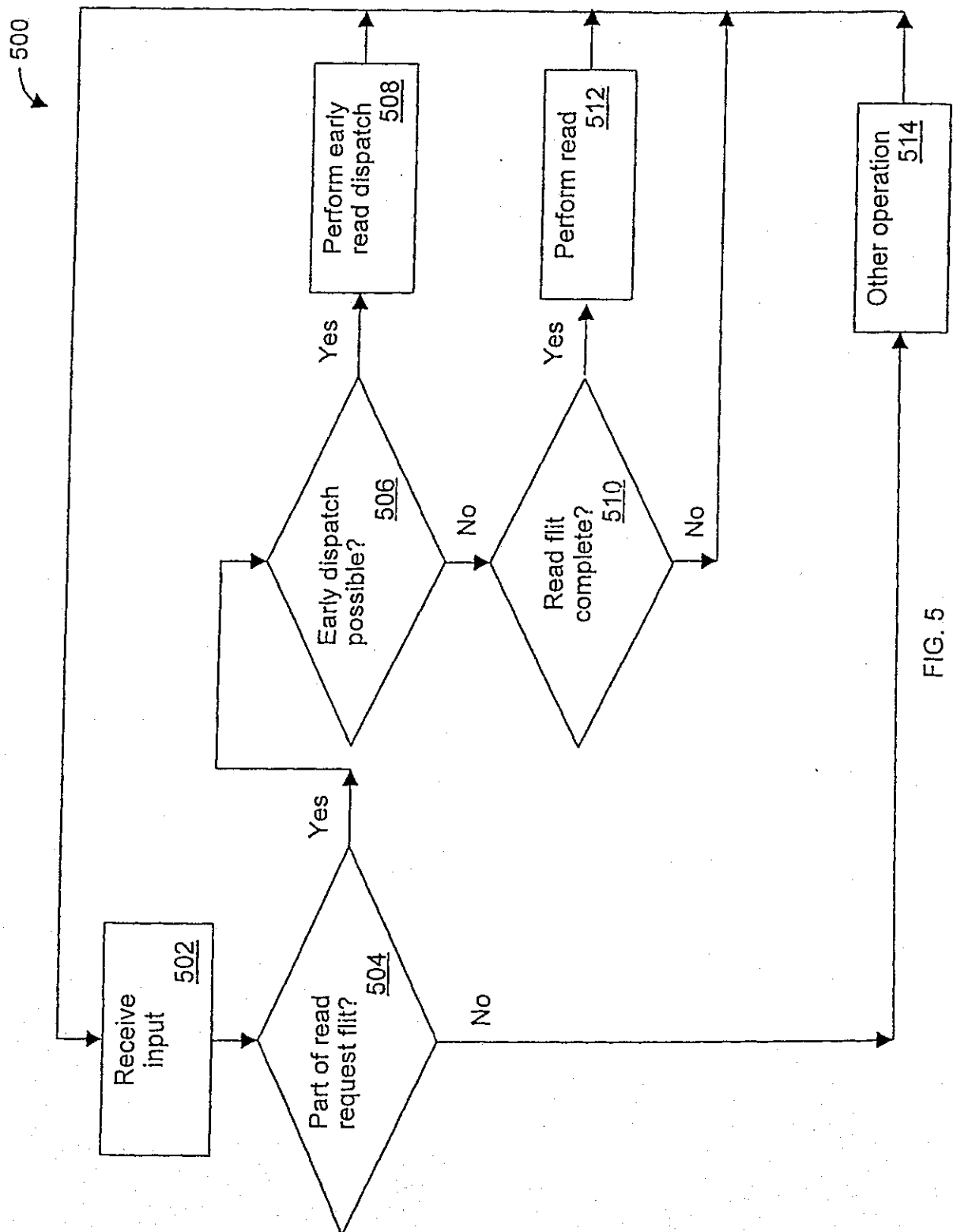


FIG. 4B

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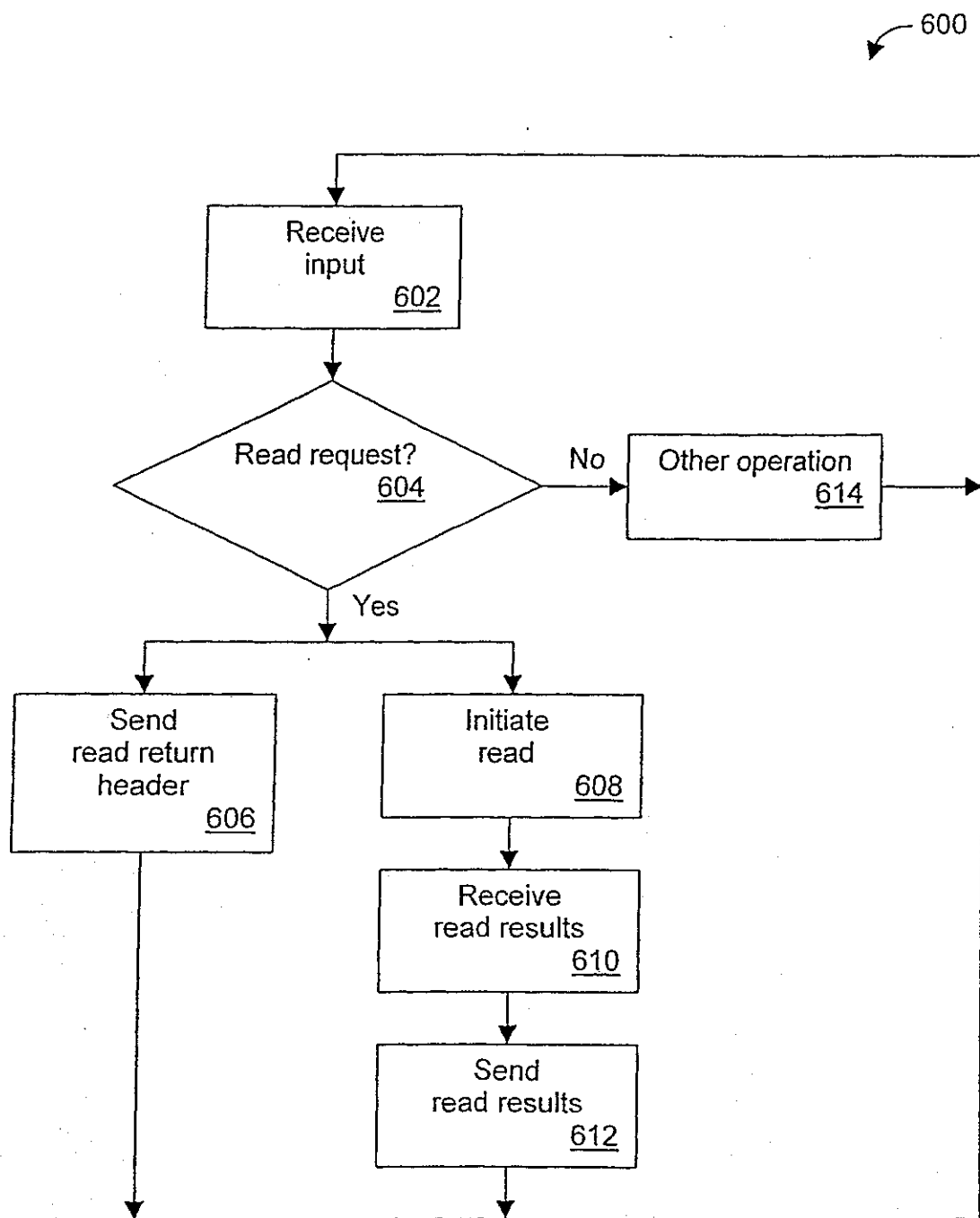


FIG. 6A

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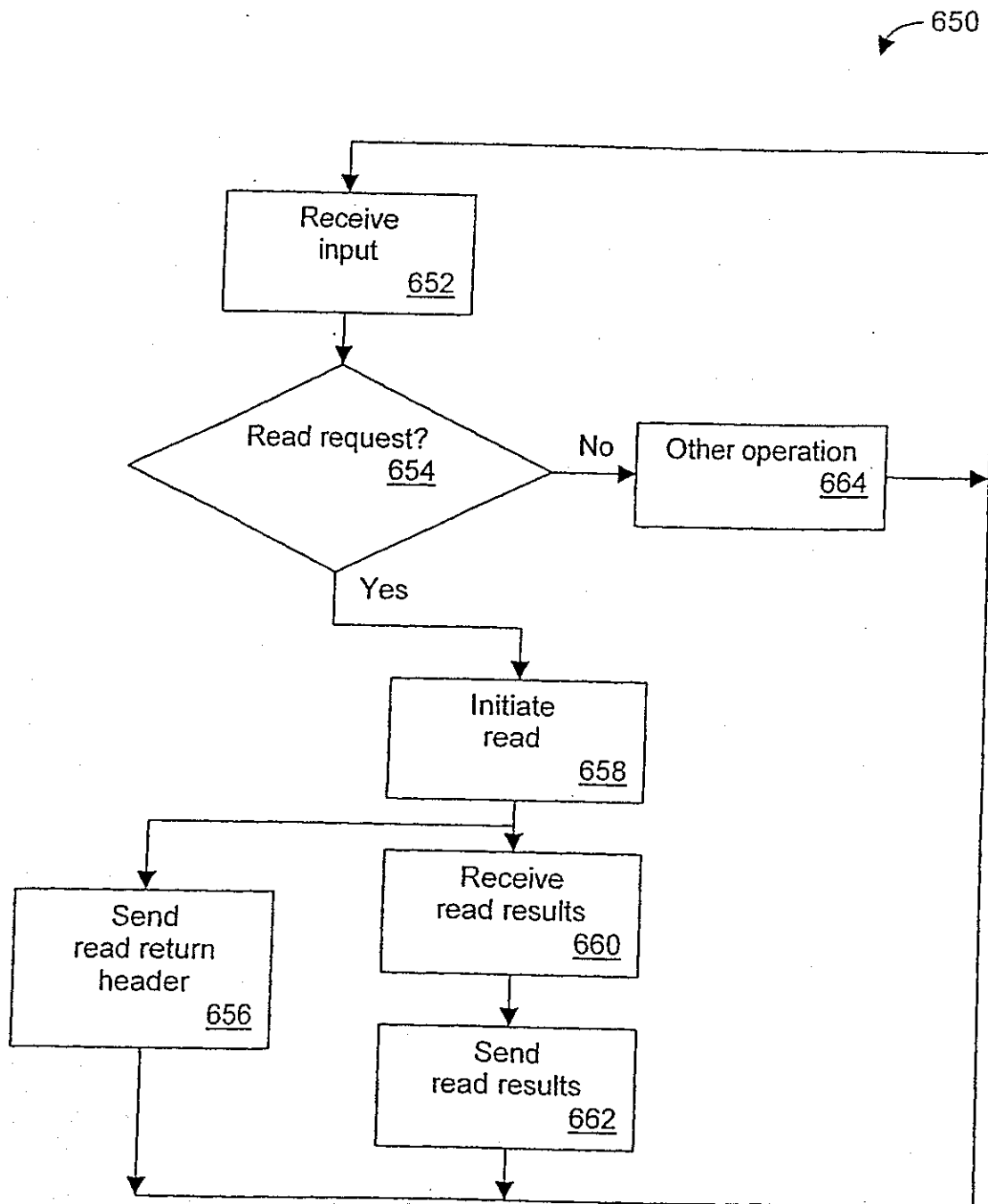


FIG. 6B

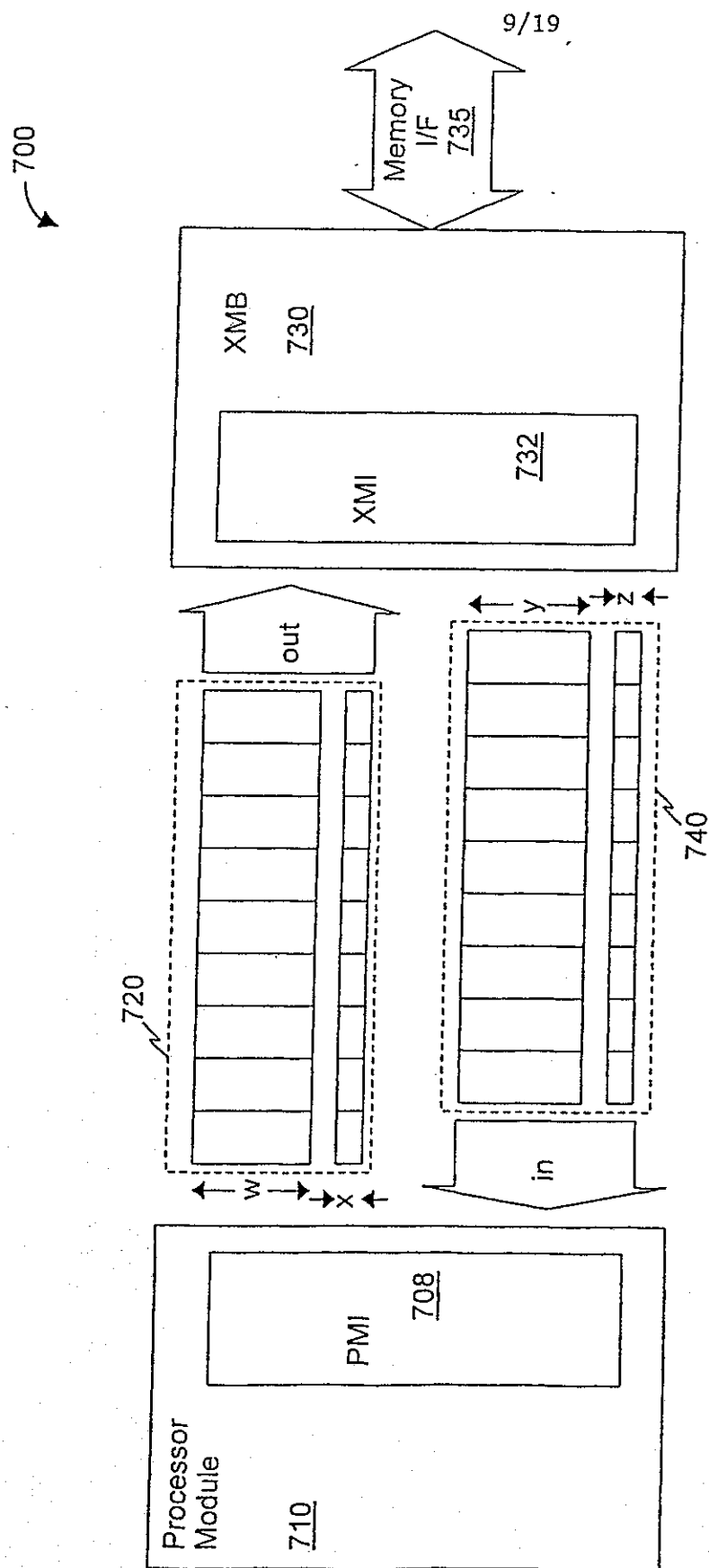


FIG. 7

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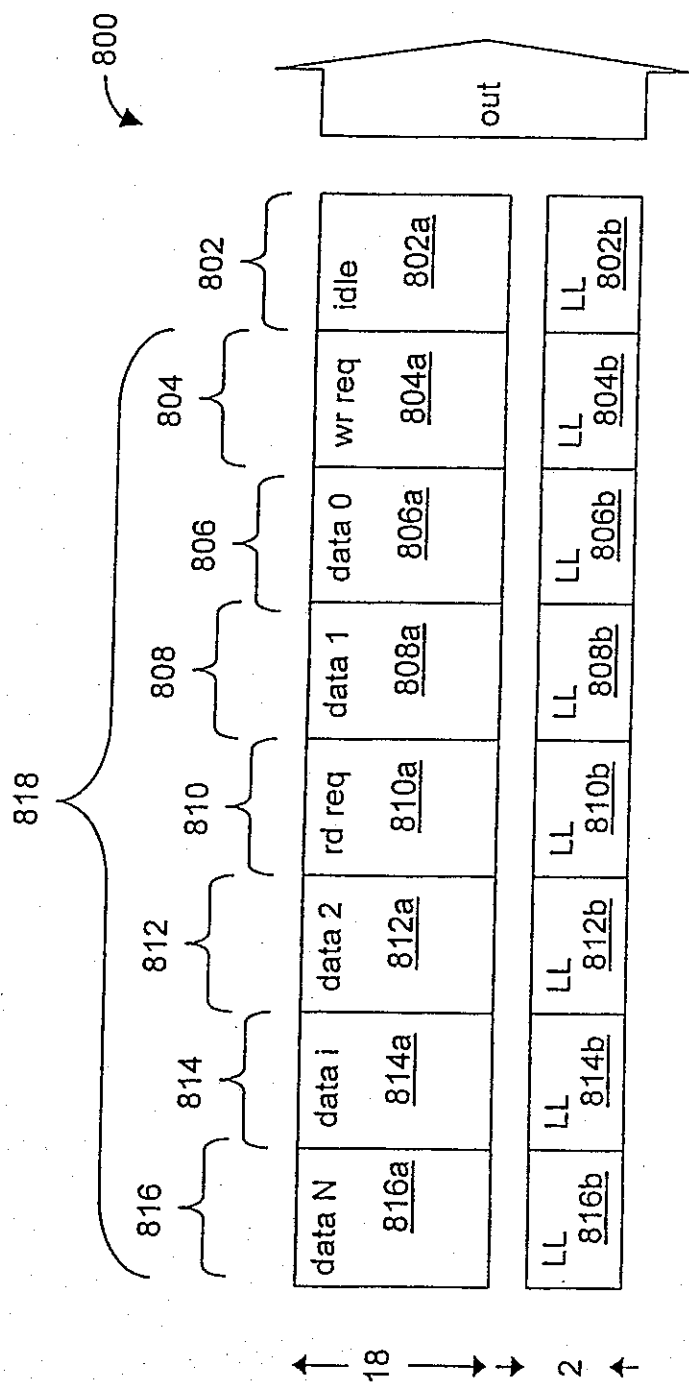


FIG. 8

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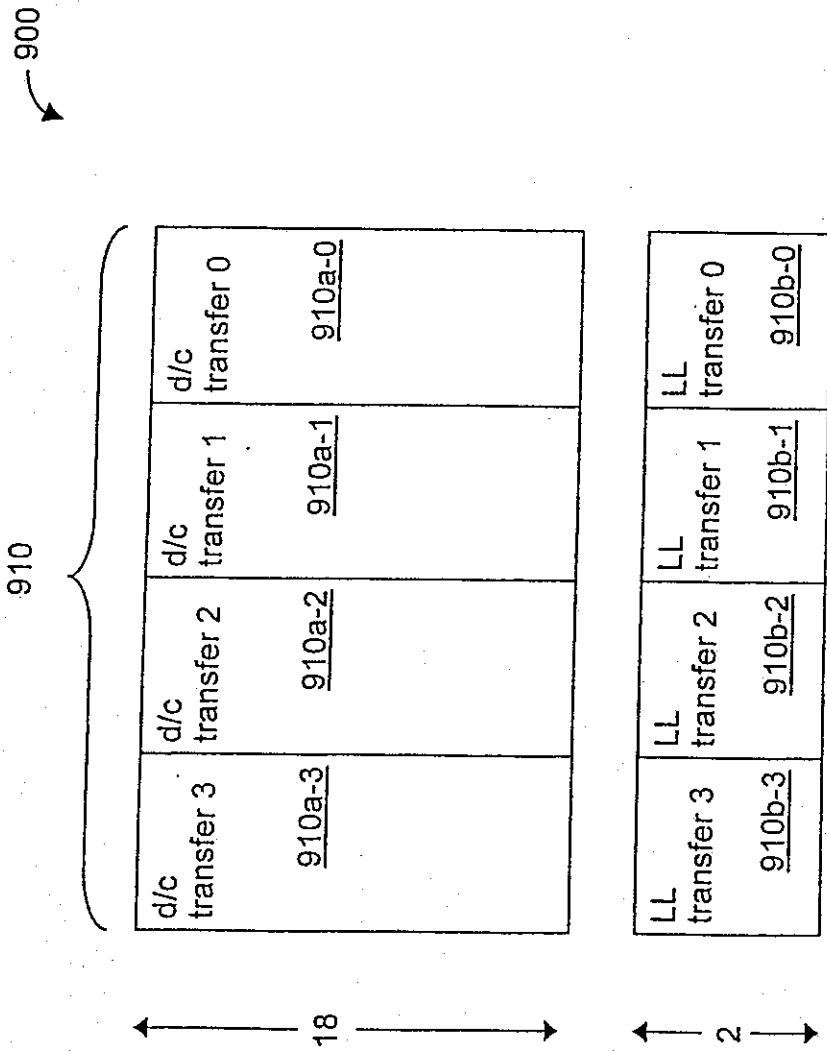


FIG. 9

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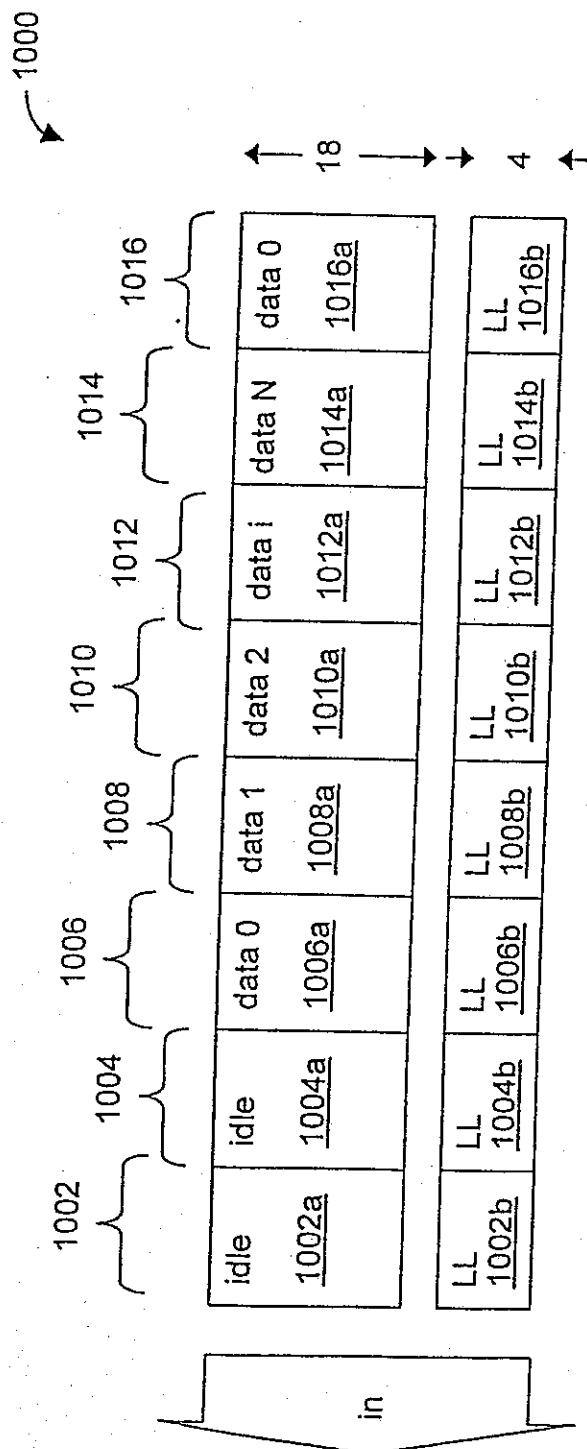


FIG. 10

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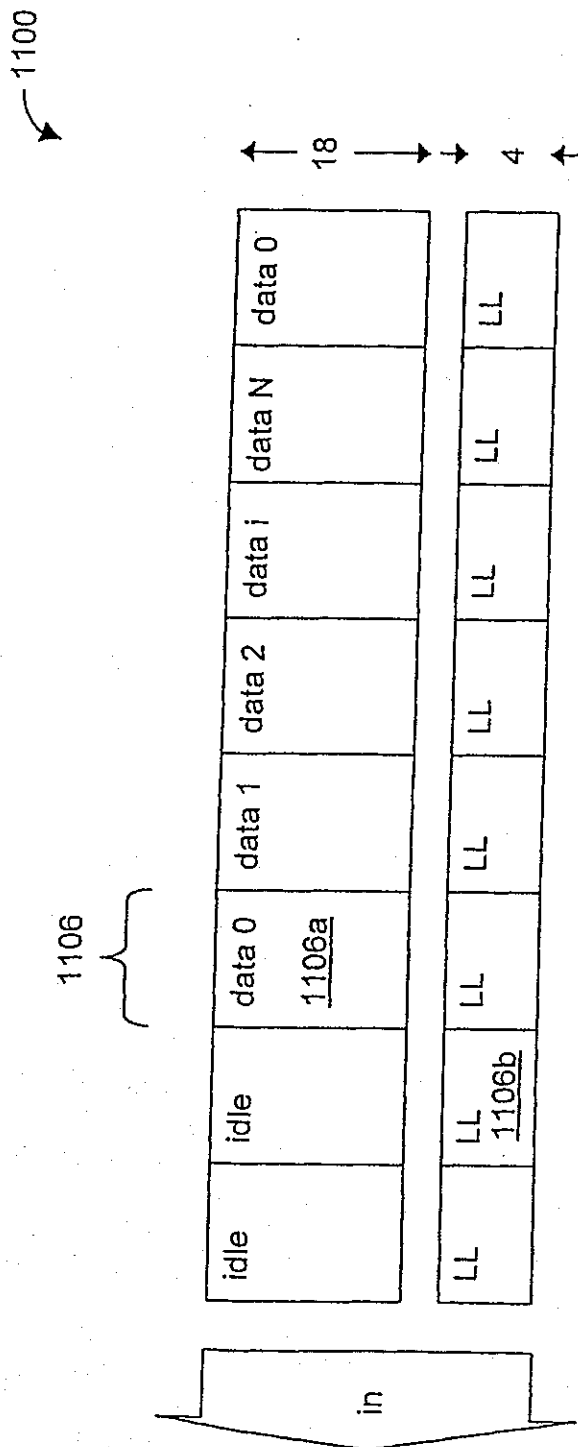


FIG. 11

1200

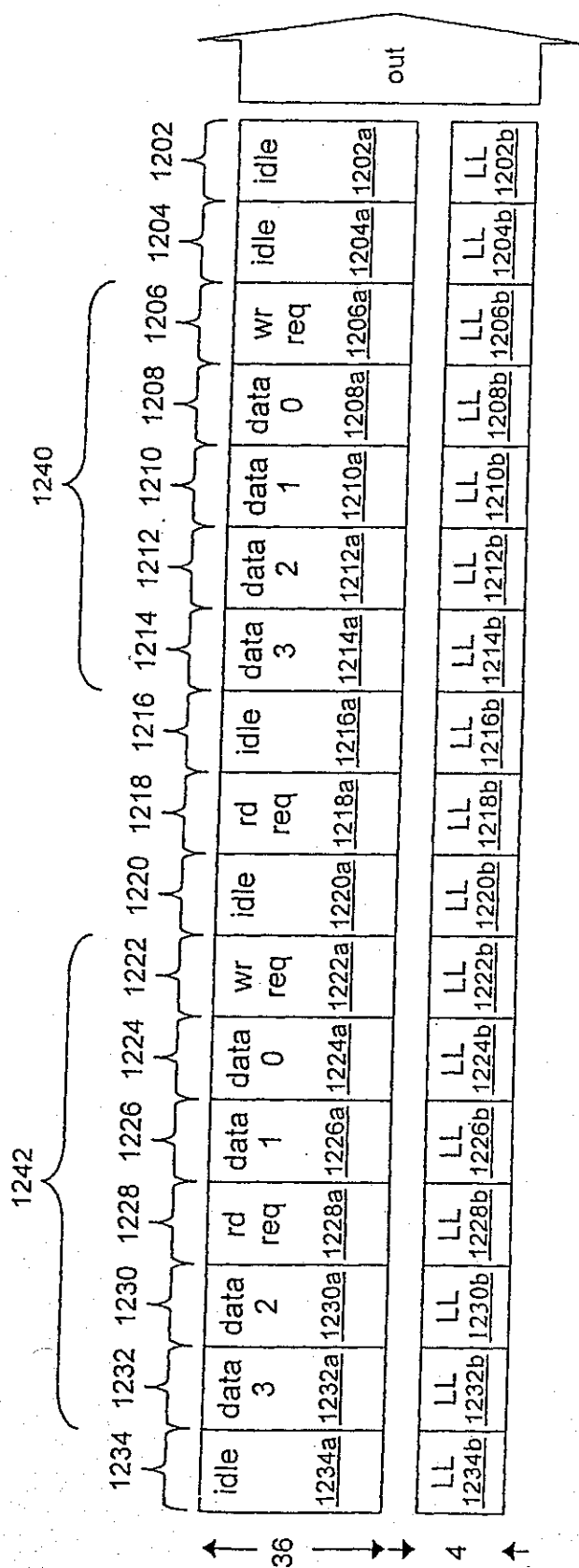


FIG. 12

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1300

↓Transfer	BITS 17:0	
0	Lower Order Address Bits and Read/Write Command	
1	Higher Order Address Bits and Early Read Indicator	
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Stream ID, Size Bits, Cancel Command, Priority, etc.	
3		

FIG. 13

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1400
↙

↓Transfer	BITS 17:0
0	Lower Order Address Bits and Read/Write Command
1	Higher Order Address Bits and Early Read Indicator
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Size Bits, etc.
3	

FIG. 14

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1500

↓Transfer	BITS 17:0
0	Lower Order Configuration Address Bits and Read/Write Command
1	Higher Order Configuration Address Bits and Early Read Indicator
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, etc.
3	

FIG. 15

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1600

LL signals	Transfers 0:3
0	Info and Check Bits
1	Header, Tail, and Check Bits
2	Extended Mode Bits
3	

FIG. 16

1700

LL signals	Transfers 0:3
0	Type and Check Bits
1	
2	Info and Check Bits
3	

FIG. 17

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1800

LL signals	Transfers 0:3
0	Tag, Control, and Check Bits
1	
2	Tag, Info, and Check Bits
3	

FIG. 18

1900

LL signals	Transfers 0:3
0	Tag and Check Bits
1	
2	Tag, Info, and Check Bits
3	

FIG. 19

2000

LL signals	Transfers 0:3
0	Signal and Check Bits
1	
2	Signal, Info, Stop, and Check Bits
3	

FIG. 20