COMPOSITE STRESS SPACER

Abstract

An examplé method embodiment forms spacers that create tensile stress on the substrate on both the PFET and NFET regions. We form PFET and NFET gates and form tensile spacers on the PFET and NFET gates. We implant first ions into the tensile PFET spacers to form neutralized stress PFET spacers. The neutralized stress PFET spacers relieve the tensile stress created by the tensile stress spacers on the substrate. This improves device performance.

Figure 4