Description

The present invention relates generally to apparatus for processing multiple asynchronous composite video signals and particularly to such apparatus as would be useful in a picture within a picture (pix-in-pix) television receiver.

A pix-in-pix television receiver displays a main image derived from one signal and an auxiliary image derived from a second signal. The auxiliary image is usually displayed as an inset in a portion of the main image as shown in FIGURE 1.

Although receivers of this type are available, they usually cost much more than conventional single-picture receivers. This extra cost is incurred due to the extra circuitry used by these receivers to reproduce a single image from two asynchronous signals.

The signals for the main and auxiliary images are typically out of phase because they are broadcast from different sources. They are difficult to combine because each signal contains several synchronizing signal components which are used by the receiver to reproduce an image. For example, the vertical sync pulses determine when each field of the picture starts and the horizontal sync pulses determine when each line starts. Since the main and auxiliary channels are broadcast from different sources, their horizontal and vertical sync pulses may occur at different times. One method of compensating for this lack of synchronism is to delay one signal with respect to the other by a sufficient time to synchronize these pulses. Although this method can be used to obtain a single synchronized image it is undesirable because it usually requires a large memory. Some prior art pix-in-pix receivers use as much as one frame of memory to provide this delay.

More difficult synchronizing problems must be solved if both the main and auxiliary images are to be displayed in color. The component of a composite video signal that controls the hue of colors in its reproduced image is the phase-modulated suppressed chrominance subcarrier. In a conventional single picture receiver the frequency of a phase locked loop oscillator is locked by the color burst signal, a component of the chrominance signal modulated with a reference phase. The signal provided by this oscillator is used by two synchronous detectors to recover quadrature modulated color difference signal components of the composite video signal. This color signal recovery circuitry is extremely sensitive to both the frequency and phase of the color synchronizing burst signal. Consequently, if the color signal components of two composite video signals are to be processed by one set of circuitry, conventional design techniques would require an extremely accurate variable delay element to synchronize the two signals. Alternatively, separate circuits can be used to process the main and auxiliary color signal components. Both of these methods add to the cost of the receiver.

Many prior art pix-in-pix receivers display a monochrome auxiliary picture to avoid the extra cost of color signal synchronization or separate color signal processing. This method, however, is undesirable since the color information in the auxiliary picture is lost.

The added cost of the apparatus used to process two composite video signals is one factor that makes pix-in-pix receivers more expensive than single picture receivers.

In accordance with the present invention, a video signal processing apparatus including a source of time-division multiplexed video signals having alternating first and second mutually independent composite video signal components each having luminance signal components and chrominance signal components including a color burst signal component, is characterised as set out in claim 1.

Another factor which adds to cost is the extra tuner that is used in the prior art to provide the auxiliary picture signal. A pix-in-pix receiver that uses only one tuner to receive both the main and auxiliary signals cand be considerably less expensive that a receiver that needs two tuners. An embodiment of the present invention provides a receiver which uses only one tuner.

FIGURE 1 is a pictorial representation of the type of image that would be produced on a display device coupled to the present invention.

FIGURE 2 is a block diagram of a pix-in-pix television receiver incorporating an embodiment of the present invention.

FIGURE 3 is a block diagram of the main/auxiliary signal processor used in the receiver shown in FIGURE 2.

FIGURE 4 is a block diagram of the comb filter used in the signal processor shown in FIGURE 3.

FIGURE 5 is a table of values useful for explaining the operation of the comb filter shown in FIGURE 4.

FIGURE 6 is a block diagram of the chroma processing circuitry.

FIGURE 7 is a block diagram of the phase error detector used in the chroma processor shown in FIGURE 6.

FIGURES 8A and 8B are block diagrams of the auxiliary signal memories used in the receiver shown in FIGURE 2.

FIGURES 9A and 9B are block diagrams of the main signal luminance and color difference signal memories respectively.

FIGURE 10 is a signal timing diagram useful for explaining the operation of the multiplexer con-

trol circuit used in the receiver shown in FIGURE 2.

FIGURE 11 is a flow diagram useful for explaining the operation of the television receiver shown in FIGURE 2.

Figure 12 is a partial block diagram of an alternative embodiment, using one tuner, of the receiver shown in FIGURE 2.

A pix-in-pix television receiver provides the soundless picture of an auxiliary program inset into the picture of the main program. In the embodiment described below, the auxiliary picture is composed of every fourth sample of every fourth line of one field from each frame of the auxiliary signal. This auxiliary picture is displayed twice during a frame time, once for each field of the main picture. In this embodiment, the inset picture occupies one-sixteenth of the main picture area and is positioned at the bottom of the main picture as shown in FIGURE 1.

A particular advantage of this embodiment of the invention is its ability to work on time-division multiplexed main and auxiliary signals. Two separate tuner circuits may be used to develop the main and auxiliary signals although the use of only one tuner is also described herein below. These signals are applied to a two-input analog switch which is controlled by signals developed from the auxiliary signal to time-division multiplex the two signals. This switch provides auxiliary signals for every fourth line of every other field of the auxiliary image. These signals are provided from a time just prior to the leading edge of the horizontal sync pulse for a given line to a time just subsequent to the end of active video on that line. This embodiment of the invention uses a microprocessor to control the analog switch as well as to control other switches in the system which direct the auxiliary and main signals along their respective paths. All of these switches are desirably closely synchronized to each other and to the auxiliary signal to minimize contamination of the signals by switching artifacts. In the present embodiment, the microprocessor synchronizes itself by monitoring the auxiliary signal for at least one frame time prior to generating a display and by periodically monitoring the timing of the horizontal sync pulses as the main and auxiliary images are displayed.

The auxiliary signal is processed through a subset of the luminance and chrominance signal processing circuitry used to process the main signal. This subset provides auxiliary luminance and color difference signals which may have a narrower bandwidth than the main channel signals but which are acceptable for the reduced-size auxiliary image.

Subsequent to this processing, auxiliary channel luminance and chrominance signals are stored in a memory for later display. The luminance signals, which had been sampled at a rate equal to four times the color burst frequency (4 f_{sc}), are stored at one-quarter of this rate (f_{sc}). Similarly, the chrominance signals which had been sampled at an f_{sc} rate are stored at a $\frac{1}{4}$ f_{sc} rate.

Since the main channel signal is time-division multiplexed with the auxiliary channel signal, the processing of the signals is also time-division multiplexed. The signal processing circuitry provides main channel luminance and color difference signals during three horizontal line periods and auxiliary channel signals during one horizontal line period. However, since the auxiliary picture is displayed as an inset in the main picture, main channel information must be displayed on at least a portion of every horizontal line. Accordingly, in the present embodiment, as each line of the main signal is processed, it is stored in a 1H memory. When an auxiliary line is processed, the contents of this 1H memory are read for display (i.e. the preceding line is displayed again).

The exemplary embodiment that is generally described above is described in more detail below. This embodiment of the invention is in the context of a digital television receiver. It is noted, however, that the invention may also be practiced in analog form.

In the drawings, broad arrows represent busses for parallel multiple-bit digital signals. Line arrows represent connections carrying analog signals or single-bit digital signals. A device having a small circle at its input terminal responds to the logical complement of the signal applied to that terminal. Depending on the processing speed of the devices, compensating delays may be required in certain of the signal paths, but one skilled in the art of circuit design would know where such delays would be needed in his particular system.

In FIGURE 2 the main and auxiliary signals are received via antenna 16 and applied to signal splitter 18. Splitter 18 provides input signals to tuner IF amplifier and demodulator circuits 22 and 24. The signal selected by the tuner of either one of the circuits 22 or 24 is converted to an intermediate frequency signal by the tuner portion of the circuit and amplified by the IF amplifier portion. This amplified IF signal is applied to the detector portion of the circuit which provides baseband composite video signals at the output terminal of the circuit.

The signal selected by the tuner of circuit 22 is the main signal and the signal selected by the tuner of circuit 24 is the auxiliary signal. Splitter 18 prevents these signals from interfering with each other. In the present embodiment circuits 22 and 24 each include a digitally controllable tuner such as, for example, the one disclosed in U.S. Patent US-A-4,385,315 entitled "Phase Locked Loop Tuning Control system including A Timed Sync Ac-

tivated AFT Signal Seeking Arrangement" issued in the names of George et al.

Signal frequencies (i.e. channels) are selected for the tuners by channel selector 10. Channel selector 10 includes, for example, a calculator-like keyboard for generating, from operator input, two sets of binary coded decimal (BCD) signals, one for each of the tuners 22 and 24. These BCD signals are applied to the tuners via a bus from selector 10. Channel selector 10 also provides a signal, NC, to microprocessor 12 that indicates when a new auxiliary channel has been selected. This signal starts an initialization sequence in the microprocessor which determines the timing of the auxiliary channel horizontal and vertical sync signals.

Circuit 22 provides main channel composite video signals to one signal input terminal of analog switch 14. Auxiliary channel signals are applied to the other signal input terminal of switch 14 by circuit 24. Analog switch 14 is controlled by a single bit digital input signal, MA_1, from microprocessor 12. This signal is set to a logic high state to condition the switch 14 to pass main channel signals and to a logic low state to condition the switch to pass auxiliary channel signals. Microprocessor 12, based on the timing information it has collected, changes this signal to a logic low state at a time immediately prior to the leading edge of the horizontal sync pulse of the auxiliary signal for every fourth line in every other field of the auxiliary image. At the end of the active video portion of each of these auxiliary lines, the microprocessor conditions the analog switch 14 to pass the main channel signal by placing MA_1 into a logic high state. Consequently, switch 14 passes the auxiliary signal for one out of every four lines in one field, passing three out of every four lines of the main signal for that field and every line of the main signal for the next subsequent field.

In order to synchronize the analog switch 14 to the auxiliary input signal, microprocessor 12 monitors the vertical and horizontal sync pulses of the auxiliary signal. These sync pulses are supplied to the microprocessor by auxiliary sync separator 26. Auxiliary channel composite video signals are applied to the input terminal of sync separator 26 by tuner IF and demodulator circuit 24. Sync separator 26 may be a conventional analog circuit which provides three signals VS_A, HS_A and BG_A; the vertical sync, horizontal sync and burst gate signals respectively for the auxiliary channel signals. The vertical and horizontal sync signals are applied to microprocessor 12.

The main channel composite video signals from circuit 22 are applied to the main sync separation circuit 28. This circuit may be identical to sync separator 26. Sync separator 28 provides three output signals, HS_M, VS_M and BG_M, the main channel horizontal sync, vertical sync and burst gate signals respectively. These signals are used at various stages of signal processing as described below.

The time-division multiplexed main and auxiliary channel composite video signals from analog switch 14 are applied to analog to digital (A/D) converter 34. A/D converter 34, which may be, for example, an 8 bit flash-type converter, provides digital samples at a $4f_{sc}$ rate. The clock signal for the A/D converter is developed by phase locked loop (PLL) 30. PLL 30 may be a known circuit, for example, the loop disclosed in U.S. Patent US-A-4,291,332 entitled "Phase-Locked Circuit" and issued in the names of Kato et al. Digital samples of composite video signals from A/D converter 34 are applied to one input of PLL 30. The phase locked loop 30 uses the burst component of these signals to lock a voltage controlled oscillator to a frequency four times the burst frequency ($4f_{sc}$). The burst component is separated from the composite video signals in a conventional manner by the burst gate signal applied to PLL 30 via AND gate 29. This burst gate signal is available to the PLL only during the burst interval of the main channel signal. AND gate 29 which has the main channel burst gate signal, BG_M, and the main/auxiliary control signal, MA_1, applied to its input terminals, provides the main channel burst gate pulse only when main channel burst component is being passed through A/D converter 34. AND gate 29 prevents PLL 30 from attempting to lock to the auxiliary channel burst.

It is noted that a phase locked clock signal is not a necessary part of this invention. It is contemplated that a suitably accurate free-running oscillator operating at $4f_{sc}$ can also be used with the disclosed apparatus.

The $4f_{sc}$ clock signal from PLL 30, the main and auxiliary burst gate signals from sync separators 28 and 26 respectively, and the composite video samples from A/D converter 34 are applied to the main/auxiliary signal processor 40. Processor 40 is controlled by microprocessor 12 via control bus SPCON. A data bus, SPD, connects processor 40 and microprocessor 12, to provide a data exchange channel between the two devices. Processor 40 converts the time-division multiplexed composite video samples into main channel luminance and R-Y and B-Y color difference signals available at output ports Y_M, $(R\text{-}Y)_M$ and $(B\text{-}Y)_M$ respectively, and into auxiliary channel luminance and color difference signals available at output ports Y_A, $(R\text{-}Y)_A$ and $(B\text{-}Y)_A$ respectively.

FIGURE 3 is a block diagram representation of the main/auxiliary signal processor 40 used in FIGURE 2. To simplify explanation, the main channel

signal processing steps of this processor are described first.

Time-division multiplexed composite video samples from A/D converter 34 are applied to comb filter 310 via bus CV. Comb filter 310 is controlled by the output signal of AND gate 390 to act only on main channel samples. The inputs to gate 390 are a single bit digital control signal, MA_2, from microprocessor 12 and the $4f_{sc}$ system clock signal from PLL 30. Signal MA_2 is a delayed replica of the main/auxiliary control signal MA_1. MA_2 is in a logic high state when main channel samples are available on bus CV and in a logic low state otherwise. Consequently, AND gate 390 provides a clock signal to comb filter 310 only when main channel samples are to be processed. Microprocessor 12 also provides control signals directly to comb filter 310 via bus SPCON.

Comb filter 310 is shown in detail in FIGURE 4. Composite video samples are applied to shift register 410 via bus CV. Shift register 410 delays these samples by one horizontal line period (1H) and applies them to the input of shift register 412 via bus CV_1. Shift register 412 further delays the samples by 1H, providing output samples via bus CV_2.

Samples from bus CV are applied to the multiplicand input terminals of sample weighting circuits W_1 and W_4. Similarly, samples from bus CV_1 are applied to the multiplicand input terminals of sample weighting circuits W_2 and W_5 and samples from bus CV_2 are applied to the multiplicand input terminals of sample weighting circuits W_3 and W_6. The multiplier inputs to sample weighting circuits W_1 through W_3 are weighting factors of $\frac{1}{2}$ or $\frac{1}{4}$ which are applied to the individual weighting circuits via bus SPCON from microprocessor 12 of FIGURE 2. Similarly, sample weighting circuits W_4 through W_6 have weighting factors of $\frac{1}{2}$ or $-\frac{1}{4}$ applied by microprocessor 12.

The scaled samples provided by the weighting circuits W_1, W_2 and W_3 are summed by adder 420 to generate a luminance signal Y. Samples from weighting circuits W_4, W_5 and W_6 are summed by adder 430 to provide a chrominance signal C.

The value of the weighting factor applied to each of the sample weighting circuits W_1 through W_6 changes as each new line of video signal is applied to input bus CV. FIGURE 5 is a table which shows the sequence of change of these weighting factors. The top row of the table shows the lines of the main channel signal that are available on the busses CV, CV_1 and CV_2 as six consecutive horizontal lines are processed. In the first column of the table, lines L1 and L2 have been stored in shift registers 412 and 410 respectively and line L3 is being received. Consequently, line L3 is available via bus CV, line L2 via bus CV_1 and line L1 via bus CV_2.

The last two rows of the table show the weighting factors that are applied to the corresponding lines, listed in the first row of the table, to obtain combed luminance, Y, and combed chrominance, C. The factors listed in the first column of the table are for the three consecutive lines of composite video signal L3, L2 and L1. In the NTSC system lines L1 and L3 have the same chrominance phase. The chrominance phase of line L2 is opposite to that of lines L1 and L3. The samples of lines L1 and L3 are respectively scaled in sample weighting circuits W_1 and W_3 by $\frac{1}{4}$, and the samples of line L2 are scaled by $\frac{1}{2}$ in weighting circuit W_2. Due to the respective chrominance phases of the signals, the chrominance components of these samples cancel when they are summed, leaving comb filtered luminance samples at the output of adder 420. The samples of lines L1 and L3 are respectively scaled by $-\frac{1}{4}$ in sample weighting circuits W_4 and W_6, and the samples of line L2 are scaled by $\frac{1}{2}$ in weighting circuit W_5. Summing these scaled samples substantially cancels the luminance component leaving comb filtered chrominance at the otuput of adder 430. Those skilled in the art will recognize that for three consecutive lines available on busses CV, CV_1 and CV_2, the apparatus of FIGURE 4 is configured as a conventional 2H comb filter.

The second column of the table shows the state of the comb filter one line later. Lines L2 and L3 are now stored in shift registers 412 and 410 respectively and a line from the auxiliary channel is being received. Since the auxiliary signal is on bus CV, the main/auxiliary control signal MA_2 will be in a low logic state. Accordingly, the clock signal to the comb filter will be disabled by AND gate 390 shown in FIGURE 3. Without a clock signal, no samples progress through the shift registers 410 and 412 so the weighting factors applied to the sample weighting circuits W_1 through W_6 are immaterial.

The third column of the table is one horizontal line period after the second column. The samples for main channel lines L2 and L3 are in shift registers 412 and 410 respectively and samples for line L5 are being applied via bus CV. In this instance, the weighting factors applied via W_1 through W_6 configure the comb filter to operate as if line L2 had been received after line L3 but before line L5.

The comb weighting factors change again one horizontal line period later, as represented by the fourth column of the table. The shift registers 410 and 412 now provide lines L5 and L3 respectively while line L6 is being received. In this instance, the weighting factors are selected to configure the apparatus to operate as a 2H comb filter in which line L6 is presumed to lie, in time, between lines L3

and L5. System operation for columns 5 and 6 of the table is the same as for columns 1 and 2 but with a different set of lines.

Returning to FIGURE 3, the chrominance samples from comb filter 310 are applied to one input terminal of multiplexer 340 via bus C. The other input terminal of multiplexer 340 is coupled to bus CV. Multiplexer 340 is controlled by signal MA_2 from microprocessor 12 of FIGURE 2 to provide the chrominance samples from comb filter 310 during main channel processing and to provide the auxiliary composite video samples from bus CV during auxiliary channel processing.

The samples provided by multiplexer 340 are applied to low-pass filter 350. For main channel processing, this filter produces samples representing the luminance vertical detail information that is included in the combed chrominance samples. These vertical detail samples are added to the luminance samples from comb filter 310 by adder 320. The main channel luminance samples from adder 320 are applied to peaking filter 330 which increases the amplitude of high frequency components of the samples relative to their low frequency components. These samples are provided to the rest of the system through output port Y_M of main/auxiliary signal processor 40.

Combed chrominance samples from multiplexer 340 are also applied to delay element 352 which compensates for the processing delay through low-pass filter 350. The vertical detail samples, derived from the combed chrominance samples by low-pass filter 350, are subtracted from the delayed combed chrominance samples provided by delay element 352 in subtracter 360. The chrominance samples from subtracter 360 are filtered by band-pass filter 370 which rejects frequencies outside of the chrominance signal band to remove residual luminance signal components. These chrominance samples are applied to chroma processor 380 which produces main channel R-Y and B-Y color difference signals.

As stated above, the signal processing circuitry used for the auxiliary signal is a subset of that used for the main signal. During auxiliary signal processing, control signal MA_2 causes multiplexer 340 to pass the composite video samples on bus CV to low-pass filter 350. Low-pass filter 350 removes the high frequency components, including the modulated chrominance subcarrier, from the composite video samples applied to it and so provides samples representing auxiliary channel luminance. These samples are available at output port Y_A of processor 40.

The auxiliary channel luminance samples are subtracted from delayed composite video samples from bus CV in subtracter 360. The delayed composite video samples are provided to subtracter 360 by delay element 352 which delays samples from multiplexer 340 by an amount of time sufficient to compensate for the processing delay of low-pass filter 350. The samples provided by subtracter 360 are effectively high-pass filtered composite video samples. These samples are applied to band-pass filter 370 which removes residual luminance components and provides auxiliary channel chrominance samples to chroma processor 380.

Chrominance samples from both the main and auxiliary channels are applied to chroma processor 380 at the $4f_{sc}$ clock rate. It can be shown that these samples occur at 90° phase intervals of the chrominance subcarrier and so represent alternating values of two quadrature phase related color difference signals. For example, if the samples from the main channel occur at phases representing the R-Y and B-Y color difference signals, the sequence of main channel samples provided to chroma processor 380 is +(R-Y), +(B-Y), -(R-Y), -(B-Y), +(R-Y) . . . etc. where the signs of the samples indicate sampling phase, not sample polarity. Because of signal processing delays, there may be phase errors between the samples provided to processor 380 and the R-Y and B-Y phases of the main or auxiliary channel signals. Moreover, since the auxiliary channel signals are not synchronized to the main channel signal, there may be different R-Y and B-Y reference phases for the two channels. Chroma processor 380 corrects these phase errors, providing R-Y and B-Y color difference signal samples for both the main and auxiliary channels at its output ports.

Chroma processor 380 is generally described in U.S. Patent US-A-4558348 entitled "A Digital Video Signal Processing System Using Asynchronous A-to-D Encoding", published on October 12, 1985. The following is a description of an adaptation of this circuit for use in the present invention. To simplify the description both the main and auxiliary channel samples provided to chroma processor 380 are referred to as $(R-Y)_S$ and $(B-Y)_S$ where the subscript S indicates that there is a phase error between the sample and the true R-Y and B-Y samples respectively.

Chrominance samples from band-pass filter 370 of FIGURE 3 are applied to demultiplexer 600 in FIGURE 6. The bandwidth of the information contained in the chrominance samples is less than 1.5 MHz. The $(R-Y)_S$ and $(B-Y)_S$ samples respectively occur at twice the subcarrier rate, e.g. 7.16 MHz for an NTSC signal The Nyquist sampling criterion may, therefore, be satisfied if alternate $(R-Y)_S$ and alternate $(B-Y)_S$ samples are processed. The demultiplexer 600 in FIGURE 6 will be assumed to provide only the $+(R-Y)_S$ and $+(B-Y)_S$ samples from recurring chrominance sequences

$+(R\text{-}Y)_S$, $+(B\text{-}Y)_S$, $-(R\text{-}Y)_S$, $-(B\text{-}Y)_S$, $+(R\text{-}Y)_S$...etc.

In FIGURE 6 the $(R\text{-}Y)_S$ and $(B\text{-}Y)_S$ digital signals are applied by demultiplexer 600 to busses 610 and 620. These signals are respectively applied to absolute value circuits 650 and 651 which pass the magnitudes of the $(R\text{-}Y)_S$ and $(B\text{-}Y)_S$ signals. The magnitudes of $(R\text{-}Y)_S$ and $(B\text{-}Y)_S$ are applied as address codes to ROM's 653 and 654 which are programmed to produce the logarithms of the address codes applied to their respective address input ports. The signal corresponding to the log $|(R\text{-}Y)_S|$ is subtracted from the signal corresponding to the log $|(B\text{-}Y)_S|$ in subtracter 655 which produces output signal codes corresponding to log $(|(B\text{-}Y)|_S/|(R\text{-}Y)_S|)$. These signal codes are applied along with the sign bits of signals $(R\text{-}Y)_S$ and $(B\text{-}Y)_S$, applied via delay elements 652 and 656 respectively, as input address codes to ROM 657 (the $(R\text{-}Y)_S$ and $(B\text{-}Y)_S$ sign bits being the most significant bits of the composite address code). ROM 657 is programmed to produce output codes corresponding to the arctangent $((B\text{-}Y)_S/(R\text{-}Y)_S)$, i.e., angles θs which are applied to adder 658. Since the codes produced by subtracter 655 were generated from the magnitudes $|(R\text{-}Y)_S|$and $|(B\text{-}Y)_S|$, they only represent the range of angles from zero to 90 degrees where zero degrees is defined along the $+(R\text{-}Y)_S$ axis. The $(R\text{-}Y)_S$ and $(B\text{-}Y)_S$ sign bits added to the address codes applied to ROM 657, provide the information needed to expand the angle information from zero to 360 degrees or from zero to ±180 degrees.

The angle codes produced by ROM 657 are also applied to the phase error detector 672. The phase error detector - which will be described with reference to FIGURE 7 - under control of the burst gate signals, examines the angle codes representing the chrominance phase angle during the burst intervals of the main and auxiliary signals. Circuit 672 calculates the difference, α, between the phase angles represented by the $(R\text{-}Y)_S$ and $(B\text{-}Y)_S$ samples of the main and auxiliary burst signals and the phase angles that would be produced were the samples taken in phase with the desired or correct axes R-Y and B-Y. The angles, α, for the main and auxiliary signals are stored until the next burst interval and are applied to adder circuit 658, when appropriate, during the period between burst intervals. Adder circuit 658 sums the angles θs and α to produce corrected angles θ'.

Digital codes corresponding to angle θ' from ADDER 658 are applied to circuit 671 which produces flesh corrected digital codes corresponding to angles ϕ. Circuit 671 may be a ROM programmed to provide a non-linear transfer function which produces flesh corrected angles ϕ for angles θ' - representing chrominance angles normally associated with flesh colors - applied as address codes. For angles θ', which do not represent chrominance angles in the range of flesh colors, the angles ϕ produced by circuit 671 equal the angles θ'. For example, ROM 671 may be programmed to generate angles ϕ equal to $(\theta'\text{-K sin } 2\theta')$ for angles θ' equal to ±90 degrees and angles ϕ equal to angles θ' for angles θ from ±90 degrees to ±180 degrees.

Angles ϕ from circuit 671 are applied as address codes directly to ROM 678 programmed to produce the sines and cosines of angles ϕ. The sines and cosines are then multiplied by the magnitude value, C_B, of the vector sum of $(R\text{-}Y)_S$ and $(B\text{-}Y)_S$, to produce flesh tone corrected quadrature signals R-Y and B-Y.

The magnitude, C_B of the vector sum of $(R\text{-}Y)_S$ and $(B\text{-}Y)_S$ in the FIGURE 6 embodiment is generated according to the equation

$$C_B = |(R\text{-}Y)_S|/|\cos\theta s|. \quad (1)$$

To this end the angles θs from elements 657 are applied as address codes to a ROM 659 which is programmed to produce the log $|\cos\theta s|$ of the angle θs signal codes applied to its address input. The log $|\cos\theta s|$ codewords from ROM 659 are applied to one input port of a subtracter circuit 660 wherein they are subtracted from the log $|(R\text{-}Y)_S|$codewords from ROM 653 to produce a signal corresponding to log $(|(R\text{-}Y)_S|/|\cos\theta s|)$. This signal is applied to ADDER 670 and ACC latch 662. Automatic Chrominance Control (ACC) is performed by microprocessor 12 of FIGURE 2 which periodically calculates the products G=ACC·Sat equal to the products of the ACC control signal and the saturation control signal.

Microprocessor 12 periodically reads the contents of the latch 662 via data bus SPD. These values may be read, for example, during the main and auxiliary channel color burst intervals. The microprocessor compares the read values against a predetermined reference value, e.g. 20 IRE and generates the logarithms of the composite gain factors G_M and G_A for the main and auxiliary signals respectively. These gain factors are provided to buffers 666 and 667 respectively via bus SPD. From buffers 666 and 667 the gain factors are applied to ADDER 670 by multiplexer 669 where they are added to the log $(|(R\text{-}Y)_S|/|\cos\theta s|)$ signal to produce signal samples corresponding to log (GC_B). These samples or codewords are applied to adder 679 where they are combined with the log $(\cos\phi)$ signals.

Multiplexer 669 is controlled by the main/auxiliary control signal MA_2 from microprocessor 12. The signal MA_2 selects the gain factor from latch 666 when main channel chrominance samples are being processed and from latch 667

when auxiliary channel samples are being processed.

The signal generator for developing the timing signals applied to the FIGURE 6 circuitry is not shown because it is not considered part of this invention. These signals may be developed by conventional techniques which are known by those skilled in the art.

FIGURE 7 shows exemplary circuitry for developing the phase angle error signals α. In FIGURE 7, angle values θs are applied to an accumulator 712 under the control of a burst gate signal. The burst gate signal applied to the accumulator is either the main channel burst gate signal, BG_M, from sync separator 28 or the auxiliary channel burst gate signal, BG_A, from sync separator 26. The main channel burst gate signal, BG_M, is applied to one input terminal of multiplexer 706 and the auxiliary channel burst gate signal, BG_A, is applied to its other input terminal. Multiplexer 706 is controlled by main/auxiliary control signal MA_2 to provide the main channel burst signal during main channel signal processing and the auxiliary channel burst signal during auxiliary channel signal processing. Counter 710 is reset by the leading transition of the burst gate pulse from multiplexer 706. Counter 710, responsive to the reset pulse, produces an enabling output potential which is applied to accumulator 712. An f_{sc} clock signal, synchronous with the occurrence of angle values θs, is applied to the clock input of the counter. The counter effectively counts a prescribed number, e.g. M, of the f_{sc} clock signals. After the prescribed number of clock pulses have occurred, the output potential of the counter changes to a potential value which disables accumulator 712. The enabling signal from counter 710 is of such duration to permit M consecutive angle values from circuit 657 to be input to the accumulator 712 during the burst interval. The M angle values will nominally be selected from the center of the burst sequence of reference cycles. Accumulator 712 sums the applied burst phasor angle values. The accumulator may consist of an adder and a latch (not shown). The respective inputs of the adder are coupled to the output of the latch and the input of the accumulator. The output of the adder is coupled to the output of the accumulator and the input of the latch. In operation, each successive sum from the adder is input to the latch from which it is available to be added to the next input value.

The output sum from the accumulator is applied to the latch 716 at the end of the burst interval by the complement of the burst gate signal. More particularly, the burst gate signal is applied to the inverter 714 which inverts the signal. The falling or trailing edge of the burst gate pulse is converted to a rising potential transition at the output terminal of inverter 714. Latch 716, in response to the rising transition of the inverted burst gate pulse, stores the value currently applied to its input port. This value is stored for one line period or until the termination of the next subsequent burst gate pulse.

The output of the latch 716 is applied to the divider circuit 718 which divides the applied value by M to produce an average value of the angle θs. It will be appreciated by those skilled in the art of digital signal processing that divider circuit 718 may be positioned to preceed latch 716. Further, if the value M is an integral power of two the divider 718 may be eliminated and division may be accomplished by shifting the bits of the PCM codeword rightward to lesser significant bit positions.

The output value from divider circuit 718 is applied as subtrahend to subtractor circuit 721 and a reference angle value, e.g. 0 degrees, from source 720 is applied as minuend to subtractor circuit 721. Subtractor 721 produces a difference value corresponding to the angle α and which is equal to the reference angle minus the average value of θs determined over the burst interval. This difference value is applied to the input terminal of demultiplexer 722, which under control of signal MA_2 from microprocessor 12 applies main channel values to latch 726 and auxiliary channel values to latch 724. Latches 726 and 724 respectively retain the last difference value calculated for the main channel while auxiliary channel samples are processed and the last value calculated for the auxiliary channel while main channel samples are processed. The output terminals of these latches are connected to the input terminals of multiplexer 728 which provides the main channel α value to adder 658 of FIGURE 6 during main channel signal processing and provides the auxiliary channel α value during auxiliary channel processing. Multiplexer 728 is controlled by signal MA_2 from microprocessor 12.

If the correction angles α change significantly from line-to-line, the value α applied to adder 658 will be substantially in error towards the end of respective line intervals. System performance may be enhanced by incrementing/decrementing the value α for the main or auxiliary signals proportional to the change of the value of the respective α between preceding lines. For example, if the last-most angle α for the auxiliary channel increased by four degrees over the preceding auxiliary α value, it may be anticipated that the nextmost value of α for the auxiliary channel will also be increased by four degrees over the present value. System performance may be enhanced if the value of α is successively increased by one degree at quarter line intervals so that, at most, the anticipated error

in α will be only one degree. More or less, corrections to α can be made over the line interval as desired. Apparatus to correct the value of α at intervals of less than one horizontal line is not shown since it is not considered part of the present invention. One skilled in the art can readily adapt the circuitry shown in FIGURE 7 to implement this method of phase angle correction if the phase shift across a single horizontal line is deemed excessive.

Returning to FIGURE 2, the auxiliary channel luminance and color difference samples provided by processor 40 at output ports Y_A, $(R\text{-}Y)_A$ and $(B\text{-}Y)_A$ are applied to auxiliary memory 50. Memory 50, under the control of signal MA_3 from microprocessor 12, stores every fourth sample of the luminance signal and every fourth sample of each of the R-Y and B-Y color difference signals for a sufficient number of lines to reproduce the auxiliary image (e.g. 64 for NTSC). Control signal MA_3 is a delayed replica of signal MA_2. It is in a logic low state only when auxiliary channel samples are available at ports. Y_A, $(R\text{-}Y)_A$ and $(B\text{-}Y)_A$.

The lines of samples are retrieved from the memory to be displayed as an inset in the main picture. Luminance and color difference signal samples are read from the memory at four times their input rate to produce auxiliary picture lines that are one-quarter the length of the lines of the main picture The reading of the contents of auxiliary memory 50 is controlled by signal S_M from multiplexer control circuit 60

Auxiliary channel signal processing and, so the writing of data into the auxiliary memory 50, is synchronized to the auxiliary signal However, the reading of data from the auxiliary memory 50 for display is synchronized to the main channel signal. Since the auxiliary and main channel signals are asynchronous and since auxiliary channel signals may be processed as the auxiliary image is displayed, there may be times when memory 50 is accessed both to write and to read data. To prevent data corruption due to simultaneous read and write access, the auxiliary memory 50 includes two stages: a buffer for receiving processed auxiliary data and a random access memory (RAM) for storing the data to be displayed. The writing of data into the buffer is synchronized to the auxiliary signal while transfers between the buffer and the RAM and the reading of data from the RAM are synchronized to the main signal. In the present embodiment, samples are loaded into the buffer at one-quarter the rate at which they are supplied by processor 44. This results in a four-to-one compression of the auxiliary image lines. Samples are transferred from the buffer to the RAM at four times this buffer storage rate. All transfers occur coincident with the leading edge of the second main channel horizontal sync pulse following each auxiliary signal processing interval. The transfers are complete one-quarter of a horizontal line period later. There is no interference between the transfers and the reading of the auxiliary memory which, as explained below, starts after three-eighths of a main channel line has been displayed.

FIGURE 8A is a block diagram of the part of the auxiliary memory 50 in which luminance samples are stored. Buffer 800, which may be a 228 x 8 first-in-first-out (FIFO) register, has an input port connected to the output port Y_A of signal processor 40, an output port connected to the input port of RAM 820, a shift-in control terminal, SI, and a shift-out control terminal, SO. Data is written into the buffer when pulses are applied to terminal SI and data is read from the buffer when pulses are applied to terminal SO.

The shift-in pulses applied to terminal SI are developed from an f_{sc} clock signal and the main/auxiliary control signal MA_3 from microprocessor 12. MA_3 is applied to inverter 801 which provides an input signal to AND gate 803. The other input to AND gate 803 is provided by clock signal f_{sc}. The output signal of gate 803 is an f_{sc} clock signal when MA_3 is in a logic low state, i.e. when auxiliary channel luminance samples are available at output port Y_A of processor 40, and a logic low signal otherwise. This output signal is applied to terminal SI of buffer 800 and conditions the buffer to store every fourth one of the auxiliary luminance samples provided by processor 40.

Data transfer from the buffer to the RAM occurs while main channel lines are being processed. Transfers occur during only one of the two fields that make up an auxiliary frame since auxiliary channel lines are processed during only one of the two fields. The transfer pulses are generated from signals MA_3; VS_A, the auxiliary channel vertical sync signal from auxiliary sync separator 26; HS_M, the main channel horizontal sync signal from the main channel sync separator 28; and the $4f_{sc}$ clock signal from PLL 30.

Transfer pulses are developed by AND gate 802. These pulses are applied to counter 804, which develops write addresses that are applied to RAM 820 via multiplexer 806. The counter is reset to zero by the auxiliary channel vertical sync pulses applied to its reset input.

The transfer pulses from AND gate 802 are applied, through delay element 808, to the shift-out terminal, SO, of buffer 800 and to the write enable terminal WE of RAM 820. These pulses condition the buffer to provide data at its output and condition the RAM to write the data into the addressed cells. Delay element 808 delays the transfer pulses a sufficient time to allow the write addresses to stabilize in the RAM.

One input terminal of AND gate 802 is coupled to receive a $4f_{sc}$ clock signal. This signal controls the rate at which the data are transferred; the other signals applied to AND gate 802 control when the transfer occurs. Signal MA_3 is applied to one input terminal of AND gate 802 to prevent it from developing transfer pulses when data is being written into buffer 800. The inverse of signal MA_3 from inverter 801 is applied to the set input (S) of RS flip-flop 805 and the auxiliary channel vertical sync signal, VS_A, is applied to the reset input (R). Flip-flop 805 is reset at the end of each auxiliary field and set as the first auxiliary channel line of a given field is processed. The output signal of flip-flop 805 is applied to AND gate 802 to prevent the gate from developing transfer pulses during fields for which no auxiliary signal lines are processed.

The last input to AND gate 802 controls the position in the main channel horizontal line period, at which a transfer occurs. Frequency divider 807, which may be a conventional divide by two circuit, has the main channel horizontal sync signal, HS_M, applied to its signal input terminal and the inverted main/auxiliary control signal, MA_3, applied to its reset input terminal. Consequently, divider 807 produces a logic low state while auxiliary channel data is being written into the buffer 800. This signal changes to a logic high state with the leading edge of the first main channel horizontal sync pulse subsequent to auxiliary signal processing. The next main channel horizontal sync pulse changes the output signal of the divider 807 to a logic low state. This output signal is applied to the reset input terminal of 8 bit counter 813.

Counter 813 has a $4f_{sc}$ clock signal from AND gate 811 applied to its signal input terminal. The 8 bit output signal of counter 813 is applied to decoder 815. Decoder 815 produces a signal having a logic high state when the value supplied by the counter is 228. The output signal from decoder 815 is applied to inverter 817 which provides one input to AND gate 811. The other input to gate 811 is the $4f_{sc}$ clock signal. AND gate 811 provides the $4f_{sc}$ clock signal to counter 813 from the time the counter is reset until 228 pulses have been counted. The circuit formed by divider 807, AND gate 811, counter 813, decoder 815 and inverter 817 provides a signal, available at the output of inverter 817, which has a logic high state starting at a point in time coincident with the leading edge of the second horizontal sync pulse following auxiliary signal processing, and remaining in a logic high state for 228 pulses of the $4f_{sc}$ clock ($\frac{1}{2}$ H). This signal is applied to an input of AND gate 802 to condition the gate to provide 228 transfer pulses during each of these intervals.

The reading of samples from the RAM 820 is controlled by the $4f_{sc}$ clock signal, the select signal, S_M, from multiplexer control circuit 60 and the main channel vertical sync signal VS_M from main sync separator 28. The select signal SM and the $4f_{sc}$ clock signal are applied to AND gate 812. Consequently, AND gate 812 produces a $4f_{sc}$ clock signal when multiplexer control circuit 60 selects auxiliary channel samples for display. Multiplexer control circuit 60 is described in more detail below. The signal provided by AND gate 812 is applied to counter 814 and to delay element 818. Counter 814 develops the read addresses that are applied to RAM 820 via multiplexer 806. Multiplexer 806 is controlled by signal SM to provide read addresses from counter 814 when auxiliary channel samples are selected for display and to provide write addresses from counter 804 otherwise. Main channel vertical sync pulses VS_M are applied to the reset input of counter 814 to return the read addresses to a starting point at the end of each main channel field.

Delay element 818 delays the read pulses applied to its input by AND gate 812 by a time sufficient to allow the read addresses to stabilize in the RAM. These delayed pulses are applied to the read enable input of RAM 820 to condition the RAM to provide the digital samples from the addressed cells at its output port Y_A'.

The portions of memory 50 which store the two sampled color difference signals are identical, so only one is shown in FIGURE 8B. This memory is essentially the same as the luminance sample memory shown in FIGURE 8A. The only differences are the frequencies of the clock signals and the number of cells in the buffer and RAM. An f_{sc} clock signal is applied to one input of gate 861 of FIGURE 8B instead of the $4f_{sc}$ signal applied to gate 811 of FIGURE 8A and an $f_{sc}/4$ clock signal is applied to one input of gate 853 of FIGURE 8B instead of the f_{sc} signalapplied to gate 803 of FIGURE 8A. Reduced rate clock signals are used because of the lower data rate of the color difference signals relative to the luminance signal. In addition, a smaller buffer containing 57 instead of 228 cells, is used to store the color difference samples provided by processor 40. A proportionally smaller RAM is also used for the color difference samples than is used for the luminance samples. Otherwise, the memories shown in FIGURES 8A and 8B are identical. The apparatus used to develop the clock signals f_{sc} and $f_{sc}/4$ is not shown since it is not considered a part of the invention. These signals may be developed by conventional techniques which are known to those skilled in the art.

The luminance and color difference samples from the output ports Y_A', $(R\text{-}Y)_A'$ and $(B\text{-}Y)_A'$ of auxiliary memory 50 are applied to one set of inputs of the main/auxiliary signal multiplexer 52.

Another set of inputs to multiplexer 52 are main channel luminance and color difference samples from the output ports Y_M, $(R-Y)_M$ and $(B-Y)_M$ of signal processor 40. The third set of input signals applied to multiplexer 52 are provided by the Y'_M,$(R-Y)'_M$ and $(B-Y)'_M$ output ports of main memory 70.

Main memory 70 includes three 1H shift registers, one each for the luminance, R-Y and B-Y color difference signals of the main channel. Luminance samples from output port Y_M of processor 40 are applied to the input port of 1H shift register 900 shown in FIGURE 9A. Register 900 may be a conventional shift register containing a sufficient number of stages to store one horizontal line of samples provided at a $4f_{sc}$ rate (e.g. 910 stages for NTSC). Samples available at the output port Y'_M of shift register 900 are main channel luminance samples delayed by one line period.

FIGURE 9B is a block diagram of one of the two color difference signal memories of main memory 70. These memories are also 1H shift registers, however, because of the lower sample rate of the digital color difference signals provided by processor 40, the shift registers 950 are clocked at a lower rate, f_{sc}, and contain fewer cells (e.g. 228 for NTSC).

The select signal, S_M, from multiplexer control circuit 60 and the main/auxiliary control signal, MA_4, from microprocessor 12 determine which of the three sets of luminance and color difference signals is provided at the output ports Y, (R-Y) and (B-Y) of multiplexer 52. Main/auxiliary control signal MA_4 switches the multiplexer between providing main channel samples from processor 40 or from main memory 70. Control signal MA_4 is generated by microprocessor 12; it has the same properties as signals MA_1 through MA_3 described above but is delayed with respect to these signals.

When MA_4 is in a logic high state, multiplexer 52 provides main channel samples from processor 40. However, when MA_4 is in a logic low state, i.e. when processor 40 is supplying auxiliary channel samples, multiplexer 52 provides samples from main memory 70.

The select signal S_M from multiplexer control circuit 60 switches the multiplexer between providing main and auxiliary channel samples. When S_M is in a logic low state, main channel samples from processor 40 or from memory 70 are provided by multiplexer 52. When S_M is in a logic high state multiplexer 52 provides auxiliary channel samples from auxiliary memory 50. The generation of S_M is described in more detail below, in reference to FIGURE 10.

The luminance signal from port Y and the color difference signals from ports (R-Y) and (B-Y) of multiplexer 52 are applied to the inputs of digital matrix 80 which combines the luminance and the R-Y and B-Y color difference signals to produce the three primary color signals, R, G and B which may be applied, for example, to a display device (not shown). A suitable digital matrix for use in the present embodiment can be assembled by one skilled in the art from conventional circuit elements. This circuitry is not shown because it is not considered part of this invention.

As stated above, the signal S_M which controls the unloading of auxiliary memory 50 and the routing of signals in multiplexer 52 is generated by multiplexer control circuit 60. The input signals applied to this circuit are the $4f_{sc}$ clock from PLL 30, and the delayed main channel horizontal and vertical sync pulses from main sync separator 28. These sync pulses are applied to delay elements 62 and 64 respectively which provide sufficient delay to synchronize these sync pulses to the processed luminance and color difference signals from processor 40. Control circuit 60 is not shown in detail because it is not considered part of the invention. It can be made from conventional components including counters and other logic by one skilled in the art with the aid of the timing diagram shown in FIGURE 10. In FIGURE 10, the waveforms labeled HS_M and VS_M represent the horizontal and vertical sync signals applied to control circuit 60. The waveform labeled Y_M represents the main channel luminance signal provided by processor 40. The waveform labeled S_M in FIGURE 10 represents the signal S_M produced by control circuit 60.

FIGURE 10 shows selected lines from one field and the first two lines from the subsequent field of an NTSC video signal. The numbers across the top of the figure represent the numbers of lines in the fields. FIGURE 10 also includes representations of the equalizing pulses and vertical synchronization pulses that occur between the fields.

The signal S_M consists of a series of pulses, each pulse being $\frac{1}{2}$ H wide and separated from the next pulse by a 3/4 H interval. If the auxiliary image is positioned at the bottom of the main image, as shown in FIGURE 1, the pulses occur only during lines 189 through 252, the last one-quarter of the lines of an NTSC field. When signal S_M is in a high logic state multiplexer 52 is conditioned to provide auxiliary channel samples to matrix 80 and main memory 70. When S_M is in a low logic state, however, the main channel samples from processor 40 are provided by multiplexer 52. The multiplexer 52 switches between supplying main and auxiliary channel samples to produce a composite main and auxiliary picture as shown in FIGURE 1.

Microprocessor 12 controls the main and auxiliary signal processing in this embodiment of the invention. FIGURE 11 is a flow diagram showing

the control sequence of the microprocessor 12. Block 1110 represents the initialization sequence of the microprocessor. The first step in block 1110 is to reset the main/auxiliary control signals MA_1 through MA_4. As stated above, these signals are set to a logic high state for main channel signal processing and reset to a logic low state for auxiliary channel processing. Signals MA_2through MA_4 are delayed with respect to MA_1 by different amounts, increasingly greater subscript values indicating increasingly greater delays. Each signal controls a different stage of the pipelined signal processing performed by the receiver. Accordingly, the step 'RESET MAs' resets MA_1, then MA_2, then MA_3 and then MA_4. The amount of delay between changing any two MA signals depends on the processing delay between the devices controlled by the signals. If the delay is an integral number of microprocessor instruction cycles then the signals can be changed by the microprocessor directly, otherwise the microprocessor may, for example, provide one signal to a three stage delay network (not shown) which provides the other three signals. Of course, the above also applies for any 'SET MAs' steps where each of the MA signals are changed from a low logic state to a high logic state.

The second step in the initialization block 1110 is to assign 0 to the variable ODDF. ODDF indicates whether the lines being processed are from an odd or even field (ODDF = 1 and ODDF = 0 respectively). This variable is used to ensure that auxiliary image lines are taken from every other field (i.e. from every odd field) of the auxiliary signal. The third initialization step resets the counters LTIME and FTIME to 0. Counters LTIME and FTIME may be internal to the microprocessor and incremented by one for each clock pulse. These counters hold the number of $4f_{sc}$ clock pulses that have occurred since the last horizontal sync pulse (LTIME) and since the last vertical sync pulse (FTIME). LTIME and FTIME are used by the microprocessor to synchronize the signals it provides with the auxiliary channel horizontal and vertical sync pulses respectively. In a microprocessor without accessible internal counters, LTIME and FTIME may be realized as functions of the $4f_{sc}$ system clock. FTIME, for example, may be the system clock minus a variable. In this situation, the program step that resets the counter FTIME would, instead, assign the current value of the system clock to the variable.

The fourth step in the initialization sequence is to monitor the auxiliary channel signal for at least one frame time to get an accurate estimate of the number of clock pulses between successive auxiliary channel horizontal sync pulses and between successive auxiliary channel vertical sync pulses. This may be accomplished by, for example, having the horizontal and vertical sync pulses from sync separator 26 activate different vectored interrupts. The interrupt subroutine which handles the particular interrupt may average its current value of HTIME, the time between auxiliary signal horizontal sync pulses, or VTIME, the time between auxiliary signal vertical sync pulses, with the difference between the values of the system clock for this interrupt and for the previous interrupt. This step in the initialization sequence monitors the auxiliary channel signals for at least one frame time, until the last line of an even field. The microprocessor may distinguish odd fields from even fields, for example, by monitoring the amount of time between the last horizontal sync pulse and the first equalization pulse. This time is longer for even fields than for odd fields.

The final step in the initialization sequence 1110 is to set the main/auxiliary control signals, MA_1 through MA_4, so that main channel signals are processed and displayed.

Decision block 1112 synchronizes the control sequence of the microprocessor to the auxiliary channel vertical sync signal by circulating through a loop until the value in counter FTIME is greater than or equal to the calculated time between auxiliary signal vertical sync pulses, VTIME.

When FTIME is greater than or equal to VTIME microprocessor 12 executes the instructions shown in block 1114. The first step in block 1114 is to update VTIME. This step is actually performed in the interrupt subroutine linked to the vertical sync interrupt. It is placed here in the microprocessor control sequence to indicate approximately when it occurs. The next two steps in block 1114 reset the auxiliary channel field and line time counters FTIME and LTIME to zero and change the value of the auxiliary channel odd field indicator ODDF between 1 and 0. If ODDF was 1 for the last field processed it is changed to 0 for this field and if it was 0 for the last field, it is changed to 1 for this field. The final step in block 1114 assigns the value 0 to the variable LINENO. LINENO is incremented by one for each horizontal line period of the auxiliary signal, so it holds the line number of the current line of the auxiliary picture. LINENO is used by the microprocessor to set and reset the MA signals and to change the weighting factors applied to comb filter 310.

Decision block 1116 is the next step in the instruction sequence of the microprocessor after block 1114. If the variable ODDF has a 0 value, indicating that the auxiliary channel is providing an even field, the microprocessor branches to block 1115. Block 1115 changes the weighting factors of comb filter 310 to those shown in column 1 of the table in FIGURE 5. These comb weights are appro-

priate for processing three successive lines from the main picture. They are used during the even field time of the auxiliary signal since only lines of the main picture are processed in this interval. From block 1115, the next step in the microprocessor control sequence is the decision block 1112 which causes the microprocessor to circulate in a loop until the next vertical sync pulse occurs.

If the variable ODDF has a value of 1 in block 1116, the next step in the control sequence of the microprocessor is decision block 1118. Block 1118 is the first block in the loop which handles the blank lines at the beginning of a field. In the NTSC system, there are 21 such line intervals. Decision block 1118 compares the auxiliary channel line number, stored in the variable LINENO, with the value 21. While the value of LINENO is less than 21, the microprocessor program steps from block 1116 to block 1118. Decision block 1118 is a loop which waits until the end of a horizontal line. If the counter variable LTIME has a value less than the predetermined horizontal line time, HTIME, the block branches back to itself and performs the test again. When LTIME is greater than or equal to HTIME, however, the control sequence switches to block 1122. Block 1122 updates the variable HTIME, increments the value of LINENO and resets the line time counter LTIME. From block 1122 the microprocessor steps back to the beginning of the loop, decision block 1118.

When LINENO is incremented to have a value greater than or equal to 21, decision block 1118 causes the microprocessor control sequence to branch to block 1124. Block 1124 is the first step of auxiliary signal image processing. In this step the modulo 4 value of the auxiliary channel line number, LINENO, is placed into the variable LN and the control sequence steps to block 1126. If LN is equal to 0, decision block 1126 causes the program to step to block 1128, otherwise the program steps to block 1130. When LN is 0, the current auxiliary channel line has a line number, LINENO, that is evenly divisible by four. The lines that satisfy this condition are chosen in the present embodiment to make up the auxiliary image. Accordingly, block 1128 resets the main/auxiliary control signals MA_1 through MA_4, causing the system to switch from processing main channel signals to processing auxiliary channel signals. From block 1128, the microprocessor program steps to decision block 1140. Block 1140 causes the program to branch to decision block 1120 if there are more lines to be processed in the current field. If there are no more lines in the current field (i.e. FTIME is greater than or equal to VTIME), decision block 1140 causes the microprocessor to branch to block 1114 and begin processing the next field.

If LN is not equal to 0, in decision block 1126, then the microprocessor steps to decision block 1130. Block 1130 steps the program to block 1132 if LN is equal to 1 and steps to decision block 1134 otherwise. Block 1132 controls the processing of the main channel lines that immediately follow the chosen auxiliary channel lines. The first step in block 1132 sets the signals MA_1 through MA_4 to resume main signal processing. The second step changes the weighting factors applied to comb filter 310 of FIGURE 3 to be those shown in the third column of the table in FIGURE 5. The program step following block 1132 is decision block 1140 described above.

If variable LN does not have a value of 1, block 1130 steps the program to decision block 1134. Block 1134 steps to block 1136 if LN has a value of 2 and to block 1138 otherwise (i.e. if LN has a value of 3). Blocks 1136 and 1138 change the weighting factors applied to comb filter 310 to be those shown in the fourth and fifth columns of the table in FIGURE 5 respectively. From both blocks 1136 and 1138, the program steps to block 1140, described above.

The microprocessor continues in this control loop until a new auxiliary channel is chosen. When this occurs, channel selector 10 of FIGURE 2 signals the microprocessor to step to initialization block 1110.

The other function of microprocessor 12 is to control the chrominance gain by monitoring, via data bus SPD, the main and auxiliary channel samples from chroma processor 380 of FIGURE 3 and by supplying gain factors for the main and auxiliary channels to this processor, via bus SPD. The control flow for this function is not shown since it is not considered a part of the invention. This function may be integrated into the main and auxiliary processing steps of the program shown in FIGURE 11 by programming techniques known to those skilled in the art.

The pix-in-pix receiver described above uses two tuners, two IF amplifiers and two demodulator systems, one for the main channel and one for the auxiliary channel. A more economical system would use only one of each of these systems. Since the present invention operates on time-division multiplexed signals and since its signal processing is pipelined, it is particulary suited for use in a single tuner pix-in-pix receiver. FIGURE 12 is a block diagram of the part of the receiver shown in FIGURE 2 that would need to be changed to produce a receiver using only one tuner. Channel selector 10 provides a data signal to microprocessor 12 indicating the channel number of a selected channel and whether it is the main or auxiliary channel. Microprocessor 12 converts the channel number into control signals for tuner 22. The control signals are passed to the tuner via data bus TD

when the channels are selected. Thereafter, tuner 22 stores these control signals in its local memory. Switching between the main and auxiliary channels is controlled by a single bit signal applied to the tuner 22 by microprocessor 12 via connection CC. Analog composite video signals from tuner 22 are applied to A/D converter 34 and to sync separator 26. A/D converter 34 is driven by a clock synchronized to the main channel burst and provides digital samples of the main and auxiliary composite video signals to the rest of the receiver. Sync separator 26 provides both the main and auxiliary channel horizontal and vertical sync pulses. These are used to synchronize conventional horizontal and vertical oscillators (not shown) to provide continual pulses for both the main and auxiliary channels. The pulses from the auxiliary channel horizontal and vertical oscillators may be applied, in lieu of actual horizontal and vertical sync pulses, to synchronize microprocesor 12 to the auxiliary signals. Alternatively, sync pulses from sync separator 26 may be applied directly to the microprocessor 12. In this instance, it would be desirable to add program steps to the interrupt subroutines linked to the horizontal and vertical sync signals to differentiate between the main and auxiliary pulses. These program steps may, for example, synchronize only to those pulses that occur at intervals close to multiples of the calculated intervals for the auxiliary channel horizontal and vertical sync pulses. The burst gate signal provided by sync separator 26 is, likewise, the burst gate signal for both the main and auxiliary signals.

The output pulses from the auxiliary channel horizontal and vertical oscillators condition microprocessor 12 to switch the tuner between the main and auxiliary channels. As in the main embodiment, the tuner is switched from the main channel to the auxiliary channel immediately prior to the leading edge of the auxiliary channel horizontal sync pulse of every fourth line of one of the two fields that make up each frame of the auxiliary picture. The tuner is switched from the auxiliary channel to the main channel immediately after the end of active video on these lines.

Claims

1. Video signal processing apparatus including a source of time division multiplexed video signal having alternating first and second mutually independent composite video signal components each having luminance signal components and chrominance signal components including a color burst signal component,

characterized by:

means (30) for generating a reference clock signal having a frequency substantially equal to an integral multiple of the frequency of the color burst signal component of said first composite video signal component;

filtering means (310,340,350,352,360,370), responsive to said time-division multiplexed composite video signal for separating the chrominance signal components therefrom to provide a time-division multiplexed chrominance signal having alternating first and second chrominance signal components corresponding respectively to the respective chrominance components of said first and second composite video signal components; and

phase correcting means (672,658), responsive to said time-division multiplexed chrominance signal, to said reference clock signal and to said color burst signal components for producing first and second phase corrected chrominance signals each comprising a sequence of clocked samples representing in succession respective color difference signal components of the same predetermined identity (e.g. R-Y; B-Y etc.).

2. Apparatus as set forth in Claim 1 wherein said generating means includes a phase locked loop (30) coupled to said source for causing said reference clock signal to have a predetermined phase relationship with respect to the color burst signal component of said first composite video signal component.

3. Apparatus as set forth in claim 1 or 2 wherein the chrominance signal components of said first and second composite video signal components each include two quadrature phase related color difference signal components, said apparatus further comprising:

means (650-660,662) responsive to the burst signal component of said first and second chrominance signals for determining values corresponding to the magnitudes of the burst signal components of said chrominance signals;

means (12,666-67-,679,683) responsive to the first and second phase corrected chrominance signals, to the values corresponding to the magnitudes of the first and second burst signal components and to a reference value, for providing first and second magnitude and phase corrected chrominance signals, the burst signal component of each having a magnitude substantially equal to said reference value; and

means (680,682) for separating each of the two quadrature phase related color difference signal components from each of said first and second magnitude and phase corrected

* C L M S *

when the channels are selected. Thereafter, tuner 22 stores these control signals in its local memory. Switching between the main and auxiliary channels is controlled by a single bit signal applied to the tuner 22 by microprocessor 12 via connection CC. Analog composite video signals from tuner 22 are applied to A/D converter 34 and to sync separator 26. A/D converter 34 is driven by a clock synchronized to the main channel burst and provides digital samples of the main and auxiliary composite video signals to the rest of the receiver. Sync separator 26 provides both the main and auxiliary channel horizontal and vertical sync pulses. These are used to synchronize conventional horizontal and vertical oscillators (not shown) to provide continual pulses for both the main and auxiliary channels. The pulses from the auxiliary channel horizontal and vertical oscillators may be applied, in lieu of actual horizontal and vertical sync pulses, to synchronize microprocesor 12 to the auxiliary signals. Alternatively, sync pulses from sync separator 26 may be applied directly to the microprocessor 12. In this instance, it would be desirable to add program steps to the interrupt subroutines linked to the horizontal and vertical sync signals to differentiate between the main and auxiliary pulses. These program steps may, for example, synchronize only to those pulses that occur at intervals close to multiples of the calculated intervals for the auxiliary channel horizontal and vertical sync pulses. The burst gate signal provided by sync separator 26 is, likewise, the burst gate signal for both the main and auxiliary signals.

The output pulses from the auxiliary channel horizontal and vertical oscillators condition microprocessor 12 to switch the tuner between the main and auxiliary channels. As in the main embodiment, the tuner is switched from the main channel to the auxiliary channel immediately prior to the leading edge of the auxiliary channel horizontal sync pulse of every fourth line of one of the two fields that make up each frame of the auxiliary picture. The tuner is switched from the auxiliary channel to the main channel immediately after the end of active video on these lines.

Claims

1. Video signal processing apparatus including a source of time division multiplexed video signal having alternating first and second mutually independent composite video signal components each having luminance signal components and chrominance signal components including a color burst signal component,

characterized by:

means (30) for generating a reference clock signal having a frequency substantially equal to an integral multiple of the frequency of the color burst signal component of said first composite video signal component;

filtering means (310,340,350,352,360,370), responsive to said time-division multiplexed composite video signal for separating the chrominance signal components therefrom to provide a time-division multiplexed chrominance signal having alternating first and second chrominance signal components corresponding respectively to the respective chrominance components of said first and second composite video signal components; and

phase correcting means (672,658), responsive to said time-division multiplexed chrominance signal, to said reference clock signal and to said color burst signal components for producing first and second phase corrected chrominance signals each comprising a sequence of clocked samples representing in succession respective color difference signal components of the same predetermined identity (e.g. R-Y; B-Y etc.).

2. Apparatus as set forth in Claim 1 wherein said generating means includes a phase locked loop (30) coupled to said source for causing said reference clock signal to have a predetermined phase relationship with respect to the color burst signal component of said first composite video signal component.

3. Apparatus as set forth in claim 1 or 2 wherein the chrominance signal components of said first and second composite video signal components each include two quadrature phase related color difference signal components, said apparatus further comprising:

means (650-660,662) responsive to the burst signal component of said first and second chrominance signals for determining values corresponding to the magnitudes of the burst signal components of said chrominance signals;

means (12,666-67-,679,683) responsive to the first and second phase corrected chrominance signals, to the values corresponding to the magnitudes of the first and second burst signal components and to a reference value, for providing first and second magnitude and phase corrected chrominance signals, the burst signal component of each having a magnitude substantially equal to said reference value; and

means (680,682) for separating each of the two quadrature phase related color difference signal components from each of said first and second magnitude and phase corrected

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chrominance signals.

4. Apparatus as set forth in claim 1 or 2 further including sampling means (34) responsive to said time multiplexed composite video signal for providing samples representative thereof at instants determined by said reference clock signal, wherein said filtering means comprises:

a comb filter (310) coupled to said sampling means for providing a filtered output signal comprising samples representing a comb filtered chrominance components and part of the low frequency spectrum of the luminance signal component of said first composite video signal component;

multiplexer (340) coupled to said sampling means and to said comb filter for providing, during alternate first and second time intervals, said filtered output signal and samples representing said second composite video signal component respectively; and

band-pass filtering means (370) coupled to said mutliplexer for attenuating the luminance signal components relative to the chrominance signal components of the samples provided by said multiplexer to provide alternating first and second sequences of samples representing the chrominance components of said first and second composite video signals respectively.

5. Apparatus as set forth in claim 1 or 2 further including sampling means (34) responsive to said time-division multiplexed composite video signal for providing samples representative thereof at instants determined by said reference clock signal, wherein said filtering means comprises:

a comb filter (310) coupled to said sampling means for providing luminance samples representing the luminance signal component of said first composite video signal component: and

a low-pass filter (350) coupled to said sampling means for providing samples representing the luminance signal component of said second composite video signal component.

6. Apparatus in accordance with claim 1 or 2 wherein said first and second composite video signal components respectively occur during alternate first and second time intervals, and the chrominance signal components of the respective composite video signal components each include two quadrature phase related color difference signal components, said apparatus further comprising:

separating means (680,682) coupled to said filtering means and responsive to said time-division multiplexed chrominance signal for providing, during said first time intervals, two sequences of samples each corresponding to a respectively different one of the two color difference signal components of said first composite video signal and for providing, during said second time interval, two sequences of samples each corresponding to a respectively different one of the two color difference signal components of said second composite video signal.

7. Apparatus as set forth in claim 6 further comprising:

an auxiliary memory (50), coupled to said separating means for storing color difference signal samples provided by said separating means during one of said second time intervals, and for providing said stored samples during a subsequent one of said first time intervals.

8. Apparatus as set forth in claim 6 or 7 further comprising:

a main memory (70), coupled to said separating means for storing color difference samples provided by said separating means during one of said first time intervals and for providing said stored samples during a subsequent one of said second time intervals.

9. Apparatus as set forth ion claim 6, 7 or 8 wherein said filtering means includes a comb filter (310) providing, during said first intervals, a first output comprising comb filtered luminance samples of said first composite video signal and a second output comprising samples representing a comb filtered chrominance signal accompanied by part of the low frequency spectrum of the luminance signal components of said first composite video signal.

10. Apparatus as set forth in claim 9 wherein the comb filter comprises:

memory means (410) having an input port coupled to receive samples of said time-division multiplexed video signal, a number of sample delaying stages, and an output port for providing delayed samples of said first composite video signal during said first time intervals;

first sample weighting means (W1), coupled to said input port for multiplying the samples received thereby during said first time intervals by a selected one of a first set of predetermined weighting factors;

second sample weighting means (W3),

coupled to the output port of said memory means for multiplying the samples provided thereby by a selected one of a second set of predetermined weighting factors;

third sample weighting means (W4), coupled to said input port for multiplying the samples received thereby during said first time intervals by a selected one of a third set of predetermined weighting factors;

fourth sample weighting means (W6), coupled to the output port of said memory means for multiplying the samples provided thereby by a selected one of a fourth set of predetermined weighting factors;

first sample combining means (420) coupled to said first and second sample weighting means for combining the samples provided thereby to produce said first output comprising said comb filtered luminance samples of said first composite video signal; and

second sample combining means (430) coupled to said third and fourth sample weighting means for combining the samples provided thereby to produce said first output including said comb filtered chrominance samples of said first composite video signal.

Revendications

1. Dispositif de traitement d'un signal vidéo comprenant une source d'un signal vidéo multiplexé par division dans le temps ayant des première et seconde composantes alternantes, mutuellement indépendantes d'un signal vidéo composé, ayant chacune des composantes d'un signal de luminance et des composantes d'un signal de chrominance comprenant une composante d'un signal de synchronisation de sous-porteuse couleur, caractérisé par :

un moyen (30) pour produire un signal d'horloge de référence ayant une fréquence sensiblement égale à un multiple entier de la fréquence de la composante du signal de synchronisation de sous-porteuse couleur de la première composante du signal vidéo composé;

un moyen de filtrage (310,340,350,352,360,370), répondant au signal vidéo composé multiplexé par division dans le temps pour séparer les composantes du signal de chrominance de celui-ci pour produire un signal de chrominance multiplexé par division dans le temps ayant des première et seconde composantes du signal de chrominance alternantes correspondant respectivement aux composantes de chrominance respectives des première et seconde composantes du signal vidéo composé; et

un moyen de correction de phase (672,658), répondant au signal de chrominance multiplexé par division dans le temps, au signal d'horloge de référence et aux composants du signal de synchronisation de sous-porteuse couleur pour produire des premier et second signaux de chrominance corrigés en phase, comprenant chacun une séquence d'échantillons synchronisés représentant en succession des composantes de signaux de différence de couleurs respectives de la même identité prédéterminée (par exemple, R-Y; B-Y, etc.).

2. Dispositif selon la revendication 1, où le moyen de production précité comprend une boucle verrouillée en phase (30) couplée à la source précitée pour amener le signal d'horloge de référence à avoir une relation de phase prédéterminée par rapport à la composante du signal de synchronisation de sous-porteuse couleur de la composante précitée du signal vidéo composé.

3. Dispositif selon la revendication 1 ou 2, où les composantes du signal de chrominance des première et seconde composantes du signal vidéo composé précitées comprennent chacune deux composantes de signaux de différence de couleurs en relation de phase en quadrature, ledit dispositif comprenant de plus :

un moyen (650-660,662) répondant à la composante du signal de synchronisation de sous-porteuse couleur des premier et second signaux de chrominance pour déterminer des valeurs correspondant aux grandeurs des composantes du signal de synchronisation de sous-porteuse couleur des signaux de chrominance;

un moyen (12,666-67-679,683) répondant aux premier et second signaux de chrominance corrigés en phase, aux valeurs correspondant aux grandeurs des première et seconde composantes du signal de synchronisation de sous-porteuse couleur et à une valeur de référence, pour produire des premier et second signaux de chrominance corrigés en grandeur et en phase, la composante du signal de synchronisation de sous-porteuse couleur de chacun ayant une grandeur sensiblement égale à ladite valeur de référence; et

un moyen (680,682) pour séparer chacune des deux composantes des signaux de différence de couleurs en relation de quadrature de phase de chacun des premier et second signaux de chrominance corrigés en grandeur et en phase.

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4. Dispositif selon la revendication 1 ou 2, comprenant de plus un moyen d'échantillonnage (34) répondant au signal vidéo composé multiplexé dans le temps pour produire des échantillons représentatifs de celui-ci à des instants déterminés par le signal d'horloge de référence précité, où le moyen de filtrage précité comprend :

un filtre en peigne (310) couplé au moyen d'échantillonnage pour produire un signal de sortie filtré comprenant des échantillons représentant une composante de chrominance filtrée en peigne et une partie du spectre de basse fréquence de la composante du signal de luminance de la première composante du signal vidéo composé;

un multiplexeur (340) couplé au moyen d'échantillonnage et au filtre en peigne pour produire, pendant des premier et second intervalles de temps alternés, le signal de sortie filtré et des échantillons représentant respectivement les secondes composantes du signal vidéo composé; et

un moyen de filtrage passe-bande (370) couplé audit multiplexeur pour atténuer les composantes du signal de luminance par rapport aux composantes du signal de chrominance des échantillons produits par le multiplexeur pour produire des première et seconde séquences alternantes d'échantillons représentant les composantes de chrominance respectivement des premier et second signaux vidéo composés.

5. Dispositif selon la revendication 1 ou 2, comprenant de plus un moyen d'échantillonnage (34) répondant au signal vidéo composé multiplexé par division dans le temps précité pour produire des échantillons représentatifs de celui-ci a des instants déterminés par le signal d'horloge de référence précité, où le moyen de filtrage comprend :

un filtre en peigne (310) couplé au moyen d'échantillonnage pour produire des échantillons de luminance représentant la composante du signal de luminance de la première composante du signal vidéo composé; et

un filtre passe-bas (350) couplé au moyen d'échantillonnage pour produire des échantillons représentant la composante du signal de lumimance de la seconde composante du signal vidéo composé.

6. Dispositif selon la revendication 1 ou 2, où les première et seconde composantes précitées du signal vidéo composé se produisent respectivement pendant des premier et second intervalles de temps alternés, et les composantes du signal de chrominance des composantes respectives du signal vidéo composé comprennent chacune deux composantes de signaux de différence de couleurs en relation de quadrature de phase, ledit dispositif comprenant de plus :

un moyen de séparation (680, 682) couplé au moyen de filtrage et répondant au signal de chrominance multiplexé par division dans le temps pour produire, pendant des premiers intervalles de temps, deux séquences d'échantillons chacune correspondant à l'une respectivement différentes des deux composantes des signaux de différence de couleurs du premier signal vidéo composé et pour produire, pendant le second intervalle de temps, deux séquences d'échantillons correspondant chacune à l'une respectivement différentes des deux composantes des signaux de différence de couleurs du second signal vidéo composé.

7. Dispositif selon la revendication 6, comprenant de plus :

une mémoire auxiliaire (50), couplée au moyen de séparation précité pour stocker des échantillons des signaux de différence de couleurs produits par le moyen de séparation pendant l'un desdits seconds intervalles de temps, et pour produire lesdits échantillons stockés pendant l'un subséquent des premiers intervalles de temps.

8. Dispositif selon la revendication 6 ou 7, comprenant de plus :

une mémoire principale (70), couplée au moyen de séparation précité pour stocker des échantillons de différence de couleurs produits par le moyen de séparation pendant l'un des premiers intervalles de temps et pour produire lesdits échantillons stockés pendant l'un subséquent des seconds intervalles de temps.

9. Dispositif selon la revendication 6, 7 ou 8, où le moyen de filtrage précité comprend un filtre en peigne (310) produisant pendant les premiers intervalles précités, une première sortie comprenant des échantillons de luminance filtrés en peigne du premier signal vidéo composé précité et une seconde sortie comprenant des échantillons représentant un signal de chrominance filtré en peigne accompagné par une partie du spectre basse fréquence des composantes du signal de luminance du premier signal vidéo composé.

10. Dispositif selon la revendication 9, où le filtre en peigne comprend :

un moyen mémoire (410) ayant une borne

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d'entrée couplée pour recevoir des échantillons du signal vidéo multiplexé par division dans le temps, un nombre d'étages à retard d'échantillon, et une borne de sortie pour produire des échantillons retardés du premier signal vidéo composé précité pendant les premiers intervalles de temps précités;

un premier moyen de pondération d'échantillons (W1), couplé à ladite borne d'entrée pour multiplier les échantillons reçus de la sorte pendant les premiers intervalles de temps par l'un choisi d'un premier jeu de facteurs de pondération prédéterminés;

un second moyen de pondération d'échantillons (W3), couplé à la borne de sortie dudit moyen mémoire pour multiplier les échantillons produits de la sorte par l'un choisi d'un second jeu de facteurs de pondération prédéterminés;

un troisième moyen de pondération d'échantillons(W4), couplé à ladite borne d'entrée pour multiplier les échantillons reçus de la sorte pendant les premiers intervalles de temps par l'un choisi d'un troisième jeu de facteurs de pondération prédéterminés;

un quatrième moyen de pondération d'échantillons (W6), couplé à la borne de sortie du moyen mémoire pour multiplier les échantillons produits de la sorte par l'un choisi d'un quatrième jeu de facteurs de pondération prédéterminés;

un premier moyen de combinaison d'échantillons (420) couplé aux premier et second moyens de pondération d'échantillons pour combiner les échantillons produits de la sorte pour produire la première sortie précitée comprenant les échantillons de luminance filtrés en peigne du premier signal vidéo composé; et

un second moyen de combinaison d'échantillons (430) couplé aux troisième et quatrième moyens de pondération d'échantillons pour combiner les échantillons produits de la sorte pour produire la première sortie précitée comprenant les échantillons de chrominance filtrés en peigne du premier signal vidéo composé.

Patentansprüche

1. Videosignalverarbeitungseinrichtung mit einer Quelle für ein zeitgemultiplextes Videosignal welches erste und zweite, alternierende, voneinander unabhängige Videosignalgemischanteile aufweist, die jeweils einen Leuchtdichtesignalanteil und einen Farbartsignalanteil einschließlich eines Farbsynchronsignalanteiles enthalten, **gekennzeichnet durch:** eine Anordnung (30) zum Erzeugen eines Referenztaktsignales mit einer Frequenz, die im wesentlichen gleich einem ganzen Vielfachen der Frequenz des Farbsynchronsignalanteiles des ersten Videosignalgemischanteiles ist;
eine Filteranordnung (310, 340, 350, 352, 360, 370) für das zeitgemultiplexte Videosignalgemisch zum Abtrennen der Farbartsignalanteile von diesem unter Erzeugung eines zeitgemultiplexten Farbartsignals, welches erste und zweite, alternierende Farbartsignalanteile entsprechend den Farbartsignalanteilen des ersten bzw. zweiten Videosignalgemischanteiles aufweist, und
eine Phasenkorrekturanordnung (672, 658), die auf das zeitgemultiplexte Farbartsignal, das Referenztaktsignal und die Farbsynchronsignalanteile anspricht, um ein erstes und ein zweites phasenkorrigiertes Farbartsignal zu erzeugen, die jeweils eine Folge von getakteten Momentanwerten enthalten, die nacheinander entsprechende Farbdifferenzsignalanteile der gleichen vorgegebenen Art (z.B. R-Y; B-Y usw.) darstellen.

2. Einrichtung nach Anspruch 1, **dadurch gekennzeichnet,** daß die Erzeugungsanordnung eine phasenverriegelte Schleife (30) enthält, die mit der genannten Quelle gekoppelt ist, um zu bewirken, daß das Referenztaktsignal eine vorgegebene Phasenbeziehung zum Farbsynchronsignalanteil des ersten Videosignalgemischanteiles aufweist.

3. Einrichtung nach Anspruch 1 oder 2, bei der die Farbartsignalanteile des ersten und des zweiten Videosignalgemischanteiles jeweils zwei in Bezug aufeinander um 90° in der Phase verschobene Farbdifferenzsignalanteile enthalten, weiterhin **gekennzeichnet durch**
eine auf den Farbsynchronsignalanteil des ersten und des zweiten Farbartsignals reagierende Anordnung (650-660, 662) zum Bestimmen von Werten entsprechend den Größen der Farbsynchronsignalanteile der Farbartsignale;
eine auf das erste und das zweite phasenkorrigierte Farbartsignal, die Werte, die Größen des ersten und des zweiten Farbsynchronsignalanteiles entsprechen, und einen Referenzwert reagierende Anordnung (12, 666-670, 679, 683) zum Erzeugen eines ersten und eines zweiten größen- und phasenkorrigierten Farbartsignals, dessen Farbsynchronsignalanteil jeweils eine Größe hat, die im wesentlichen gleich dem Referenzwert ist, und
eine Anordnung (680, 682), um die in Bezug aufeinander um 90° in der Phase verschobenen Farbdifferenzsignalanteile jeweils vom er-

sten und zweiten größen- und phasenkorrigierten Farbartsignal abzutrennen.

4. Einrichtung nach Anspruch 1 oder 2, mit einer Abtastanordnung (34) für das zeitgemultiplexte Videosignalgemisch zum Erzeugen von diesem entsprechenden Momentanwerten zu Zeitpunkten, welche durch das Referenztaktsignal bestimmt werden, **dadurch gekennzeichnet,** daß die Filteranordnung enthält:
ein Kammfilter (310), das mit der Abtastanordnung gekoppelt ist, um ein gefiltertes Ausgangssignal zu erzeugen, welches Momentanwerte enthält, welche kammgefilterte Farbartsignalkomponenten und einen Teil des niederfrequenten Spektrums der Leuchtdichtesignalkomponente des ersten Videosignalgemischanteiles darstellen, einen Multiplexer (340), der mit der Abtastanordnung und dem Kammfilter gekoppelt ist, um während erster und zweiter, alternierender Zeitintervalle das gefilterte Ausgangssignal bzw. Momentanwerte, die dem zweiten Videosignalgemischanteil entsprechen, zu erzeugen und
eine mit dem Multiplexer gekoppelte Bandpaßfilteranordnung (370) zum Dämpfen der Leuchtdichtesignalanteile bezüglich der Farbartsignalanteile der vom Multiplexer gelieferten Momentanwerte, um erste und zweite alternierende Folgen von Momentanwerten zu erzeugen, welche die Farbartsignalanteile des ersten bzw. zweiten Videosignalgemisches darstellen.

5. Einrichtung nach Anspruch 1 oder 2, mit einer Abtastanordnung (34) für das zeitgemultiplexte Videosignalgemisch zum Erzeugen von dieses darstellenden Momentanwerten zu Zeitpunkten, die durch das Referenztaktsignal bestimmt werden, **dadurch gekennzeichnet,** daß die Filteranordnung enthält: ein mit der Abtastanordnung gekoppeltes Kammfilter (310) zum Erzeugen von Leuchtdichtesignal-Momentanwerten, welche den Leuchtdichtesignalanteil des ersten Videosignalgemischanteiles darstellen, und
ein mit der Abtastanordnung gekoppeltes Tiefpaßfilter (350) zum Erzeugen von Momentanwerten, welche den Leuchtdichtesignalanteil des zweiten Videosignalgemischanteiles darstellen.

6. Einrichtung nach Anspruch 1 oder 2, bei welchem der erste und der zweite Videosignalgemischanteil während erster bzw. zweiter alternierender Zeitintervalle auftreten und die Farbartsignalanteile der jeweiligen Videosignalgemischanteile jeweils zwei in Bezug aufeinander um 90° in der Phase verschobene Farbdifferenzsignalanteile enthalten, weiterhin **gekennzeichnet durch**
eine mit der Filteranordnung gekoppelte Trennanordnung (680, 682) für das zeitgemultiplexte Farbartsignal um während der ersten Zeitintervalle zwei Folgen von Momentanwerten zu erzeugen, welche jeweils verschiedenen der beiden Farbdifferenzsignalanteile des ersten Videosignalgemisches entsprechen, und um während der zweiten Zeitintervalle zwei Folgen von Momentanwerten zu erzeugen, die jeweils verschiedenen der beiden Farbdifferenzsignalanteile des zweiten Videosignalgemisches entsprechen.

7. Einrichtung nach Anspruch 6, weiterhin **gekennzeichnet durch** einen mit der Trennanordnung gekoppelten Hilfsspeicher (50) zum Speichern von Farbdifferenzsignal-Momentanwerten, welche von der Trennanordnung während eines der zweiten Zeitintervalle geliefert werden und zum Liefern der gespeicherten Momentanwerte während eines folgenden der ersten Zeitintervalle.

8. Einrichtung nach Anspruch 6 oder 7, weiterhin **gekennzeichnet durch** einen mit der Trennanordnung gekoppelten Hauptspeicher (70) zum Speichern von Farbdifferenzsignal-Momentanwerten, die durch die Trennanordnung während eines der ersten Zeitintervalle geliefert werden, und zum Liefern der gespeicherten Momentanwerte während eines folgenden der zweiten Zeitintervalle.

9. Einrichtung nach Anspruch 6, 7 oder 8, **dadurch gekennzeichnet,** daß die Filteranordnung ein Kammfilter (310) enthält, das während der ersten Intervalle ein erstes Ausgangssignal, welches kammgefilterte Leuchtdichtesignal-Momentanwerte des ersten Videosignalgemisches enthält, und ein zweites Ausgangssignal, welches ein von einem Teil des niederfrequenten Spektrums der Leuchtdichtesignalanteile des ersten Videosignalgemisches begleitetes kammgefiltertes Farbartsignal darstellen, liefert.

10. Einrichtung nach Anspruch 9, **dadurch gekennzeichnet,** daß das Kammfilter enthält:
eine Speicheranordnung (410), die einen für den Empfang von Momentanwerten des zeitgemultiplexten Videosignals geschalteten Eingangsanschluß, eine Anzahl von Momentanwert-Verzögerungsstufen und einen Ausgangsanschluß für die Lieferung von verzögerten Momentanwerten des ersten Videosignalgemisches während der ersten Zeitinter-

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valle aufweist, eine mit dem Eingangsanschluß gekoppelte erste Momentanwert-Wichtungsanordnung (W1) zum Multiplizieren der während der ersten Zeitintervalle eintreffenden Momentanwerte mit einem ausgewählten Wichtungsfaktor eines ersten Satzes vorgegebener Wichtungsfaktoren,
eine zweite Wichtungsanordnung (W3), die mit dem Ausgangsanschluß der Speicheranordnung gekoppelt ist, um die von diesen gelieferten Momentanwerte mit einem ausgewählten Wichtungsfaktor aus einem zweiten Satz von vorgegebenen Wichtungsfaktoren zu multiplizieren,
eine dritte Wichtungsanordnung (W4), die mit dem Eingangsanschluß gekoppelt ist, um die bei diesem während der ersten Zeitintervalle eintreffenden Momentanwerte mit einem ausgewählten Wichtungsfaktor aus einem dritten Satz vorgegebener Wichtungsfaktoren zu multiplizieren,
eine vierte Wichtungsanordnung (W6), die mit dem Ausgangsanschluß der Speicheranordnung gekoppelt ist, um die von diesen gelieferten Momentanwerte mit einem ausgewählten Wichtungsfaktor aus einem vierten Satz vorgegebener Wichtungsfaktoren zu multiplizieren,
eine erste Momentanwert-Kombinieranordnung (420), die mit der ersten und der zweiten Momentanwert-Wichtungsanordnung gekoppelt ist, umd die von diesen gelieferten Momentanwerte unter Erzeugung des ersten Ausgangssignales zu kombinieren, welches die kammgefilterten Leuchtdichtesignal-Momentanwerte des ersten Videosignalgemisches enthält, und
eine zweite Momentanwert-Kombinieranordnung (430), die mit der dritten und der vierten Momentanwert-Wichtungsanordnung gekoppelt ist, um die von diesen gelieferten Momentanwerte unter Erzeugung des ersten Ausgangssignales, welches die kammgefilterten Farbartsignal-Momentanwerte des ersten Videosignalgemisches enthält, zu kombinieren.