

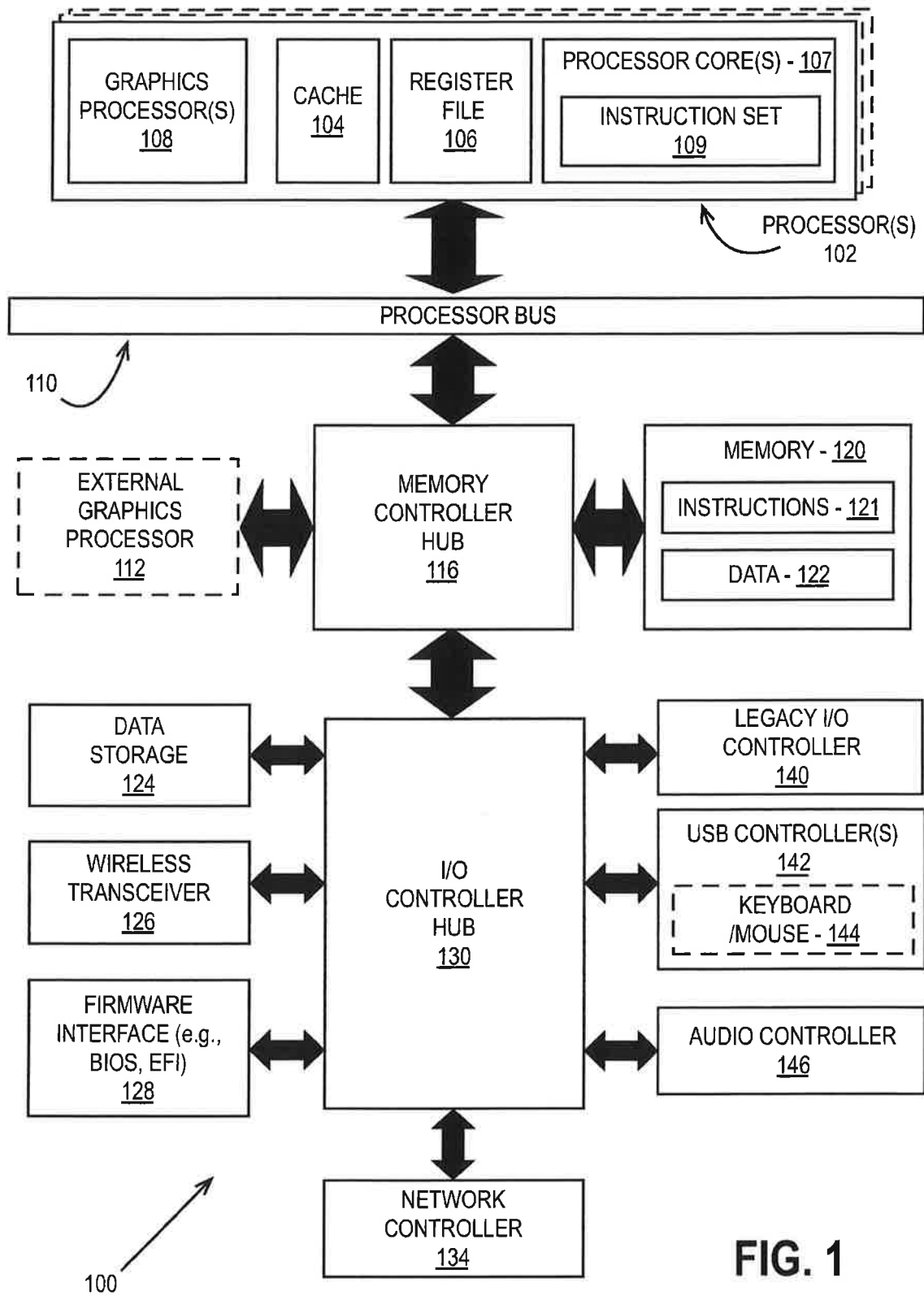


FIG. 1

PROCESSOR 200

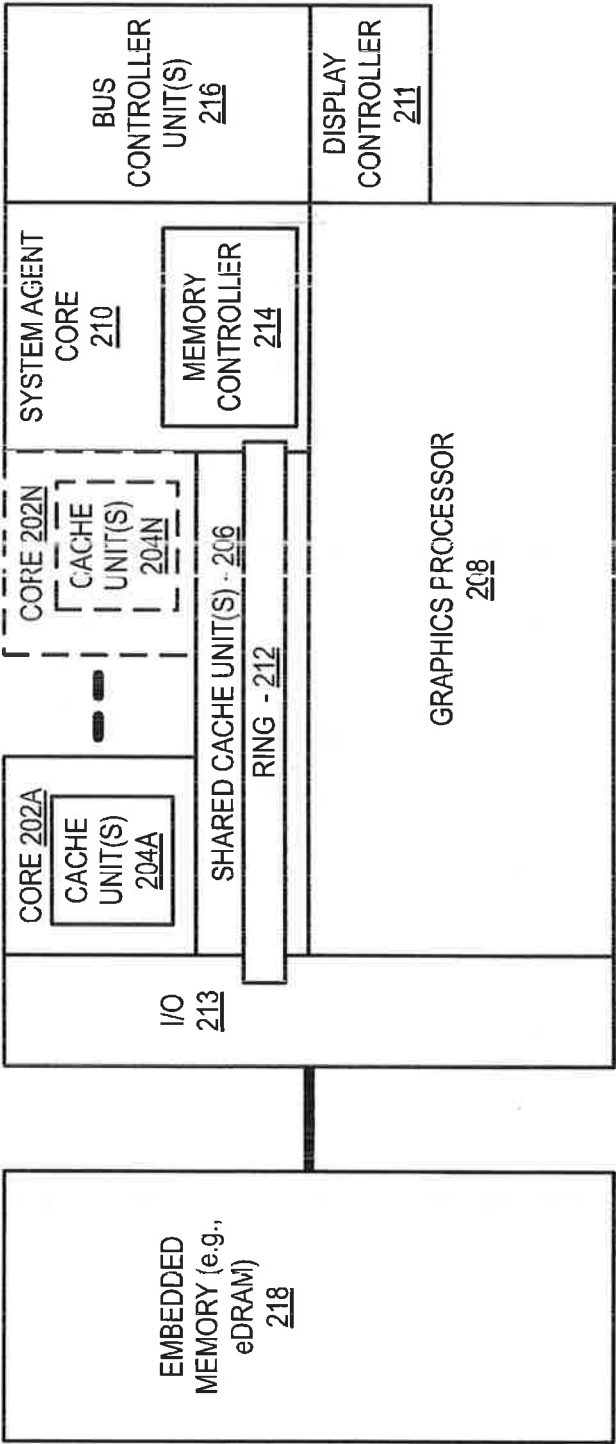


FIG. 2

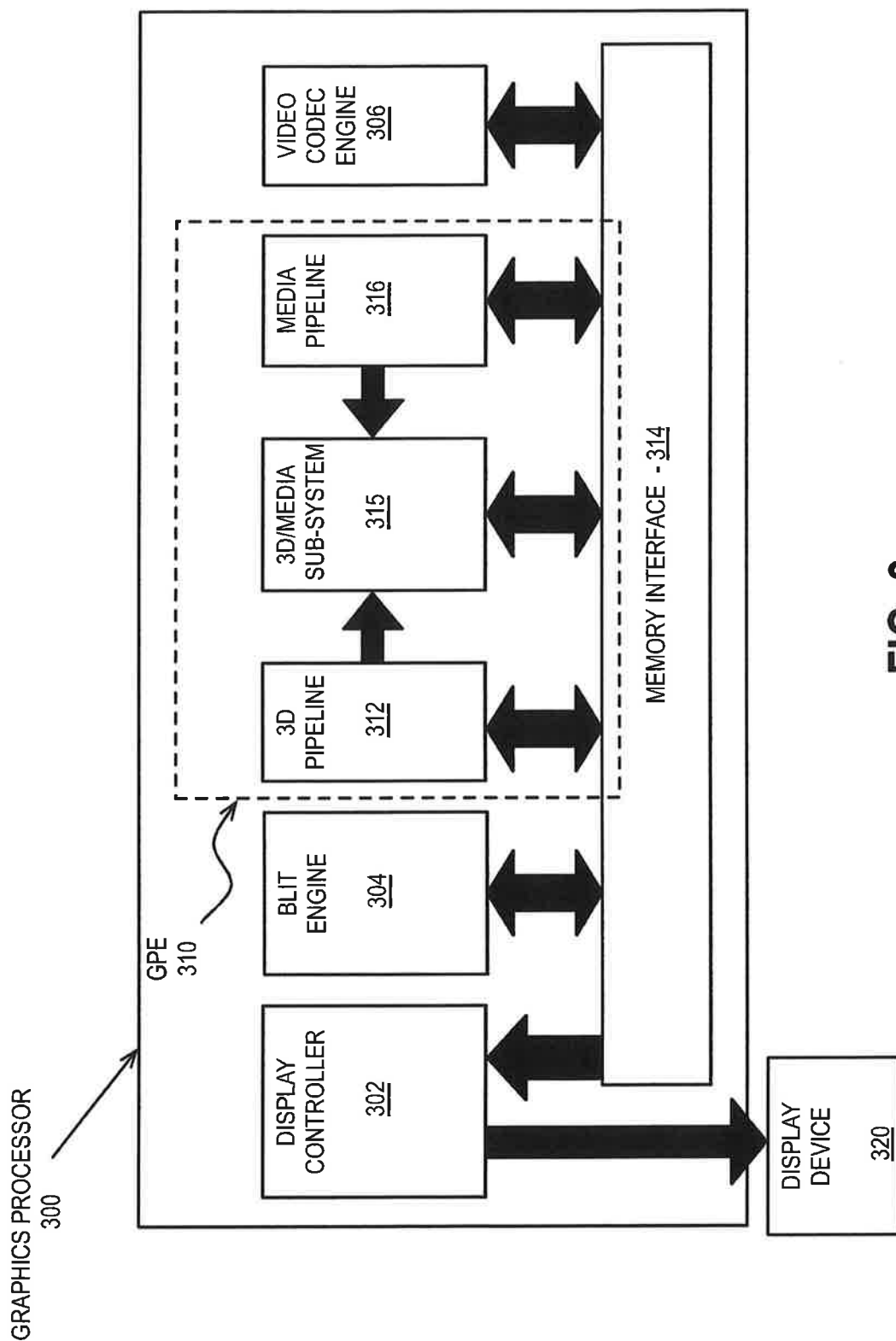


FIG. 3

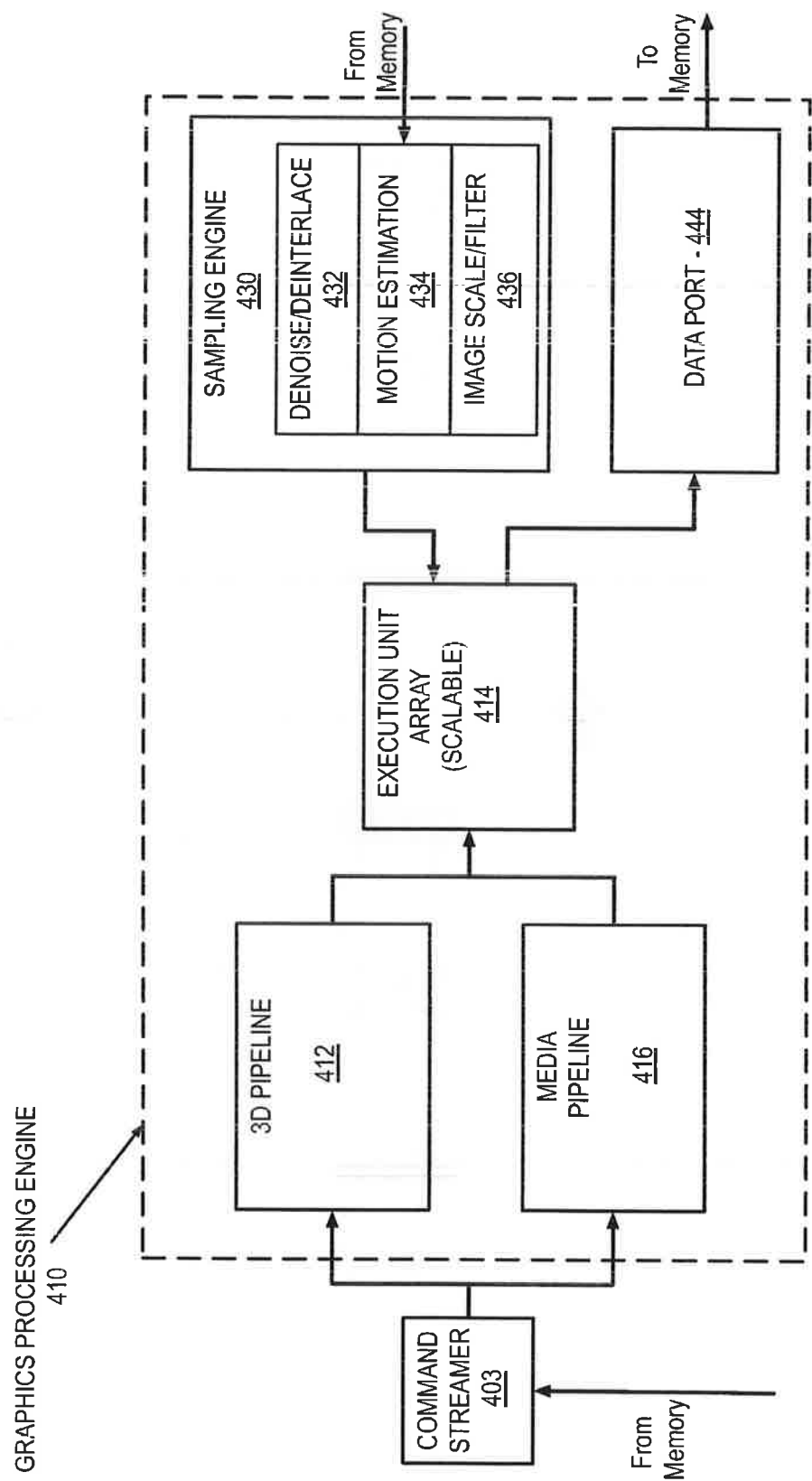


FIG. 4

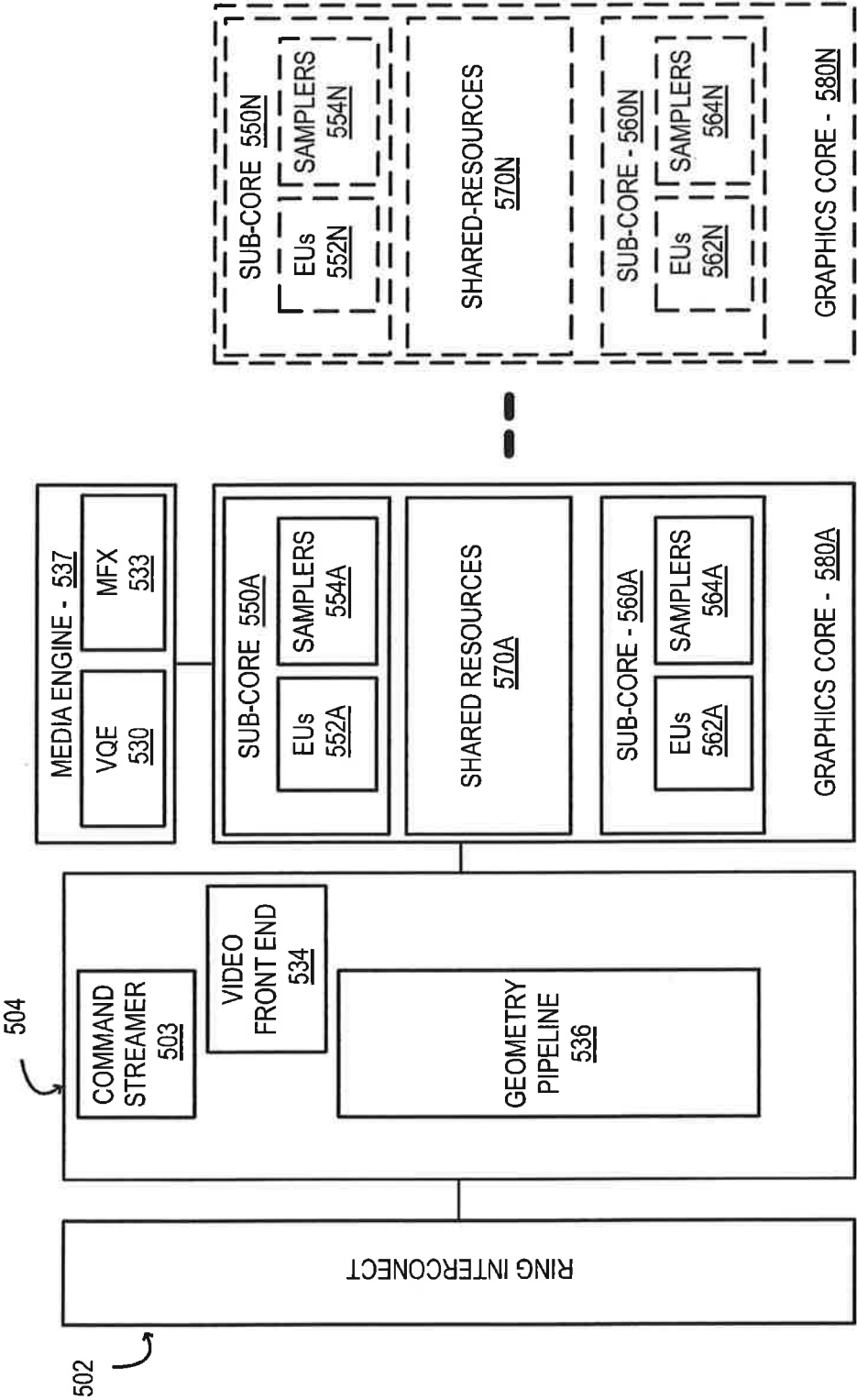


FIG. 5

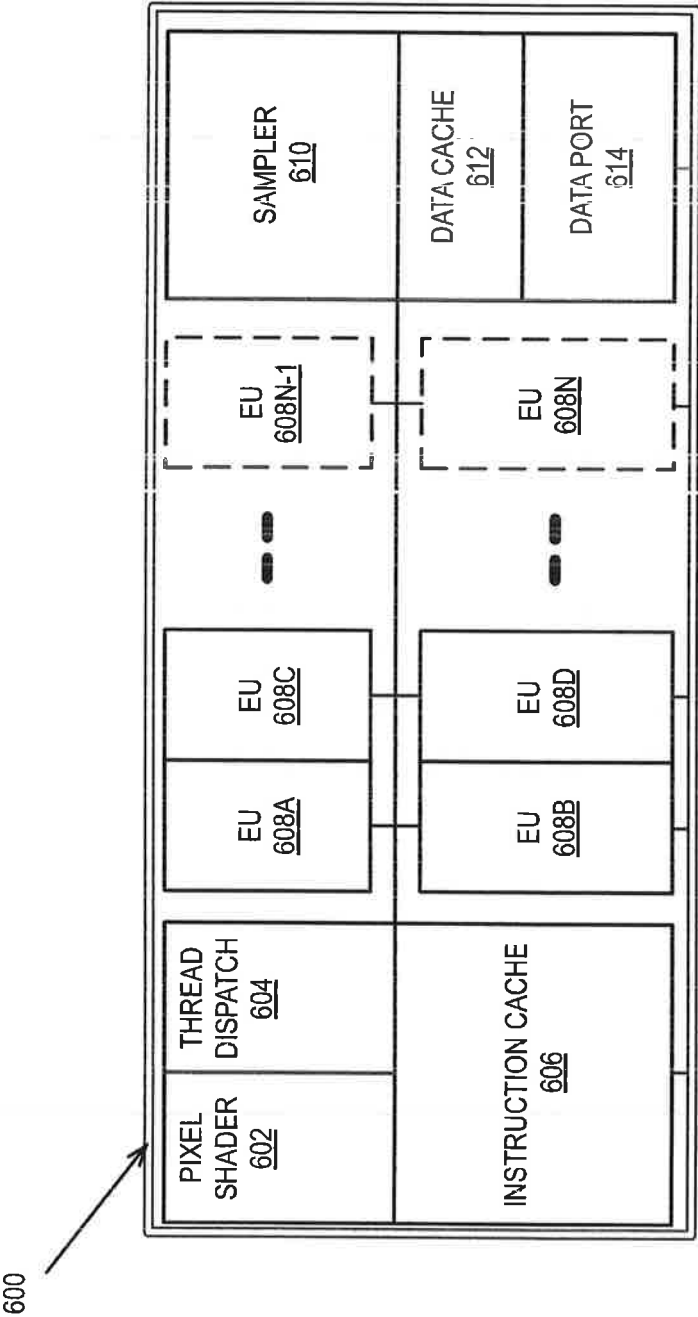


FIG. 6

GRAPHICS CORE INSTRUCTION FORMATS

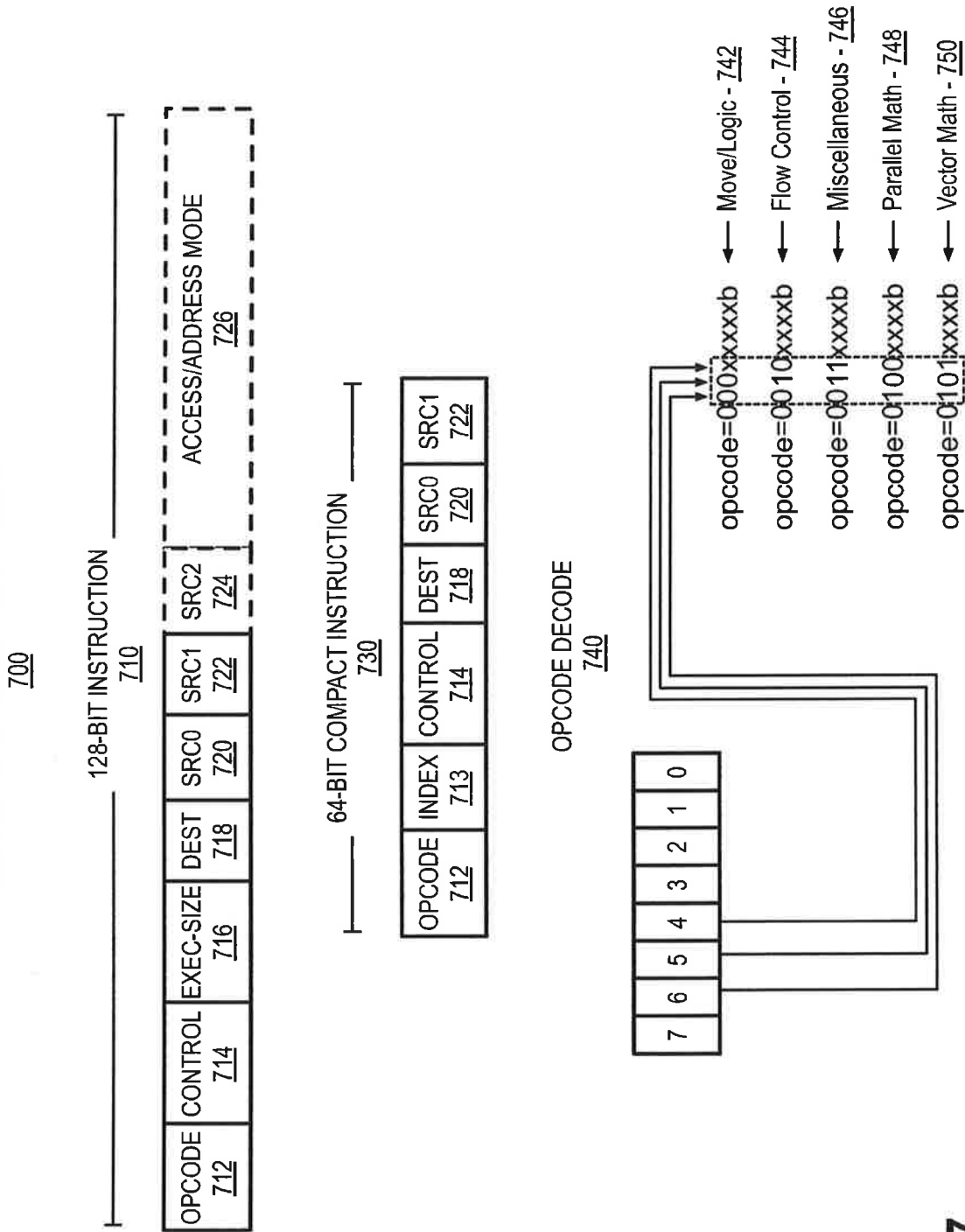


FIG. 7

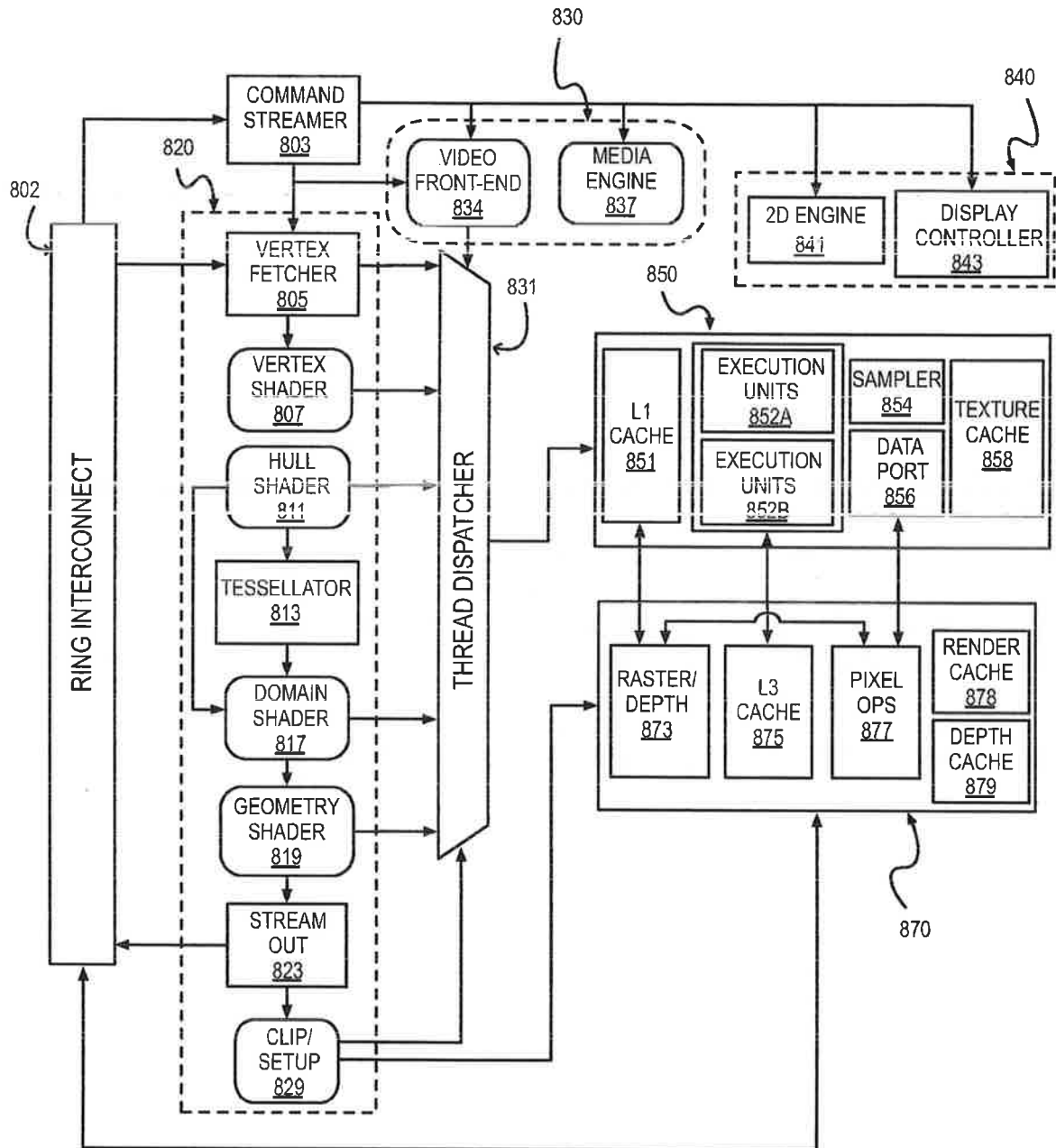
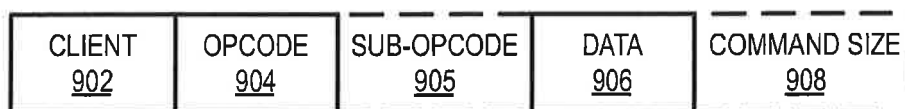
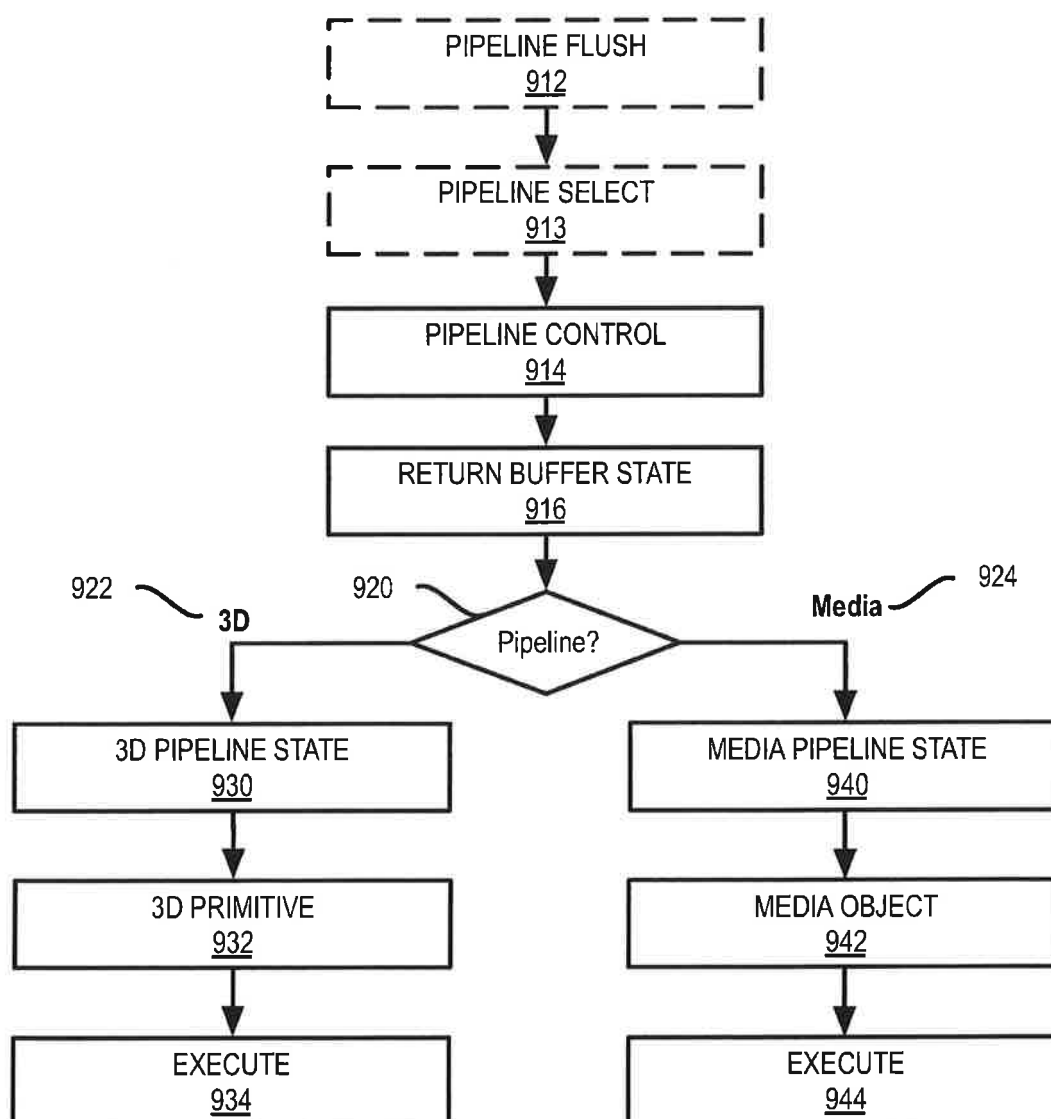


FIG. 8

FIG. 9A**SAMPLE COMMAND FORMAT**900**FIG. 9B****SAMPLE COMMAND SEQUENCE**910

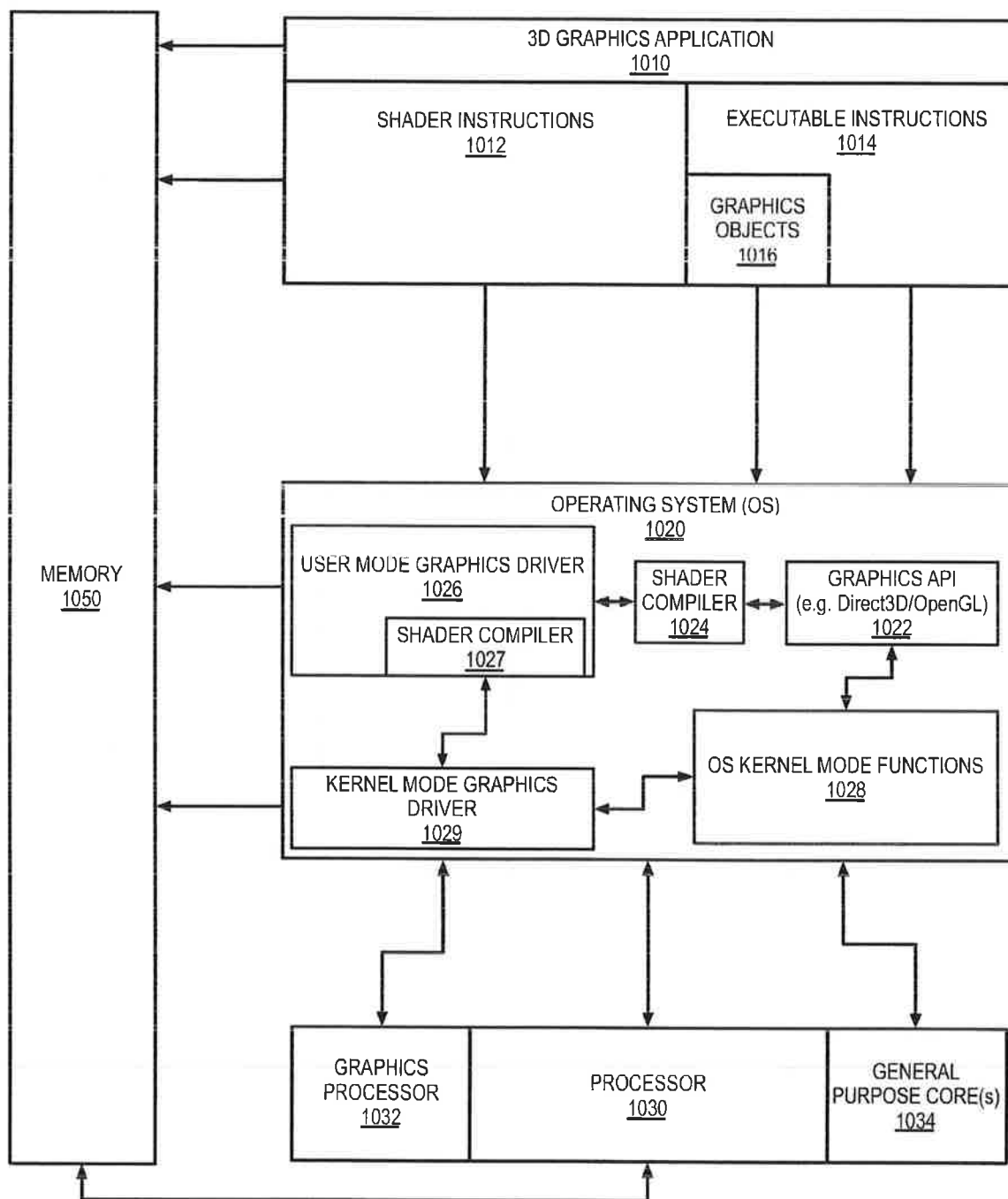


FIG. 10

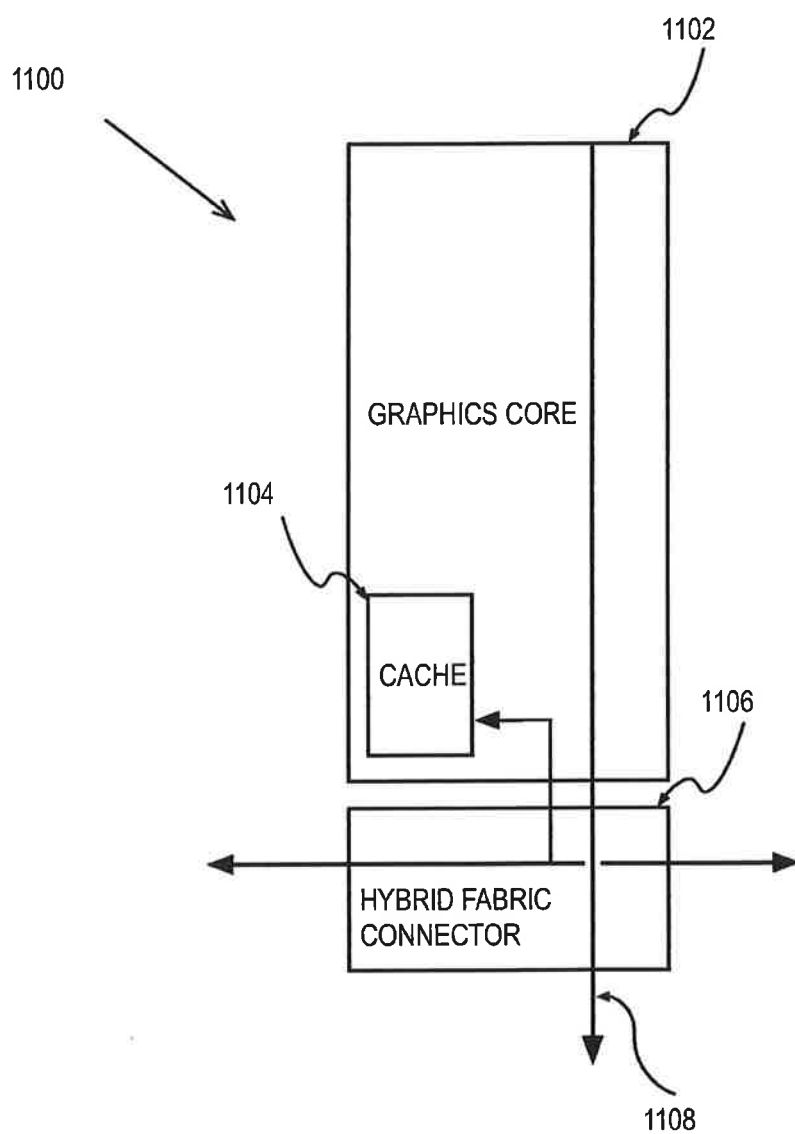
**FIG. 11**

FIG. 12A

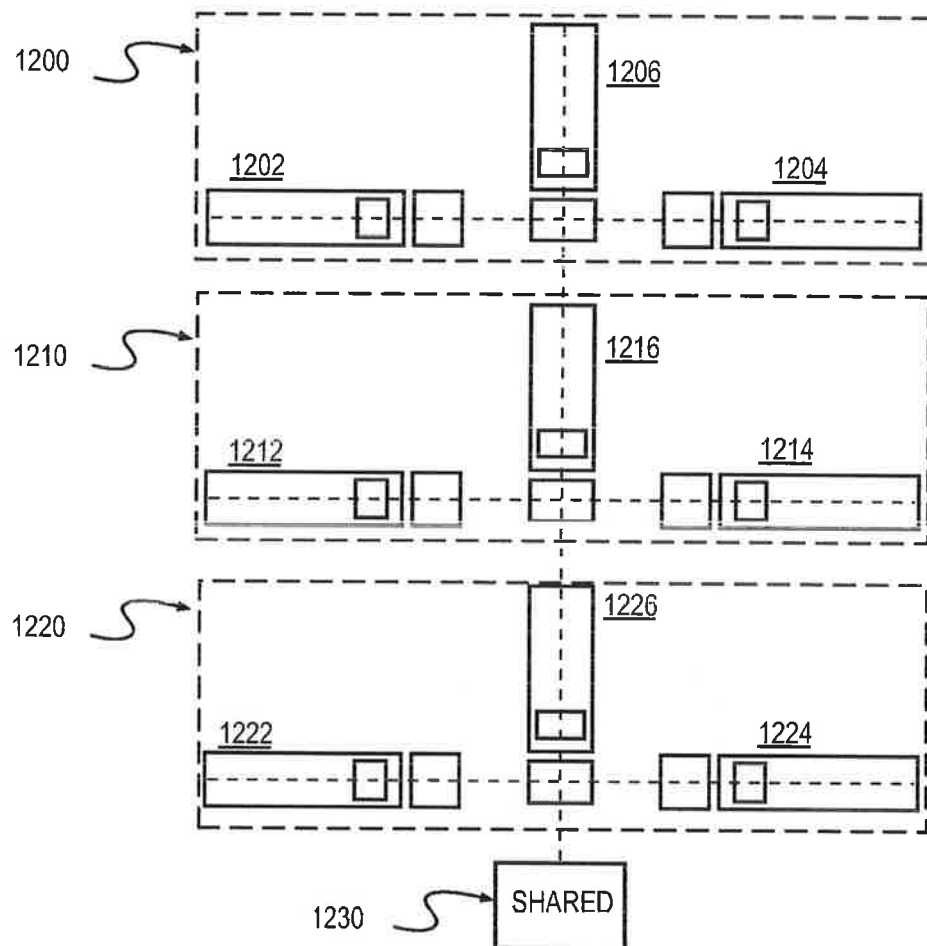
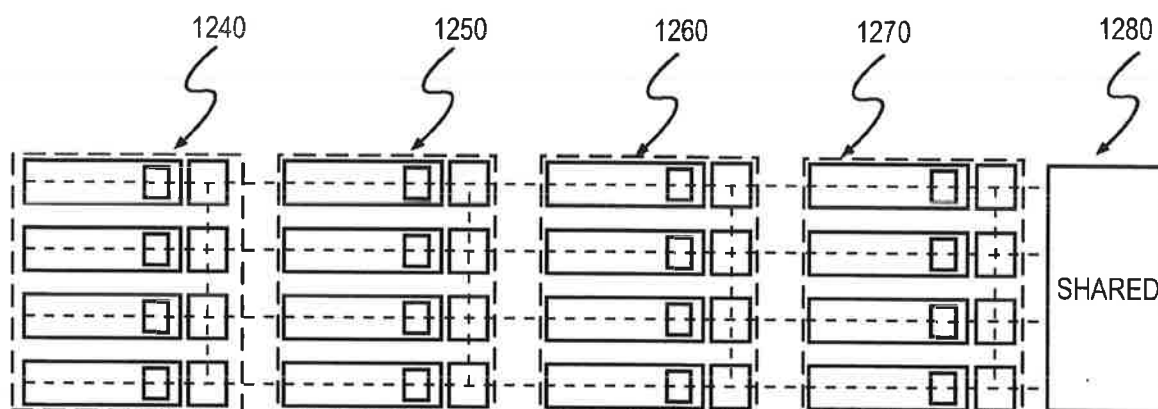


FIG. 12B



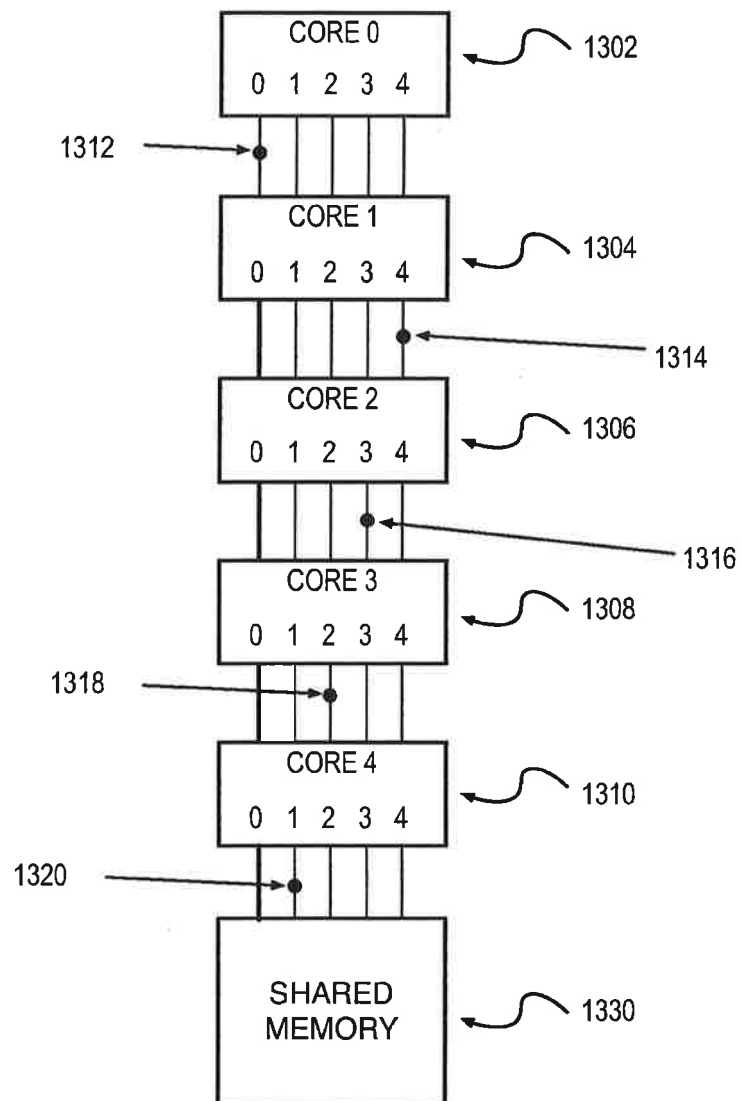


FIG. 13

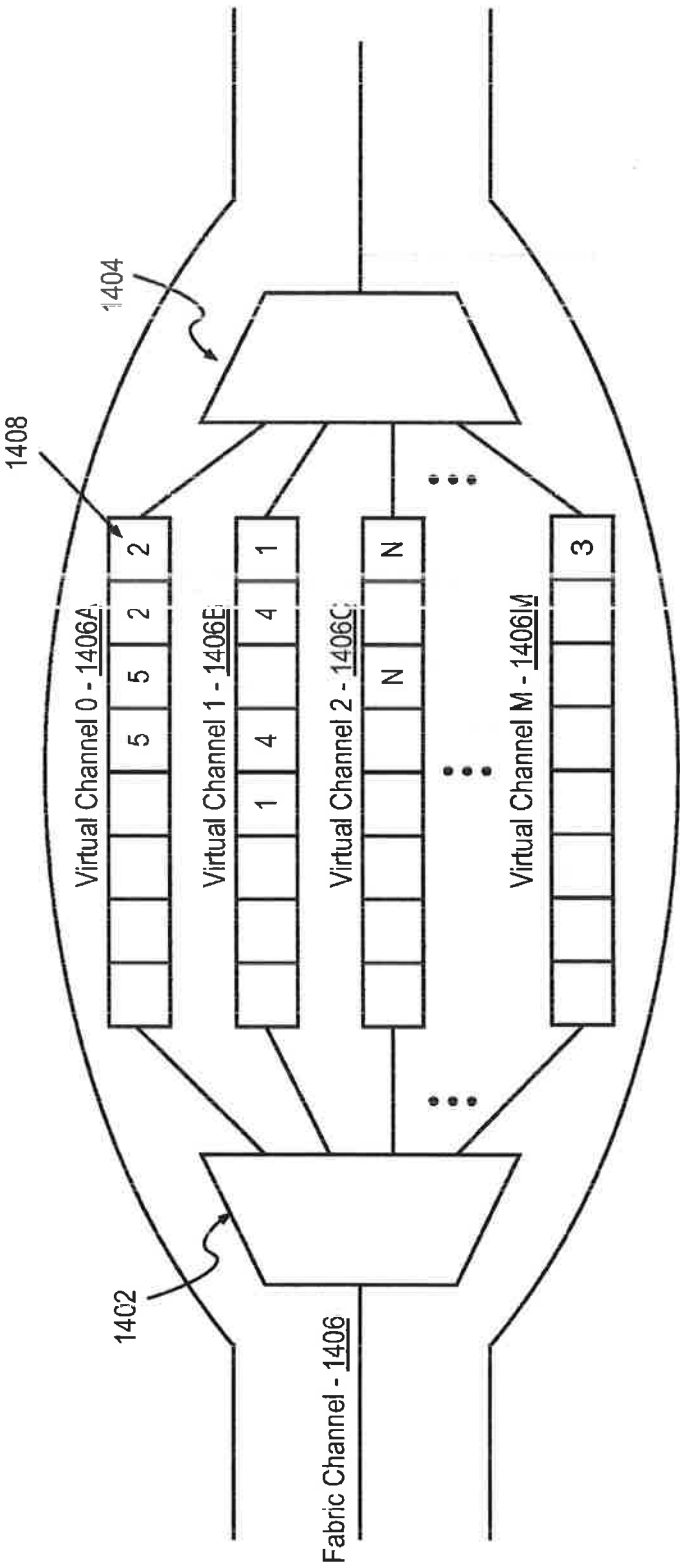
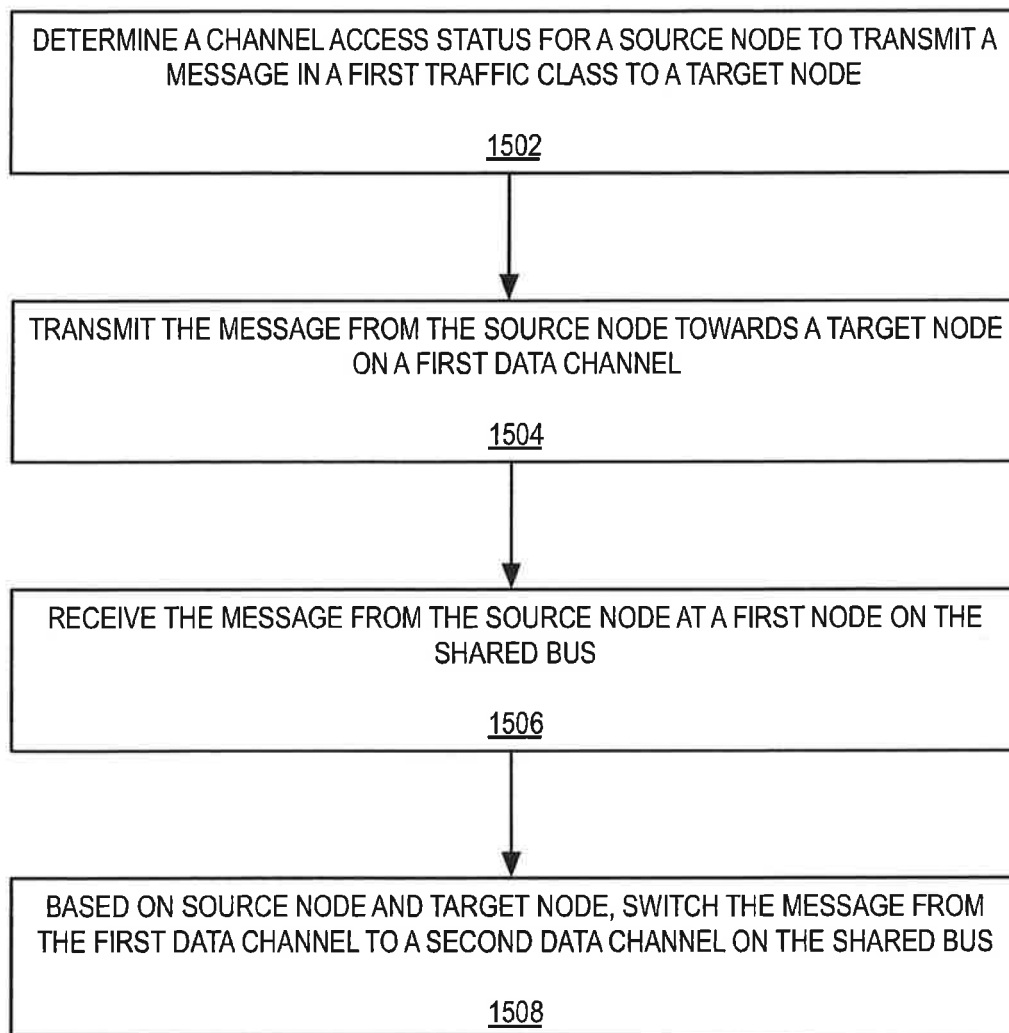


FIG. 14

**FIG. 15**