

Description

Background of the Invention

This invention relates generally to a frequency synthesizer circuit and a method for frequency synthesizing according to the first part of claims 1 and 3, respectively. Such circuit and method are described in DE—B—1 255 736.

High frequency synthesizers are now commonly utilized substitutes for the crystal controlled transmitter oscillators and receiver local oscillators because they are able to provide a frequency stable signal at any one of a plurality of frequencies without the need of a crystal for each such frequency. Such synthesizers generally utilize a phase-locked loop including a voltage controlled oscillator (VCO), a reference oscillator, and a phase detector for comparing the output of the VCO with a reference source. Normally one or more programmable or switchable multipliers or dividers are included within the phase-locked loop so that the loop can be locked to various multiples of the reference source frequency.

As high frequency synthesizers have become widely utilized, they have even been incorporated into portable or mobile battery powered radio communication equipment, such as cellular type radio telephone equipment. It has been found, however, that during normal operation, the phase-locked loop of a synthesizer requires substantial power to operate. Cellular radio equipment must spend large amounts of time receiving a signalling channel. During such reception, the phase-locked loop of its synthesizer is normally continuously operated. Under such operating conditions, the high power drain associated with the synthesizer expends the available battery power in an impractically short period of time.

In order to overcome the rapid battery drain associated with the continuous use of a phase-locked loop high frequency synthesizer in battery powered radio equipment, it is desired to have a high frequency synthesizer arrangement utilizing less battery power than conventional arrangements without sacrificing synthesizer performance.

For ease in discussion and illustration, a phase-locked loop synthesizer is considered to include a VCO, a phase-locked loop means, and a reference source. The phase-locked loop means includes a phase comparator and perhaps one or more programmable dividers and/or multipliers and a loop (low pass) filter. After appropriate division and/or multiplication, the phase locked-loop means compares the VCO signal output with that of the reference source and provides a loop control signal to the VCO for controlling its frequency.

According to the prior art described in DE—B—1 255 736 a "memory circuit" functioning as a sample and hold, is coupled between the loop control signal output of the phase-locked loop and the control input of the voltage controlled oscillator. This memory circuit comprises a switch for opening and closing the control signal line

from the phase-locked loop, a capacitor coupled so as to be charged by the control signal from the phase-locked loop when the switch is closed, and an amplifier having a high impedance input coupling the capacitor and switch to the control input of the voltage controlled oscillator. When the switch is closed the loop operates normally and locks. Once the loop has been locked, power to the phase-locked loop can be interrupted. During such power interruptions, the switch is opened and the voltage on the capacitor coupled to the input of the high impedance amplifier becomes the control signal for the voltage controlled oscillator. This control signal is equal in magnitude to the control signal from the phase-locked loop just before power to the loop was interrupted. The amplifier is selected to have a high input impedance so that the voltage on the capacitor will not discharge very rapidly and the voltage controlled oscillator will be prevented from drifting substantially. Before the voltage controlled oscillator can drift too far, power is reapplied to the phase-locked loop and the switch is again closed so that the loop can be relocked. The frequency and duration of power interruptions and attendant switch openings and the various circuit parameters are determined by how severely the loop drifts when unlocked.

Thus there is provided a prior art method for frequency synthesizing using a phase-locked loop synthesizer comprising the steps of: generating, with phase-locked loop means, a loop control signal for use in controlling a voltage controlled oscillator (VCO) associated with the phase-locked loop means; sampling the magnitude of the loop control signal; generating a memory signal indicative of the sampled magnitude of the loop control signal; interrupting power to the phase-locked loop means; and applying the memory signal, simultaneously with the interruption of power, to a control input of the VCO for controlling its frequency during the power interruption.

As used in a cellular radio such as a mobile telephone, power to the phase-locked loop is normally interrupted (once the loop has been locked a first time). During the time power is interrupted, the switch of the memory means is open. Periodically power is automatically applied to the phase-locked loop and the switch is closed. In addition, power is continuously applied to the phase-locked loop in response to (a) a received command to switch frequency (synthesizer must switch to a new frequency) and transmit, or (b) a received command to transmit on the current frequency, (c) an off-hook condition or (d) a loss of a received signal.

Summary of the Invention

It is an object of the invention to provide for control of the voltage controlled oscillator also during periods of power interruption to the phase-locked loop. According to the invention the voltage controlled oscillator is controlled by the output of a receiver discriminator within the communication equipment. Switch means are

provided for periodically switching the control input of the voltage controlled oscillator away from the loop control signal output of the phase-locked loop means and connecting it instead to the output of the discriminator. An integrator is coupled in the loop control signal path to the voltage controlled oscillator. In this arrangement, the loop is first locked in the conventional manner. Then, the switch means switches the input of the integrator from its normal connection to the phase-locked loop to the output of the discriminator. Of course, using this arrangement, both the phase-locked loop and discriminator must have a zero voltage error signal during a locked condition. Properly designed FM receivers with S-type discriminators can produce a DC voltage proportional to the deviation of the local oscillator frequency and the transmitted signal carrier frequency. In this second embodiment, the phase-locked loop need only be relocked in the traditional manner if the received signal is lost or when it is desired to change received channels.

Further there is provided by the invention a method for frequency synthesizing comprising the steps of: generating, with phase-locked loop means, a loop control signal for use in controlling a voltage controlled oscillator (VCO) associated with the phase-locked loop means; locking the phase-locked loop, decoupling the control input of the VCO from the phase-locked loop means and coupling it instead to the output of a receiver discriminator so that the VCO will be controlled by the discriminator output rather than the loop control signal from the phase-locked loop means; and interrupting power to the phase-locked loop means.

As used in a cellular radio, such as a mobile telephone, after the phase-locked loop has been initially locked, normally power to the phase-locked loop is disabled. During the time the phase-locked loop is disabled, the voltage controlled oscillator is driven by the receiver discriminator. Power is applied to the phase-locked loop whenever (1) a received command calling for a switch in frequency and transmission on the new frequency, (b) a received command calling for transmission on the current frequency, (c) an off-hook condition, or (d) loss of a received signal. A return to the normally disabled (power interrupted conditions of the phase-locked loop occurs in the absence of any of the (a)–(d) conditions above-listed.

Brief Description of the Drawings

The invention will become better understood by reference to the following detailed description and the appended claims when read in conjunction with the Figures, wherein:

FIGURE 1 is a block diagram of a prior art of the frequency synthesizer arrangement; and

FIGURE 2 is a block diagram of an embodiment of the frequency synthesizer arrangement according to the present invention.

Detailed Description of the Preferred Embodiment

Referring now to FIGURE 1, there is shown a prior art battery saving frequency synthesizer circuit. As previously stated, phase-locked loop synthesizers generally include a voltage controlled oscillator (VCO) providing the output of the synthesizer, one or more dividers for dividing the output signal of the voltage controlled oscillator, a phase detector for comparing the direct or derivative (divided) signal from the VCO with a stable signal from a reference source, and a loop filter for receiving the comparison signal from the phase detector and providing a VCO control signal. By changing the divide ratio of the dividers, various multiples of the reference oscillator frequency can be locked onto by the phase-locked loop.

Phase-locked loop (PLL) 10 represents all of the components of a conventional phase-locked loop synthesizer except for its voltage controlled oscillator (VCO) 12 shown as a separate block. The output of phase-locked loop 10 on a signal line 11 represents the loop control signal normally obtained from the loop filter of a phase-locked loop synthesizer. Thus, phase-locked loop 10 includes a phase comparator for comparing the signal output of VCO 12 with the signal from a reference source 14. In essence, the phase comparator of PLL 10 receives a signal from reference source 14 on a signal line 16 and the output of VCO 12 on a signal line 18. For the purposes of this description, the specific details of the phase-locked loop synthesizer 10 are omitted. The details for designing phase-locked loop synthesizers for specific applications can be obtained from a reading of "Frequency Synthesizers Theory and Design" by V. Manassewitsch, published by John Wiley & Sons, copyright 1976. Various phase-locked loops suitable for use as phase-locked loop 10 are even available in "off the shelf" integrated circuit packages.

The loop control signal on line 11 is coupled to one pole of a switch 20. The other pole of switch 20 is coupled to a capacitor 22 and to the input of an amplifier 24, the output of which is coupled to the control input 26 of VCO 12.

The phase-locked loop synthesizer operates as a conventional phase-locked loop when power is applied to PLL 10 and when switch 20 is closed. In this manner, the loop control signal on line 11 is coupled to capacitor 22 and to the input of amplifier 24. During "battery save" operation, switch 20 is opened and power to phase-locked loops 10 on a power line 28 is removed. The means for interrupting power on line 28 to PLL 10 is symbolized by a switch 60. Of course, in a practical design, switch 60 would probably be an electronic switch driven by a pulse generator, or other suitable arrangement. During the time when power is interrupted to PLL 10 via switch 60 and switch 20 is open power is maintained to VCO 12 and amplifier 24. Thus, during battery save operation, phase-locked loop 10 is disabled and the power normally drawn thereby is saved. The magnitude of the loop control signal on line 11,

just before switch 20 is opened, is "memorized" by capacitor 22. The input to amplifier 24 is of sufficiently high impedance so that the voltage on capacitor 22 does not discharge substantially during the time interval that phase-locked loop 10 is disabled. Thus, the value of the loop control signal just before switch 20 is opened continues to be coupled to control input 26 of VCO 12 during the time that phase-locked loop 10 is disabled. Periodically, phase-locked loop 10 is reenergized via switch 60 and switch 20 is closed. Thus switches 20 and 60 are operated periodically and synchronously. This allows the loop to relock and reestablish a loop control signal before too much error builds up in the VCO output frequency due to drift.

This FIGURE 1 arrangement is highly suitable for use in a cellular radio such as a mobile telephone. Operated in a mobile telephone, power, on line 28, is normally interrupted to PLL 10 (after a period of initial lock). During the time when power to PLL 10 is disabled, switch 20 is opened and VCO 12 is controlled by the signal on capacitor 22. PLL 10 is automatically recurrently enabled. During such time of enablement, switch 20 is closed so that the magnitude of the control signal on line 11 is updated by capacitor 22. PLL 10 is continuously enabled in response to any of the following conditions:

- (a) a received command indicating a switch in frequency and transmission on the new frequency,
- (b) a received command calling for a transmission on the current frequency,
- (c) on off-hook condition, or
- (d) the loss of a received signal.

In the absence of any of conditions (a) through (d), above, the synthesizer is returned to its normally PLL disabled state with switch 20 open and switch 60 open to interrupt power to PLL 10. During the time intervals the power to PLL 10 is interrupted by switch 60, considerable battery power is saved.

Referring now to FIGURE 2, there is shown a block diagram of an embodiment of the battery saving frequency synthesizer circuit according to the present invention. As in FIGURE 1 phase-locked loop 10 represents all of the phase-locked loop synthesizer components except for the VCO which is shown as a separate block 12. In this embodiment, the switch for switching between normal and battery saving modes of operation is a single pole double throw switch 40. In normal operation (non-battery save), a loop control signal on signal line 11 from phase-locked loop 10 is coupled through switch 40 to the input of an integrator 42. The integrator 42 is represented by an amplifier 44 in combination with a feedback capacitor 46. However, other integrators will serve the same purpose. The output of integrator 42 is coupled to control input 26 of VCO 12. As in FIGURE 1, the output of VCO 12, which is the synthesizer output, is coupled on signal line 18 to a phase comparator (or divider) within phase-locked loop 10.

In this embodiment, during battery save operation, the phase-locked loop 10 is held close to lock by an FM receiver 48 and discriminator 50. Thus, this embodiment is highly suitable for use in receivers or transceivers in mobile or portable communication.

Because the loop control signal of signal line 11 from phase-locked loop 10 is coupled to control input 26 of the VCO 12 through an integrator 42, the phase-locked loop error signal must produce a zero error signal when locked. Thus, when locked, the magnitude of the VCO control signal applied to control input 26 will not change. Only when the signal on line 11 from phase-locked loop 10 deviates from zero will the control input to VCO 12 change.

A properly designed FM receiver 48 using an S-type discriminator can produce a DC voltage proportional to deviation between its local oscillator frequency and signal frequency as received through it and antenna 52. This DC voltage produced by FM receiver 48 and discriminator 50, known as the automatic frequency control (AFC) signal is coupled to the second throw of switch 40 and is utilized to control the phase-locked loop during battery save operation.

During battery save operation, switch 40 is switched so that the AFC output of discriminator 50 is coupled to the input of integrator 42, and power to phase-locked loop 10 via line 28 is interrupted by the opening of switch 60. During such power interruption periods, the AFC output of discriminator 50 maintains an appropriate control signal on VCO 12 unless the signal received by receiver 48 is lost or until it is desired to change received channels.

In the context of operation of the FIGURE 2 embodiment in a cellular radio such as a mobile telephone, power to PLL 10 is normally disabled after an initial lock of the phase-locked loop. During times of power interruption to PLL 10, discriminator 50 drives VCO 12. PLL 10 is enabled continuously in response to the occurrence of any of the following conditions:

- (a) a received command calling for a switch in frequency and transmission on the new frequency,
- (b) a received command calling for transmission on the current frequency,
- (c) an off-hook condition or
- (d) the loss of a received signal.

The synthesizer is returned to its normally PLL disabled state with discriminator control of VCO 12 in response to the absence or disappearance of any of conditions (a) through (d) above.

Thus, there has been provided a frequency synthesizer circuit arrangement highly suitable for mobile or portable use. During extended periods of time, power to the phase-locked loop is disabled thereby considerably extending battery life.

Of course, other alternative embodiments and modifications of the present invention will be apparent to those of ordinary skill in the art having the benefit of the teachings contained herein.

Therefore, such alternate embodiments and modifications are intended to be covered within the scope of the appended claims.

Claims

1. A frequency synthesizer circuit comprising:
a voltage controlled oscillator (12) having a control input (26);

an input phase-locked loop synthesizer means (10) for (a) comparing a signal output of said voltage controlled oscillator (12) with a signal from a reference oscillator and (b) providing a loop control signal related thereto;

means (60) for interrupting power to the phase-locked loop synthesizer means (10);

characterized by

switch means (40) for selectively coupling the input of the voltage controlled oscillator (12) to either the loop control signal from the phase-locked loop synthesizer means (10) when power is applied thereto or to a signal from a receiver discriminator (50), whenever power to the phase-locked loop synthesizer means (10) is interrupted, whereby the frequency of the voltage controlled oscillator (12) is controlled by the receiver discriminator signal during periods of power interruption to the phase-locked loop synthesizer means (10).

2. A frequency synthesizer circuit according to claim 1, characterized in that said switch means (40) is coupled to the input of said voltage controlled oscillator (12) through an integrator (42).

3. A method for frequency synthesizing comprising the steps of:

generating, with phase-locked loop means (10), a loop control signal for use in controlling a voltage controlled oscillator (12) associated with the phase-locked loop means;

locking the phase-locked loop (10);

interrupting power to the phase-locked loop means (10);

characterized by

decoupling the control input (26) of the voltage controlled oscillator (12) from the phase-locked loop means (10) and coupling it instead to the output of a receiver discriminator (50) so that the voltage controlled oscillator (12) will be controlled by the discriminator output rather than the loop control signal from the phase-locked loop means (10).

4. A method according to claim 3 for operating radio communications equipment having a phase-locked loop synthesizer including phase-locked loop (PLL) means and a voltage controlled oscillator (VCO) wherein the equipment includes a receiving section having a discriminator,

characterized by:

(a) locking the PLL means (10) to provide a loop control signal to the VCO (12);

(b) normally interrupting power to the PLL means (10) and a coupling signal from the discriminator (50) to the control input of the VCO to

control its frequency during the time period when the PLL is disabled;

(c) enabling the PLL continuously in response to the occurrence of any of the following conditions:

(aa) a received command calling for a switch in frequency and transmission on the new frequency,

(bb) a received command calling for transmission on the current frequency,

(cc) an off-hook condition, or

(dd) loss of a received signal;

(d) returning to the normally PLL disabled state wherein the output of the discriminator (50) drives the VCO (12) in response to the absence of any of the conditions (aa) through (dd) above.

Patentansprüche

1. Frequenzsynthesizerschaltung enthaltend:

einen spannungsgesteuerten Oszillator (12) mit einem Steuereingang (26);

einem PLL-(phase-locked loop)-Synthesizer (10) zum (a) Vergleichen des Ausgangssignals des spannungsgesteuerten Oszillators (12) mit einem Signal von einem Referenzoszillator und (b) zum Liefern eines darauf bezogenen Schleifensteuersignals;

Mittel (60) zum Unterbrechen der Stromzufuhr zum PLL-Synthesizer (10),

gekennzeichnet durch

eine Schalteinrichtung (40) zum selektiven Verbinden des Eingangs des spannungsgesteuerten Oszillators (12) mit entweder dem Schleifensteuersignal von dem PLL-Synthesizer (10), wenn Strom zugeführt wird, oder mit einem Signal von einem Empfängerdiskriminator (50), wenn die Stromzufuhr zum PLL-Synthesizer (10) unterbrochen ist, wodurch die Frequenz des spannungsgesteuerten Oszillators (12) durch das Empfängerdiskriminatordesignal während der Perioden der Stromunterbrechung zum PLL-Synthesizer (10) gesteuert ist.

2. Frequenzsynthesizerschaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Schalteinrichtung (40) mit dem Eingang des spannungsgesteuerten Oszillators (12) über einen Integrator (42) verbunden ist.

3. Verfahren zur Frequenzsynthesisierung mit den Schritten:

Erzeugung, mit einer phasenstarren, Schleife (10), eines Schleifensteuersignals zur Verwendung bei der Steuerung eines spannungsgesteuerten Oszillators (12), der der phasenstarren Schleife zugeordnet ist,

Verriegeln der phasenstarren Schleife (10),

Unterbrechen der Stromzufuhr zur phasenstarren Schleife (10),

gekennzeichnet durch

Trennen des Steuereingangs (26) des spannungsgesteuerten Oszillators (12) von der phasenstarren Schleife (10) und Verbinden des Steuereingangs (26) stattdessen mit dem Ausgang eines Empfängerdiskriminatordesignals (50), so daß der spannungsgesteuerte Oszillator (12) durch das Diskriminatordesignal gesteuert ist

Therefore, such alternate embodiments and modifications are intended to be covered within the scope of the appended claims.

Claims

1. A frequency synthesizer circuit comprising:
a voltage controlled oscillator (12) having a control input (26);

an input phase-locked loop synthesizer means (10) for (a) comparing a signal output of said voltage controlled oscillator (12) with a signal from a reference oscillator and (b) providing a loop control signal related thereto;

means (60) for interrupting power to the phase-locked loop synthesizer means (10);

characterized by
switch means (40) for selectively coupling the input of the voltage controlled oscillator (12) to either the loop control signal from the phase-locked loop synthesizer means (10) when power is applied thereto or to a signal from a receiver discriminator (50), whenever power to the phase-locked loop synthesizer means (10) is interrupted, whereby the frequency of the voltage controlled oscillator (12) is controlled by the receiver discriminator signal during periods of power interruption to the phase-locked loop synthesizer means (10).

2. A frequency synthesizer circuit according to claim 1, characterized in that said switch means (40) is coupled to the input of said voltage controlled oscillator (12) through an integrator (42).

3. A method for frequency synthesizing comprising the steps of:

generating, with phase-locked loop means (10), a loop control signal for use in controlling a voltage controlled oscillator (12) associated with the phase-locked loop means;

locking the phase-locked loop (10);

interrupting power to the phase-locked loop means (10);

characterized by

decoupling the control input (26) of the voltage controlled oscillator (12) from the phase-locked loop means (10) and coupling it instead to the output of a receiver discriminator (50) so that the voltage controlled oscillator (12) will be controlled by the discriminator output rather than the loop control signal from the phase-locked loop means (10).

4. A method according to claim 3 for operating radio communications equipment having a phase-locked loop synthesizer including phase-locked loop (PLL) means and a voltage controlled oscillator (VCO) wherein the equipment includes a receiving section having a discriminator, characterized by:

(a) locking the PLL means (10) to provide a loop control signal to the VCO (12);

(b) normally interrupting power to the PLL means (10) and a coupling signal from the discriminator (50) to the control input of the VCO to

control its frequency during the time period when the PLL is disabled;

(c) enabling the PLL continuously in response to the occurrence of any of the following conditions:

(aa) a received command calling for a switch in frequency and transmission on the new frequency,

(bb) a received command calling for transmission on the current frequency,

(cc) an off-hook condition, or

(dd) loss of a received signal;

(d) returning to the normally PLL disabled state wherein the output of the discriminator (50) drives the VCO (12) in response to the absence of any of the conditions (aa) through (dd) above.

Patentansprüche

1. Frequenzsynthesizerschaltung enthaltend:
einen spannungsgesteuerten Oszillator (12) mit einem Steuereingang (26);

einem PLL-(phase-locked loop)-Synthesizer (10) zum (a) Vergleichen des Ausgangssignals des spannungsgesteuerten Oszillators (12) mit einem Signal von einem Referenzoszillator und (b) zum Liefern eines darauf bezogenen Schleifensteuersignals;

Mittel (60) zum Unterbrechen der Stromzufuhr zum PLL-Synthesizer (10),

gekennzeichnet durch
eine Schalteinrichtung (40) zum selektiven Verbinden des Eingangs des spannungsgesteuerten Oszillators (12) mit entweder dem Schleifensteuersignal von dem PLL-Synthesizer (10), wenn Strom zugeführt wird, oder mit einem Signal von einem Empfängerdiskriminator (50), wenn die Stromzufuhr zum PLL-Synthesizer (10) unterbrochen ist, wodurch die Frequenz des spannungsgesteuerten Oszillators (12) durch das Empfängerdiskriminatordesignal während der Perioden der Stromunterbrechung zum PLL-Synthesizer (10) gesteuert ist.

2. Frequenzsynthesizerschaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Schalteinrichtung (40) mit dem Eingang des spannungsgesteuerten Oszillators (12) über einen Integrator (42) verbunden ist.

3. Verfahren zur Frequenzsynthesisierung mit den Schritten:

Erzeugung, mit einer phasenstarren Schleife (10), eines Schleifensteuersignals zur Verwendung bei der Steuerung eines spannungsgesteuerten Oszillators (12), der der phasenstarren Schleife zugeordnet ist,

Verriegeln der phasenstarren Schleife (10),

Unterbrechen der Stromzufuhr zur phasenstarren Schleife (10),

gekennzeichnet durch

Trennen des Steuereingangs (26) des spannungsgesteuerten Oszillators (12) von der phasenstarren Schleife (10) und Verbinden des Steuereingangs (26) stattdessen mit dem Ausgang eines Empfängerdiskriminatordesignals (50), so daß der spannungsgesteuerte Oszillator (12) durch das Diskriminatordesignal gesteuert ist



statt durch das Schleifensteuersignal von der phasenstarrten Schleife (10).

4. Verfahren nach Anspruch 3 zum Betreiben eines Gerätes für drahtlose Verbindungen mit einem PLL-(phase-locked loop)-Synthesizer mit einem Phasenregelkreis und einem spannungsgesteuerten Oszillator, wobei das Gerät einen Empfangsabschnitt mit einem Diskriminator aufweist,

gekennzeichnet durch:

(a) Verriegeln des Phasenregelkreises (10) zur Lieferung eines Schleifensteuersignals an den spannungsgesteuerten Oszillator (12);

(b) normalerweise Unterbrechen der Stromzufuhr zu dem Phasenregelkreis (10) und Anlegen eines Signals von dem Diskriminator (50) an den Steuereingang des spannungsgesteuerten Oszillators, um dessen Frequenz während der Zeitperiode zu steuern, während der der Phasenregelkreis gesperrt ist;

(c) Freigeben des Phasenregelkreises ständig auf das Auftreten irgendeiner der folgenden Bedingungen hin:

(aa) einen empfangenen Befehl, der eine Umschaltung der Frequenz und das Senden auf der neuen Frequenz verlangt,

(bb) einen empfangenen Befehl, der das Senden auf der gegenwärtigen Frequenz verlangt,

(cc) einen Hörer-abgehoben-Zustand oder

(dd) Verlust eines empfangenen Signals;

(d) Zurückkehren zu dem Zustand der normalerweise gesperrten Phasenregelschleife, wobei das Ausgangssignal des Diskriminators (50) den spannungsgesteuerten Oszillator (12) auf das Nichtvorhandensein irgendeiner der vorstehenden Bedingungen (aa) bis (dd) hin steuert.

Revendications

1. Un circuit synthétiseur de fréquence comprenant:

un oscillateur commandé par tension (12) ayant une entrée de commande (26);

des moyens synthétiseurs à boucle de verrouillage de phase (10) ayant pour fonctions (a) de comparer un signal de sortie de l'oscillateur commandé par tension (12) avec un signal provenant d'un oscillateur de référence et (b) de produire un signal de commande boucle lié à celui-ci;

des moyens (60) destinés à interrompre l'alimentation des moyens synthétiseurs à boucle de verrouillage de phase (10);

caractérisé par

des moyens de commutation (40) destinés à appliquer sélectivement à l'entrée de l'oscillateur commandé par tension (12) soit le signal de commande de boucle provenant des moyens synthétiseurs à boucle de verrouillage de phase (10), lorsqu'ils sont alimentés, soit un signal provenant d'un discriminateur de récepteur (50), chaque fois que l'alimentation des moyens synthétiseurs à boucle de verrouillage de phase (10) est interrompue, grâce à quoi la fréquence de l'oscillateur commandé par tension (12) est com-

mandée par le signal du discriminateur de récepteur pendant les périodes d'interruption de l'alimentation des moyens synthétiseurs à boucle de verrouillage de phase (10).

2. Un circuit synthétiseur de fréquence selon la revendication 1, caractérisé en ce que les moyens de commutation (40) sont connectés à l'entrée de l'oscillateur commandé par tension (12) par l'intermédiaire d'un intégrateur (42).

3. un procédé pour la synthèse de fréquence comprenant les opérations suivantes:

on gère, avec une boucle à verrouillage de phase (10), un signal de commande de boucle destiné à être utilisé pour la commande d'un oscillateur commandé par tension (12) qui est associé à la boucle de verrouillage de phase;

on verrouille la boucle de verrouillage de phase (10);

on interrompt l'alimentation de la boucle de verrouillage de phase (10);

caractérisé en ce que

on déconnecte l'entrée de commande (26) de l'oscillateur commandé par tension (12) de la boucle de verrouillage de phase (10), et on la connecte à la place à la sortie d'un discriminateur de récepteur (50), de façon que l'oscillateur commandé par tension (12) soit commandé par le signal de sortie du discriminateur, au lieu de l'être par le signal de commande de boucle provenant de la boucle de verrouillage de phase (10).

4. Un procédé selon la revendication 3 pour faire fonctionner un équipement de radiocommunication comportant un synthétiseur à boucle de verrouillage de phase qui comprend une boucle de verrouillage de phase et un oscillateur commandé par tension (OCT), dans lequel l'équipement comprend une section de réception ayant un discriminateur,

caractérisé en ce que:

(a) on verrouille la boucle de verrouillage de phase (10) pour appliquer un signal de commande de boucle à l'OCT (12);

(b) on interrompt normalement l'alimentation de la boucle de verrouillage de phase (10) et on applique un signal provenant du discriminateur (50) à l'entrée de commande de l'OCT pour commander sa fréquence pendant la période au cours de laquelle la boucle de verrouillage de phase est hors fonction;

(c) on met continuellement en fonction la boucle de verrouillage de phase sous l'effet de l'apparition de l'une quelconque des conditions suivantes:

(aa) la présence d'un ordre reçu demandant une commutation de fréquence et l'émission sur la nouvelle fréquence,

(bb) la présence d'un ordre reçu demandant l'émission sur la fréquence courante,

(cc) un état décroché, ou

(dd) la perte d'un signal reçu;

(d) on retourne à l'état normal dans lequel la boucle de verrouillage de phase est hors fonction et dans lequel la sortie du discriminateur (50) attaque l'OCT (12) sous l'effet de l'absence de l'ensemble des conditions (aa) à (dd) ci-dessus.

