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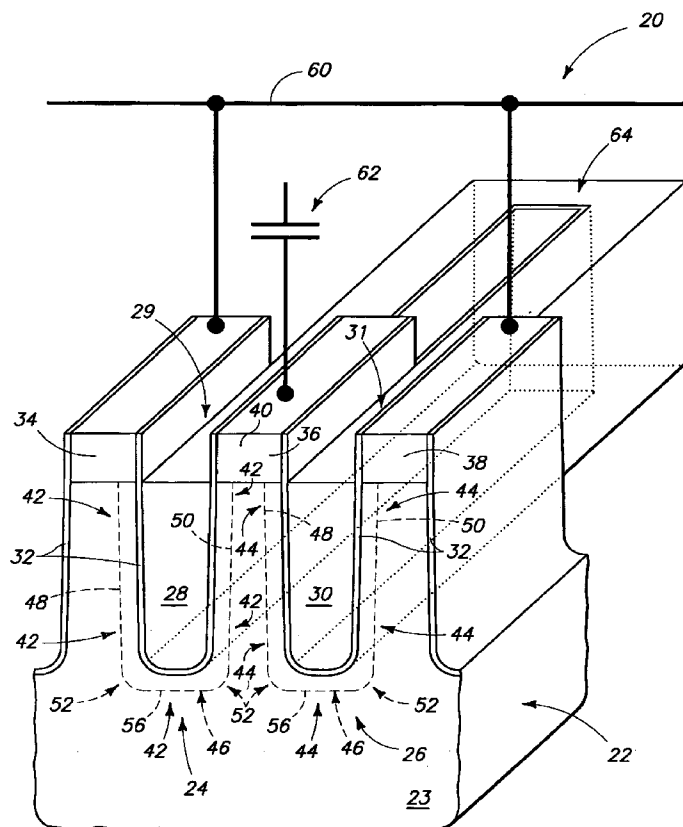
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(54) Title: DRAM TRANSISTOR WITH RECESSED GATES AND METHODS OF FABRICATING THE SAME



(57) Abstract: A memory array includes a plurality of memory cells (20) formed on a semiconductor substrate (22). Individual of the memory cells include first (24) and second (26) field effect transistors respectively comprising a gate (28/30), a channel region, and a pair of source/drain regions. The gates of the first and second field effect transistors are formed in openings in the substrate and are hard wired together. A conductive data line (60) is formed in an opening in the substrate and is hard wired to two of the source/drain regions. A charge storage device (62) is hard wired to at least one of the source/drain regions other than the two.



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- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*