

TIMING CIRCUIT UTILIZING A
CLOCK TREE AS A DELAY DEVICE

ABSTRACT OF THE DISCLOSURE

A timing circuit (60) that utilizes the delay inherent in a clock tree (70,80) to achieve a desired timing relationship between control or clock signals. The timing circuit is particularly applicable to high speed environments and to asynchronous logic (90), though it is also applicable to lower speed environments and synchronous logic (90). A method producing the desired control or clock signals is also disclosed.

Figure 2