WHAT IS CLAIMED IS

1. A memory device, comprising:

a stack structure over a substrate, the stack structure comprising one or more drain-select gate (DSG) lines;

a channel structure extending in the stack structure;

a dielectric layer over the channel structure, the dielectric layer comprising a first material;

a drain-select gate (DSG) cut structure in contact with the one or more DSG lines, wherein the DSG cut structure comprises a second material different from the first material, and

a contact above and in contact with the channel structure, wherein the contact is in the dielectric layer and is in contact with the DSG cut structure, wherein the contact is formed of a conductive material.

2. The memory device of claim 1, wherein the DSG cut structure extends through the dielectric layer; and wherein the DSG cut structure is in contact with the channel structure, and the stack structure comprises a plurality of conductive layers, wherein the plurality of conductive layers comprises the one or more DSG lines.

3. The memory device of claim 1 or 2, wherein an etching selectivity of the first material over the second material is greater than 1.

4. The memory device of any one of claims 1-3, wherein the first and second materials each comprises a respective dielectric material.

5. The memory device of each one of claims 1-4, wherein the first material comprises silicon oxide and the second material comprises silicon nitride.

6. The memory device of any one of claims 1-5, wherein the DSG cut structure does not comprise silicon oxide.

7. The memory device of claim 6, where the DSG cut structure comprises silicon nitride.

8. The memory device of any one of claims 1-5, wherein the DSG cut structure comprises a liner silicon oxide layer and a silicon nitride layer surrounded by the liner silicon oxide layer.

9. The memory device of claim 8, wherein the DSG cut structure comprises a silicon nitride layer surrounded by the liner silicon oxide layer, and a filler layer surrounded by the silicon nitride layer.

10. The memory device of claim 9, wherein the filler layer comprises an airgap.

11. The memory device of any one of claims 1-10, further comprises a pair of source contact structures extending in a lateral direction and a memory block between the pair of source contact structures, the memory block comprising a plurality of memory cells in a plurality of channel structures between the source contact structures, wherein

the memory block comprises a pair of strings adjacent to each other, each of the strings comprising a plurality of rows of channel structures in the lateral direction, and

the DSG cut structure, extending in the lateral direction, is between the pair of strings and is in contact with at least one of the rows of the channel structures.

12. The memory device of claim 11, wherein each of the strings comprises four rows of channel structures.

13. A memory system, comprising:

a memory device configured to store data, the memory device comprising:

a stack structure over a substrate, the stack structure comprising one or more drain-select gate (DSG) lines,

a channel structure extending in the stack structure,

a dielectric layer over the channel structure, the dielectric layer comprising a first material,

a drain-select gate (DSG) cut structure in contact with the one or more DSG lines, wherein the DSG cut structure comprises a second material different from the first material, and

a contact above and in contact with the channel structure, wherein the contact is in the dielectric layer and is in contact with the DSG cut structure, wherein the contact is formed of a conductive material; and

a memory controller coupled to the memory device and configured to control operations of the channel structure.

14. A method for forming a memory device, comprising:

forming a stack structure over a substrate and forming one or more drain-select gate (DSG) lines in the stack structure;

forming a channel structure extending in the stack structure;

depositing a first material to form a dielectric layer over the channel structure;

patterning the dielectric layer and the stack structure to form an opening, the opening in contact with a conductive layer in a top portion of the stack structure;

depositing a second material into the opening to form a drain-select gate (DSG) cut structure and contacting the DSG cut structure with the one or more DSG lines, the second material being different from the first material; and

forming a contact in the dielectric layer above and in contact with the channel structure after the DSG cut structure is formed in the stack structure, wherein forming the contact in the dielectric layer includes etching the dielectric layer to form another opening in contact with the channel structure and the DSG cut structure, and depositing a conductive material to fill the other opening.

15. The method of claim 14, wherein the opening is through the dielectric layer; and wherein the opening is in contact with the channel structure.

16. The method of claim 14 or 15, wherein depositing the first material comprises depositing silicon oxide.

17. The method of any one of claims 14-16, wherein depositing the second material to form the DSG cut structure comprises depositing silicon nitride.

18. The method of claim 17, wherein depositing the second material to form the DSG cut structure comprises depositing the silicon nitride to fill the opening.

19. The method of claim 17, wherein depositing the second material to form the DSG cut structure comprises:

depositing a liner oxide layer in the opening, the liner oxide layer in contact with surfaces of the opening; and

depositing a silicon nitride layer to fill the opening.

20. The method of claim 17, wherein depositing the second material to form the DSG cut structure comprises:

depositing a liner oxide layer in the opening, the liner oxide layer in contact with surfaces of the opening;

depositing a silicon nitride layer over the liner oxide layer; and

forming an air gap in the silicon nitride layer during the deposition of the silicon nitride layer.