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(54) OHMIC CONTACT AND ELECTRICAL LEAD FOR SEMICONDUCTOR DEVICES

(71) We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices and provision of combined electrical leads and ohmic contacts therefor. More particularly, the invention relates to integrated circuits having circuit components connected by an ohmic contact and electrical lead arrangement which forms a first level interconnection pattern and is connected at one or more selected locations to a second level interconnection pattern separated from the first level pattern by electrical insulation; the second level interconnection pattern may itself be connected to further levels of interconnection patterns separated by layers of electrical insulation. The increased demand for microminiaturization has been reflected in the field of electronics by the development of semiconductor integrated circuits or networks, whereby a plurality of active and/or passive circuit components are formed in or on a single slice of semiconductor material, each of the circuit components thereafter being interconnected in a particular manner to provide the desired circuit function. For example, an integrated circuit device of the monolithic type may have a number of transistors and resistors formed by diffusion beneath one major face of a slice or wafer of semiconductor material (a suitable one being silicon), a protective layer (usually of silicon oxide) upon the face of the wafer, and metallic films upon the oxide layer interconnecting the resistors and the various regions of the

transistors in a desired pattern through apertures in this oxide. With increasing complexity of circuitry, however, and the corresponding increase in complexity of the interconnection pattern, it has become necessary to form more than one level of metallic film interconnections, with adequate electrical insulation or isolation between the various levels at the cross-over points. This is particularly true when, upon a single slice of semiconductor material, a plurality of separate circuits are formed and it becomes necessary to interconnect the circuits for cooperative action to produce one unitary circuit function.

The materials of which the metal films and the electrical insulating layer or layers are formed must in themselves exhibit favorable chemical, electrical, thermal, and mechanical properties, including compatibility with one another to provide an adequate multi-level contact and interconnection system. For example, the metallic film or films of the first level should provide low resistance ohmic contact to the semiconductor material should adhere well to the protective layer of oxide upon the face of the slice or wafer, should not excessively alloy with the semiconductor material at temperatures encountered in the processing or packaging of the device so as to degrade device characteristics, and should not have a melting point below the temperature to which the device will be exposed during processing and device operation. The insulating material between levels of metal films, on the other hand, should afford adequate electrical isolation and be substantially free of pinholes to avoid the possibility of electrical shorting between levels. In addition, the entire system should be fabricated of metals and insulators or oxides which are hard, structurally strong materials that will not yield or break up during wafer or slice handling and testing;

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all of the materials should be physically and chemically stable when subjected to high temperatures so that none of the materials will undesirably react with one another or
5 with the semiconductor substrate; the metals and the isolation or insulation medium should tightly adhere to one another and there should be good "interlevel" ohmic contact between the last or exposed metallic
10 film of one level and the first film of the next level at conductive cross points.

In the embodiments of this invention to be described, use is made of molybdenum and gold in combination because of the
15 many superior properties that this combination offers. A detailed description of some of these properties appears in British Patent Specification No. 1104804, some of the most favorable ones including the fact that
20 molybdenum makes good electrical contact to silicon semiconductor material, particularly if the contact regions are heavily doped, but yet does not undesirably alloy with the silicon surface so as to degrade
25 the device. Furthermore, the molybdenum adheres well to silicon oxide, can be etched in a controlled manner with an etchant not incompatible with other materials used during the fabrication process, and when used
30 in combination with gold is virtually impervious to the gold. In this regard, it is to be noted that when molybdenum is formed in contact with the silicon semiconductor material and a gold layer overlies the molybdenum, there results a virtually "alloyless"
35 contact system, the molybdenum not alloying with the silicon and the gold not alloying with the molybdenum. Gold, in addition to its excellent conductivity, is easily deposited by conventional evaporation techniques, lends itself nicely to photo-resist
40 etch procedures associated with defining the contact and interconnection patterns and, is easily bondable with an external gold wire.

In addition, the molybdenum-gold contact system is not subject to increasing electrical resistivity due to the inter-diffusion or compound formation associated with many other metallic film combinations. For example, copper wire manufacturers go to
50 great expense to provide ultra high purity copper to obtain high conductivity. This may be explained on the basis that any impurity atoms in even a relatively pure metal
55 tend to scatter the moving electrons in the metal, thus increasing their resistance to current flow. This, however, is not present in the molybdenum-gold film combination because molybdenum and gold have very low
60 mutual solubilities (so that interdiffusion is concentration limited) and also because they form no compounds with one another.

The molybdenum-gold system also offers reliability advantages in high current-density applications. It has been observed that

expanded ohmic contacts for integrated circuits and discrete transistors, for example, become electrically open-circuit after prolonged operation at current densities of the order of 1×10^6 A/cm² or higher, thus
70 causing device failure. This failure mechanism is believed related to a phenomenon termed current-induced mass transport, the rate of which is approximately inversely
75 proportional to the activation energy of self diffusion of the particular metal conductor or conductors involved. It has been observed that some metals which have low values of activation energy, aluminum for example,
80 have a greater reliability risk associated with them than other metals which have higher values of activation energy. Gold and particularly molybdenum, on the other hand, have very high values of this activation
85 energy of self diffusion, and thus have minimal susceptibility to current-induced mass transport problems.

The invention provides a semiconductor device having at least one semiconductor region extending to one face of a substrate
90 having a protective coating of insulating material thereon, and an electrical lead and ohmic contact which is ohmically connected to that semiconductor region through an aperture in the protective coating and which
95 extends on to the protective coating, the lead and contact arrangement comprising overlying films of, respectively, molybdenum, gold, and molybdenum. In a particular embodiment, a further protective coating of
100 insulating material overlies the said lead and contact and has an opening therein above the underlying lead and contact through which opening and a corresponding
105 opening in the underlying adjacent molybdenum film, an electrical connection is made directly to the gold film of the said lead and contact.

More particularly, the invention provides an integrated circuit device comprising: a
110 plurality of circuit elements disposed at a common surface of a substrate, each circuit element including at least one semiconductor region, the semiconductor regions being covered by a protective coating of insulating
115 material disposed on the common face of the substrate, and electrically interconnecting selected ones of the semiconductor regions, an ohmic contact and electrical lead arrangement comprising overlying films of,
120 respectively, molybdenum, gold and molybdenum, the lead and contact arrangement being disposed on the protective coating and making ohmic connection with the said selected regions through apertures in the
125 protective coating.

In such an integrated circuit device, the ohmic contact and electrical lead arrangement can form a first level interconnection and include a portion extending over the
130

protective coating to a selected position; a second level interconnector can be ohmically connected with the said portion of the first level interconnection at the selected position whilst being isolated from other parts of the first level interconnection by an interposed layer of electrical insulation which may include a genetic film of molybdenum oxide formed on the molybdenum film of the first level interconnection outermost from the substrate. The second level interconnector can comprise a film of molybdenum disposed on the insulating medium and overlaid by a film of gold, the molybdenum film of the second level interconnector directly contacting the gold film of the said portion of the first level interconnection at the selected position thereon.

Reference in the preceding paragraphs to "molybdenum" and "gold" is to be construed as including the inclusion of added trace impurities e.g. to improve the adherence thereof. The invention also provides specific methods for providing multi-level ohmic contacts and electrical interconnections in a semiconductor integrated circuit of the type having a plurality of circuit components formed as integral parts of a body, by semiconductor regions defining pn junctions extending to a surface of the body beneath the protective coating upon that surface.

By way of example, embodiments of the invention will now be described in greater detail with reference to the accompanying drawings, in which:

FIGURE 1 is a plan view, greatly enlarged, of a semiconductor wafer or slice containing a plurality of electrical circuit functional elements and suitable for carrying out this invention:

FIGURE 2 is a circuit diagram of one of the functional elements shown in FIGURE 1;

FIGURE 3 is a plan view, greatly enlarged, of the layout of circuit components in one of the functional elements in the wafer of FIGURE 1, these same circuit components being illustrated in schematic diagram form in FIGURE 2;

FIGURES 4-6 are sectional views of a portion of the integrated circuit structure shown in FIGURE 3 taken along the section line 4-4, showing subsequent steps in a provision of the multi-level interconnection system which is the subject of our co-pending application No. 13609/70 (Serial No. 1203087); and

FIGURES 7a and 7b are also partial views, in section, of the same sectional portion described with respect to FIGURES 4-6, but describing an embodiment of the present invention;

All of the figures are not necessarily to scale, but in some instances relative dimen-

sions have been exaggerated to emphasize particular features of the invention.

Referring now to the drawings, a slice or wafer substrate 10 of semiconductor material, in this case silicon semiconductor material, is illustrated in FIGURE 1, having a number of electrical circuit functional elements therein. Although only sixteen such functional elements are shown for illustration, ordinarily a much larger number is utilized. Each of the functional elements 11-26 contains the necessary number of transistors, resistors, capacitors or other components, interconnected to produce a desired electrical circuit function. For example, the functional element 13 may comprise the circuit shown schematically in FIGURE 2 and by plan view in FIGURE 3. The circuit of this functional element 13 would then include the P-N-P transistors 32, 33, 34 and 35 and the N-P-N transistors 36, 37, 43, 45, 46, 47 and 50, the three input terminals A, B, and X and an output terminal G. These terminals, along with the voltage supply terminal V, would correspond to the five identically designated terminals on the functional element 13 in FIGURE 1.

Let us assume that it is desired to appropriately interconnect the four functional elements 13, 16, 21 and 26 of the sixteen functional elements 11-26 for their cooperative action to produce a unitary electrical function. As depicted in FIGURE 1, therefore, the terminals B, D, J, and O of functional elements 13, 16, 21 and 26, respectively, are electrically joined by the interconnector 28; similarly, the terminals V, F, L and R are electrically joined by the interconnector 29, and the terminals X, H, M and Q are electrically joined by the interconnector 30. Recognizing that there are already a large number of first level electrical interconnections joining the various transistors with one another as well as with the other circuit components and terminals, as shown in FIGURE 3, it will be appreciated that the interconnectors 28, 29 and 30 must necessarily overlie some of the first level metal interconnection pattern shown in FIGURE 3. For this reason, and also because the interconnections between functional elements are preferably made in an operation separate from the one by which the interconnections within an element are formed, the interconnection pattern of FIGURE 1 must necessarily be formed as a second level, separated from the first level interconnection pattern by an insulating medium.

The transistors and the other circuit components may be formed within or upon the semiconductor substrate 10 by any of the techniques known in the integrated circuit art such as, for example, epitaxial growth or diffusion. Thus, looking at FIGURE 4

there is depicted, in section, a portion of the integrated circuit structure of FIGURE 3 before the application of any of the metal interconnectors. The N-P-N transistor 36 comprises an N-type collector formed by the substrate 10, the diffused P-type base region 51, and an N-type diffused emitter region 52. The resistor R_1 is provided by the P-type diffused region 53, formed simultaneously with the base region 51 of the transistor. An oxide coating 54 on the top surface of the substrate acquires a stepped configuration, as shown, due to the successive diffusion operations. Thereafter apertures or holes are cut in the oxide coating 54 where the first level interconnection ohmic contacts are to be made.

As the next step, a thin metal film 55 of 20,000 angstroms, for example, formed of molybdenum, one of the better electrical conductors, (see FIGURE 5) is deposited upon the surface of the oxide layer 54 and in ohmic contact with the semiconductor material within the apertures or holes in the oxide layer. Various techniques may be utilized for the deposition of the molybdenum film 55, for example sputtering, evaporation, or sublimation; one evaporation technique being described more particularly in British Patent Specification No. 1104804. Using conventional photographic masking and etching techniques known in the industry, selected portions of the molybdenum film 55 are removed to provide the first level pattern of ohmic contacts and interconnections, the interconnector 71 ohmically connecting the base of the transistor 36 to one end of the resistor R_1 , the interconnector 72 making ohmic contact to the transistor 36 emitter; while the interconnector 73 ohmically connects the collector of the transistor 36 to the supply terminal V, as illustrated in FIGURE 5.

A layer 56 of insulating medium is then deposited by any suitable technique, for example evaporation, sputtering or electron beam deposition, over the molybdenum film 55, and then selectively etched to expose the surface of the molybdenum film solely at the terminal point V, as depicted in FIGURE 6. The purpose of the insulating layer 56 is to electrically isolate the metal of the first level interconnectors from the metal of the second level interconnectors which are to be subsequently deposited. Accordingly, the layer 56 may be formed of inorganic materials such as silicon nitride, aluminum oxide, tantalum oxide, or various organic insulating materials. In this particular example the insulating layer 56 is silicon dioxide, deposited by RF sputtering to a thickness of 10,000 angstroms. The layer is then selectively removed to expose the top surface of the molybdenum film 55 at the bonding pad V.

Another molybdenum film 57 is now deposited upon the insulating oxide layer 56 to a thickness of, say, 1200 angstroms, followed by the deposition by evaporation, for example, of a gold film 58, formed to a thickness of approximately 7500 angstroms, for example. The metal films 57 and 58 are then selectively etched to provide the pattern for the second level interconnector 29, the inter-level contact being provided at the bonding pad V between the molybdenum films 57 and 55, respectively. The top layer 58, being of gold, has an extremely high conductivity and adheres well to the molybdenum film 57. An external bonding wire of gold, for example, may then be bonded by thermocompression to the gold film 58. Among the advantages of this system, as illustrated in FIGURE 6, is the extremely good adherence of the molybdenum layers or films 55 and 57 to the insulating layer 56. If a three, four, or a higher level contact and interconnection system is desired, each of the levels besides the final one could be of a pure molybdenum film with the final level being a molybdenum-gold combination, the overlying layer of gold facilitating bonding with an external wire.

Prior to the deposition of the molybdenum film 57, it may be desirable to carry out a careful pre-deposition cleanup, for example by sputter-cleaning, of the surface of the insulating film 56 and the exposed surface of the molybdenum film 55. This cleaning minimizes or eliminates any surface oxides that may have formed upon the exposed surface of the molybdenum film 55, thus insuring good inter-level ohmic contact between the molybdenum films 55 and 57, as well as the adherence of the molybdenum film 57 to the insulating film 56.

In accordance with an embodiment of the present invention, the single layer of molybdenum of the first level patterns 71, 72 and 73 is replaced by a three layer sandwich structure indicated in FIGURES 7a and 7b. Such a structure comprises a first thin film 55a of molybdenum formed to a thickness of 1200 angstroms, ohmically engaging the semiconductor material 10, and overlying the protective oxide layer 54, a second thin film 55b of a gold deposited to a thickness of 7500 angstroms, and a third layer 55c of molybdenum deposited to a thickness of 1000 angstroms. The final level of metalization overlying the insulating medium then comprises the films 57 and 58 of molybdenum and gold, respectively, as previously described with respect to FIGURE 6. The insulating layer 56 and the molybdenum layer 55c are selectively etched at the bonding pad V to allow the molybdenum layer 57 to make direct ohmic contact to the gold film 55b. By utilizing an

etchant that selectively etches molybdenum but substantially unaffected gold, for example one comprised of 70 parts phosphoric acid, 15 parts acetic acid, 3 parts nitric acid, and 1 parts deionized water by volume, it is possible to carefully control this selective removal step at the bonding pad V so that the gold layer 55b is not etched all the way through. In addition, a color change accompanies this etching operation (from a silver color to a gold color) and provides a convenient visual control over the etching operation. The molybdenum films 55c and 57 tightly adhere to the insulating layer 56 and increase the interfilm adhesion of the entire multi-level interconnection system. The replacement of the single film 55 of molybdenum by the tri-metal sandwich structure molybdenum-gold-molybdenum has the additional advantages of increasing the first level interconnection electrical conductivity due to the addition of the highly conductive gold film 55b and of decreasing the inter-level electrical contact resistance between the first and second level due to the direct ohmic contact between the molybdenum film 57 of the second level interconnector and the exposed surface portion of the gold film 55b of the first level.

A double oxide or insulating layer between multilevels may be obtained by oxidizing a surface portion of the molybdenum film 55c illustrated in the drawing of FIGURES 7a and 7b prior to the deposition of the insulating layer 56. The final structure would then be as shown in FIGURES 7a and 7b but there would be additionally a genetically formed molybdenum oxide film overlying the top molybdenum film 55c of the molybdenum-gold-molybdenum multi-layer films of the first level. The top or final contact or level could then be formed by etching through the insulating layer 56, the molybdenum oxide film, and the molybdenum film 55c to expose the surface of the gold film 55b at the bonding pad V, and then depositing the next level of molybdenum film 57 and gold film 58, for example.

The molybdenum oxide film may be formed by placing the entire assembly in an oxygen atmosphere for about ten minutes at approximately 400°C to thermally oxidize the surface of the molybdenum film 55c, thus forming a molybdenum oxide insulating skin, a few thousand angstroms thick. The resulting structure has the advantage of two distinctly different insulating layers or oxides sandwiched together to avoid any congruent pin holes, thereby increasing the electrical isolation between the levels of interconnectors. In addition, it is to be particularly noted that the oxidation of the molybdenum layer or film 55c provides isolation or insulation not only at the

top of this layer but also around edges of the film, thereby additionally increasing the electrical isolation.

Various modifications of the above described embodiments and processes may be utilized in accordance with the invention. For example, it may be desirable to perform very shallow diffusions of impurities at the points of contact between the molybdenum film (films) and the semiconductor surface to provide low resistance ohmic contacts at these points. In addition, instead of depositing the molybdenum film directly upon the semiconductor surface, regions or zones of metallic material may be deposited intermediate the silicon surface and the molybdenum film. These metallic regions may be, for example, platinum-silicide deposits formed in the contact areas prior to the deposition of the molybdenum film, or a flash or very thin layer of aluminum applied prior to the deposition of the molybdenum film. Further, it is to be understood that throughout the above description the use of the metals molybdenum and gold are to include not only pure molybdenum and gold layers, but also molybdenum and gold layers that may have a minor percentage of impurities added thereto. For example, trace impurities may be added to the molybdenum film to increase its adherence and the gold films may have a minor percentage of platinum added thereto to increase the adhesion of the gold to the molybdenum.

While the embodiments and processes of the present invention have been directed toward monolithic integrated circuits and the application of multi-level interconnections to these monolithic integrated circuits, the processes and structures described above may have other applications such as in the areas of discrete semiconductor components and hybrid integrated circuits, for example, whenever it is desired to provide alternating layers or films of metal and electrical insulating material. Various other modifications of the disclosed processes and embodiments will become apparent to persons skilled in the art without departing from the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

A semiconductor device having at least one semiconductor region extending to one face of a substrate having a protective coating of insulating material thereon, and an electrical lead and ohmic contact which is ohmically connected to that semiconductor region through an aperture in the protective coating and which extends on to the protective coating, the lead and contact arrangement comprising overlying films of, respectively, molybdenum, gold and molybdenum.



etchant that selectively etches molybdenum but substantially unaffected gold, for example one comprised of 70 parts phosphoric acid, 15 parts acetic acid, 3 parts nitric acid, and 5 parts deionized water by volume, it is possible to carefully control this selective removal step at the bonding pad V so that the gold layer 55b is not etched all the way through. In addition, a color change accompanies this etching operation (from a silver color to a gold color) and provides a convenient visual control over the etching operation. The molybdenum films 55c and 57 tightly adhere to the insulating layer 56 and increase the interfilm adhesion of the entire multi-level interconnection system. The replacement of the single film 55 of molybdenum by the tri-metal sandwich structure molybdenum-gold-molybdenum has the additional advantages of increasing the first level interconnection electrical conductivity due to the addition of the highly conductive gold film 55b and of decreasing the inter-level electrical contact resistance between the first and second level due to the direct ohmic contact between the molybdenum film 57 of the second level interconnector and the exposed surface portion of the gold film 55b of the first level.

A double oxide or insulating layer between multilevels may be obtained by oxidizing a surface portion of the molybdenum film 55c illustrated in the drawing of FIGURES 7a and 7b prior to the deposition of the insulating layer 56. The final structure would then be as shown in FIGURES 7a and 7b but there would be additionally a genetically formed molybdenum oxide film overlying the top molybdenum film 55c of the molybdenum-gold-molybdenum multi-layer films of the first level. The top or final contact or level could then be formed by etching through the insulating layer 56, the molybdenum oxide film, and the molybdenum film 55c to expose the surface of the gold film 55b at the bonding pad V, and then depositing the next level of molybdenum film 57 and gold film 58, for example.

The molybdenum oxide film may be formed by placing the entire assembly in an oxygen atmosphere for about ten minutes at approximately 400°C to thermally oxidize the surface of the molybdenum film 55c, thus forming a molybdenum oxide insulating skin, a few thousand angstroms thick. The resulting structure has the advantage of two distinctly different insulating layers or oxides sandwiched together to avoid any congruent pin holes, thereby increasing the electrical isolation between the levels of interconnectors. In addition, it is to be particularly noted that the oxidation of the molybdenum layer or film 55c provides isolation or insulation not only at the

top of this layer but also around edges of the film, thereby additionally increasing the electrical isolation.

Various modifications of the above described embodiments and processes may be utilized in accordance with the invention. For example, it may be desirable to perform very shallow diffusions of impurities at the points of contact between the molybdenum film (films) and the semiconductor surface to provide low resistance ohmic contacts at these points. In addition, instead of depositing the molybdenum film directly upon the semiconductor surface, regions or zones of metallic material may be deposited intermediate the silicon surface and the molybdenum film. These metallic regions may be, for example, platinum-silicide deposits formed in the contact areas prior to the deposition of the molybdenum film, or a flash or very thin layer of aluminum applied prior to the deposition of the molybdenum film. Further, it is to be understood that throughout the above description the use of the metals molybdenum and gold are to include not only pure molybdenum and gold layers, but also molybdenum and gold layers that may have a minor percentage of impurities added thereto. For example, trace impurities may be added to the molybdenum film to increase its adherence and the gold films may have a minor percentage of platinum added thereto to increase the adhesion of the gold to the molybdenum.

While the embodiments and processes of the present invention have been directed toward monolithic integrated circuits and the application of multi-level interconnections to these monolithic integrated circuits, the processes and structures described above may have other applications such as in the areas of discrete semiconductor components and hybrid integrated circuits, for example, whenever it is desired to provide alternating layers or films of metal and electrical insulating material. Various other modifications of the disclosed processes and embodiments will become apparent to persons skilled in the art without departing from the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

A semiconductor device having at least one semiconductor region extending to one face of a substrate having a protective coating of insulating material thereon, and an electrical lead and ohmic contact which is ohmically connected to that semiconductor region through an aperture in the protective coating and which extends on to the protective coating, the lead and contact arrangement comprising overlying films of, respectively, molybdenum, gold and molybdenum.

2. A semiconductor device as claimed in Claim 1, including a further protective coating of insulating material overlying the said lead and contact and which has an opening therein above the underlying lead and contact.

3. A semiconductor device according to Claim 2, including an electrical connection directly to the gold film of the said lead and contact through the opening in the further protective coating and an aperture in the molybdenum film of the lead and contact which is outermost from the substrate.

4. An integrated circuit device comprising a plurality of circuit elements disposed at a common surface of a substrate, each circuit element including at least one semiconductor region, the semiconductor regions being covered by a protective coating of insulating material disposed on the said common face of the substrate, and electrically interconnecting selected ones of the semiconductor regions, an ohmic contact and electrical lead arrangement comprising overlying films of, respectively, molybdenum, gold and molybdenum, the lead and contact arrangement being disposed on the protective coating and making ohmic connection with the said selected regions through apertures in the protective coating.

5. An integrated circuit device as claimed in Claim 4, in which the said ohmic contact and electrical lead arrangement forms a first level interconnection and includes a portion extending over the protective coating to a selected position, a second level interconnector being ohmically connected with the said portion of the first level interconnection at the said selected position and being isolated from other parts of the first level interconnection by an interposed layer of electrical insulation.

6. An integrated circuit device as claimed in Claim 5, in which there is a generic film of molybdenum oxide intermediate the said layer of electrical insulation and the molybdenum film of the first level interconnection outermost from the substrate.

7. An integrated circuit as claimed in Claim 5 or Claim 6, in which the second level interconnector comprises a film of molybdenum disposed on the said insulating medium and overlaid by a film of gold, and in which the molybdenum film of the second level interconnector directly contacts the gold film of the said portion of the first level interconnection at the said selected position.

8. An integrated circuit device according to any one of Claims 4-7, in which the said components are formed as integral parts of a single body of semiconductor material.

9. An integrated circuit device according to Claim 8, in which the said body is

composed of silicon.

10. An integrated circuit device according to any one of Claims 4-9, in which the said insulating medium is composed of silicon oxide.

11. An integrated circuit device according to any one of Claims 4-9, in which the said insulating medium is composed of silicon nitride, aluminium oxide, or tantalum oxide.

12. A device according to any one of the preceding claims, in which the said protective coating is composed of silicon oxide.

13. A device according to any one of the preceding claims, in which the ohmic contact and electrical lead arrangement directly contacts the or each underlying semiconductor region.

14. A device according to any one of Claims 1-12, in which ohmic connections of the ohmic contact and electrical lead arrangement with the or each underlying semiconductor region is effected by an interposed metallic region.

15. A device according to Claim 14, in which the said interposed metallic region is composed of aluminum or platinum silicide.

16. An integrated circuit device according to claim 4, substantially as described herein with reference to Figs. 1-6 only as modified in the manner described and illustrated with reference to Figs. 7a and 7b of the accompanying drawings.

17. A method for providing ohmic contacts and multi-level electrical interconnections in a semiconductor integrated circuit of the type having a plurality of circuit components formed as integral parts of a body, by semiconductor regions extending to a surface of the body beneath a protective coating upon that surface, comprising the steps of:

a) forming a plurality of apertures in the protective coating to expose the surfaces of selected ones of the semiconductor regions;

b) depositing a first film of molybdenum upon the protective coating and within the said apertures to contact the selected regions, depositing a second film of gold upon the first film and depositing a third film of molybdenum upon the second film;

c) selectively etching the first, second and third films to provide ohmic contacts to the selected regions and a plurality of first level interconnectors electrically interconnecting desired groups of the selected regions.

d) depositing a layer of insulating medium overlying each of the said first level interconnectors.

e) selectively etching the layer of insulating medium, and the third said film to expose a portion of the said second



gold film of at least one of the first level interconnectors, and

f) selectively forming a second level interconnector upon the insulating medium to electrically interconnect with the exposed gold portion of the said one first level interconnector.

18. A method as claimed in claim 17, in which following the said step c) the exposed surface portions only of the third film of molybdenum of each of the first level interconnectors is converted to molybdenum oxide, in which in the said step d) the layer of insulating medium is deposited on the molybdenum oxide film on each of the said first level interconnectors, and in which in the said step f) the layer of insulating medium, the molybdenum oxide film and the said third film are selectively etched.

19. A method as claimed in claim 17 or claim 18, in which following the said step a) but before the step b), a film of aluminium or platinum silicide is deposited in the apertures in the said protective coat-

ing formed by the said step a).

20. A method as claimed in any of claims 17-19, in which the said second level interconnector is formed by depositing a film of molybdenum upon the insulating medium which interconnects with the said exposed gold portion of the said one first level interconnector and then depositing a film of gold on the said molybdenum film.

21. A method as claimed in any of claims 17-20, in which the said body is composed of silicon and in which the said protective coating and insulating medium is composed of silicon oxide.

22. A method as claimed in claim 17, substantially as described herein with reference to the accompanying drawings.

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