18/06/02
200236598

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

162162

(43) International Publication Date
5 July 2001 (05.07.2001)

PCT

(10) International Publication Number
WO 01/48598 A1

(51) International Patent Classification[7]: G06F 9/38

(21) International Application Number: PCT/US00/32087

(22) International Filing Date:
20 November 2000 (20.11.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/471,308 23 December 1999 (23.12.1999) US

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 01/48598 A1

(54) Title: MECHANISM FOR HANDLING FAILING LOAD CHECK INSTRUCTIONS

(57) Abstract: A mechanism is provided for recovering from a failing load check instruction in a processor that implements advanced load instructions. An advanced load address table (ALAT) tracks status information for the advanced load instruction. The status information is read when an associated load check operation is processed, and an exception is triggered if the status information indicates data returned by the advanced load operation was modified by a subsequent store operation. The load check instruction is converted to a load operation, instructions are flushed from the processor's instruction execution pipeline, and the pipeline is resteered to the first instruction that follows the load check instruction.

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