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"METHOD OF FORMING AN INTEGRATED CIRCUIT ASSEMBLY OR PART THEREOF"

The present invention relates to a method of forming an integrated circuit assembly or part thereof and, although the invention is not so restricted, it relates more particularly to a method of forming a circuit substrate with leads having projections known as "bumps".

According to the present invention, there is provided a method of forming at least a part of an integrated circuit assembly comprising forming said part with at least one lead whose distal end is provided with a contact surface at least a portion of which has a roughness as herein defined of at least 5 microns, the or each contact surface being adapted to be connected to a connector portion of an electronic element.

The term "roughness" as used herein is to be understood to mean the distance, in a direction at right angles to the contact surface, between the deepest trough and the highest crest in the said contact surface.

The roughness may be between 5 and 20 microns and is preferably between 5 and 15 microns.

Preferably, the or each said distal end is provided with a projection having the said contact surface. Moreover, the or each lead may have a recessed portion immediately adjacent to its projection.

The or each contact surface may be constituted by the surface of a gold plating.

The or each contact surface may be chemically etched to produce the said roughness, or the or each said distal end may be plated to provide a contact surface having a roughness greater than that of the distal end prior to plating. In the latter case, the roughness of the contact surface of the plating may be at least 25% greater than that of the distal end prior to the plating.

The method of the present invention also comprises connecting the or each said contact surface to a connector portion of an electronic element. Thus at least the surface of the or each connector portion may be formed of aluminium or an aluminium alloy.

The or each contact surface is preferably connected to its respective connector portion by the application of heat and pressure so as to produce an alloy connection therebetween.

Preferably the said part is constituted by an insulating film of resin which forms a circuit substrate, there being a purality of separate leads which are formed from a conductive layer of metal foil which is mounted on the circuit substrate.

The metal may be made of copper.

The circuit substrate may be provided with an opening for housing an electronic element, the said conductive layer extending over said opening.

The method may comprise providing front and back surfaces of the conductive layer with photo-resist layers; patterning both the photo-resist layers by simultaneous exposure and development so as to form lead patterns; subjecting portions of the said front and back surfaces to partial etching; applying a protective resist layer to the said back surface; completing the etching of the conductive layer by further etching of the said front surface so as to provide the conductive layer with the said plurality of separate leads;and removing the photo-resist and protective resist layers.

The partial etching may be effected with ferric chloride solution.

The back surface of each lead may be etched to produce a curved surface adjacent its projection and/or may be etched to provide a lead which tapers towards its projection.

The invention also comprises an integrated circuit assembly or part thereof when made by the method set forth above.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a broken away cross-sectional view of a part of an integrated circuit assembly known to the Applicants and not forming part of the present invention:

Figure 2 is a broken away cross sectional view of a part of an integrated circuit assembly made by the method of the present invention;

Figure 3 shows a greatly magnified view of a portion of a contact surface of the part shown in Figure 2;

Figure 4 is a broken away cross sectional view of an integrated circuit assembly made by the method of the present invention and incorporating the part shown in Figure 2;

Figure 5 illustrates the steps in a method of forming a part of an integrated circuit assembly, the said method being known to the Applicants and not forming part of the present invention;

Figure 6 illustrates the steps in a method according to the present invention of forming a part of an integrated circuit assembly;

Figures 7-9 are plan views of photo-masks which may be used in the method illustrated in Figure 6;

Figures 10-12 are broken away sectional views illustrating alternative forms of leads forming portions of the said part of an integrated circuit assembly which may be made by the method illustrated in Figure 6;

Figure 13 is a broken away sectional view of an integrated circuit assembly incorporating the said part which may be made by the method illustrated in Figure 6;

Figure 14 is a view similar to that of Figure 13 but illustrating a modification, and

Figure 15 is a broken away cross sectional view of another part of an integrated circuit assembly made by the method of the present invention.

Reference is made to Figure 1 which is a cross sectional view of a part of an integrated circuit assembly known to the Applicants and not forming part of the present invention.

In Figure 1 there is shown a circuit substrate base film 1 on which is mounted a film 3 which is provided with a conductive pattern (not shown), the film 3 being secured to the circuit substrate base film 1 by a layer 2 of adhesive. The circuit substrate base film 1 has an aperture 1a therein, the film 3 having a plurality of finger leads 4 each of which extends over part of the aperture 1a. An electronic element such as an integrated circuit chip (not shown) may be mounted in the aperture 1a.

Each finger lead 4 is provided with a concave neck-like portion 5 so that a projection, or "bump" 6 is formed at the distal end of the lead. Generally, the surface 8 of the "bump" 6 which is to be connected to an aluminium pad of the integrated circuit chip is substantially plane such that the roughness, as defined above, is less than 3 microns.

The construction shown in Figure 1, however, has some disadvantages. For example, when the integrated circuit (hereinafter "IC") chip is attached at its aluminium pads to the "bumps" 6, the connection between the IC chip and the circuit substrate base film 1 is often unstable, weak or even cannot be made at all, especially when the oxide film on the surface of the aluminium pad is relatively thick.

Figure 2 is a cross section similar to that of Figure 1 but showing an embodiment of the present invention. Parts of Figure 2 which correspond to those of Figure 1 are given the same reference numerals. Thus in the construction of Figure 2, there is provided a circuit substrate base film 1 of polyimide or the like, an adhesive layer 2, a film 3 (e.g. of copper) having a conductive pattern, and finger leads 4 each of which has a neck-like or recessed portion 5 and a projection or "bump" portion 6. Each "bump" portion 6 is provided at the distal end of its respective finger lead 4, the recessed portion 5 being provided immediately adjacent to the "bump" portion 6. Each "bump" portion 6 has a contact surface 7. The "bump" portion 6 may be formed of copper material on which there is a nickel plating, there being a gold plating on the nickel plating so that the gold plating constitutes the contact surface 7. The contact surface 7, in one particular embodiment, has a roughness of about 9 microns. This is in contrast to the contact surface 8 of the "bump" 6 of the Figure 1 construction which has a roughness of about 3 microns or less.

In the embodiment of Figure 2, each finger lead 4 may be about 35 microns in thickness and about 60 microns in width. The depth of the neck-like portion 5 may be about 15 microns and the "bump" 6 may be about 35 micron in thickness, about 60 microns in width and about 60 microns in length. The nickel

plating on the "bump" 6 may be as thick as about 1 micron, while the gold plating may also be as thick as about 1 micron.

A construction such as shown in Figure 2 enables a stable connection to be made between a "bump" 6 and an aluminium pad of an IC chip by ensuring that the roughness of the contact surface 7 is at least 5 microns, and preferably between 5 and 20 microns, the best range being between 5 and 15 microns.

In the case of the construction of Figure 2, when the IC chip is mounted in position in the aperture 1a in the circuit substate base film 1, the convex portions of the uneven surface of the "bump" 6 eat into the surface of the aluminium pads of the IC chip and alter in shape, thereby destroying the oxide films on the surface of the aluminium pads effectively. Then the metal forming the "bumps" and the pure metal inside the aluminium pads beneath the oxide films are easily made into an alloy to provide the required strong connection.

When the roughness of the contact surface 7 is 5 microns or more, the effect produced by destroying the oxide film of the aluminium pad is considerable and the connection strength and proportion of satisfactory connections are excellent.

If the roughness is over 15 microns and especially if the roughness is over 20 microns, however, the thickness of the "bump" 6 in the regions of the concave portions of the uneven surface is considerably reduced and the strength of

the finger lead 4 itself is extremely low in comparison with the connection strength between the substrate and the IC chip.

The shape of the contact surface 7 is illustrated in Figure 3 in which the distance, in a direction at right angles to the contact surface 7, between the deepest trough 7a and the highest crest 7b is shown in the case as being about 6.5 microns.

In Figure 4 the structure of Figure 2 is shown assembled to an IC chip 9 disposed in the aperture 1a. As shown in Figure 4, the "bumps" 6 are in registration with aluminium pads or other connector portions 10 of the IC chip 9.

With respect to the method of forming such a contact surface 7 having a roughness of about 9 microns, there are two cases. Firstly, when the contact surface 7 is to be provided on the same side of the finger lead 4 as the circuit substrate base film 1, as in the embodiment of Figure 2, an uneven adhesion surface 12 of the finger lead 4 in contact with the adhesive layer 2 on the film 3 having the conductive pattern 3 is used as it is without performing a chemical or other polishing step and the surface of the "bump" 6 is sequentially plated with nickel and with gold. The adhesion surface 12 is primarily made uneven, with particles separated out from an electrolytic copper plating, for the purpose of improving

the adhesion strength with the adhesive layer 2 in the process of forming the copper foil 3. Secondly, when the contact surface 7 is to be provided on the side opposite to the circuit substrate base film 1, the free surface 13 of the finger lead 4 has a roughness of 3 microns or less during the process of forming the copper foil, and accordingly, chemical etching is performed on the surface 13 to make it uneven. Thereafter the surface 13 is plated first with nickel and then with gold.

Thus when the aluminium pads 10 of the IC chip 9 and the "bumps" 6 of the finger leads 4 are simultaneously connected, strong and stable connections are provided as shown in Figure 4.

Such strong and stable connections are obtained by the following method.

First, the aluminium pads 10 of the IC chip 9 are positioned in registration with the "bumps" 6 of the finger leads 4. Then, using a heater tool, the "bump" 6 of each finger lead 4 is pressed against the IC chip 9 so that the contact surface 7 of the "bump" 6 is in contact with the respective aluminium pad 10 and pressure and heat are applied thereto. The pressure may be about 100g per bump and the heating may be effected by a heater tool at a temperature of about 500^{o}C for 1 to 2 seconds. At this time, the projecting portions of the uneven contact surface 7 initially

eat into the aluminium pad 10 of the IC chip 9 like wedges. Then, as a result of the pressure applied by the heater tool, the projecting portions of the contact surface 7 are crushed and deform to expand in a direction at right angles to the direction in which the pressure is applied. Consequently, the aluminium oxide film on the surface of the aluminium pad 10 is very effectively destroyed and removed to expose the pure aluminium inside the aluminium pad 9. As a result of the pressing and the heating mentioned above, the metal forming the "bump" and the aluminium easily react together and an efficient alloy is formed, thereby providing a strong connection.

As a result, the mean connection strength between the "bump" 6 and the aluminium pad 10 is 22.1g with a standard deviation of 4.1g which is an improvement by about 50% in comparison with a mean strength of 14.6g with a standard deviation 5.4g in the case of the construction of Figure 1.

Further, the connection yield, i.e. the proportion of satisfactory connections, is also improved to 99% or more in the case of the Figure 2 construction, as compared with about 80% in the case of the construction of Figure 1.

Herein, the "connection strength" means the strength to destruction which is measured with measurement equipment by a method in which the terminal of the equipment is hitched around the neck-like portion 5 of the finger lead 4 on the IC chip in Figure 4 and the equipment is pulled in a direction so as to part the finger leads from the I.C. chip 9, i.e. upwardly when

the parts are disposed as shown in Figure 4. When the equipment is pulled to a certain degree, the joint between the finger lead 4 and the IC chip 9 is destroyed in some cases and the finger lead 4 itself or the IC chip 9 itself is destroyed in other cases.

TABLE 1 gives detailed data of the connection strength and the connection yield with variations of the roughness of the contact surface 7.

TABLE 1

Roughness	connection strength	connection yield
3 microns	14.6g	80%
5 microns	19.8g	95%
7 microns	21.3g	97%
9 microns	22.1g	99%
12 microns	22.3g	99%
15 microns	22.0g	99%
19 microns	17.1g	98%

As is apprent from the above TABLE 1, when the roughness of the contact surface 7 is between 5 and 15 microns, the connection strength and the connection yield are very high. When the roughness is 3 microns, that is, below 5 microns, the oxide film of the pad 10 of the IC chip 9 is not adequately broken and so the connection strength and the connection yield are inadequate for practical use. When, on the contrary, the

roughness is 19 microns, that is, over 15 microns, the connection yield is rather good but there is another problem. Namely, since the roughness of the contact surface 7 is very considerable, the thickness of the finger lead 4 at the portion of the contact surface 7 where the deepest trough is located is considerably reduced and thus the strength of the finger lead 4 itself is even less than the strength of the joint portion. Nevertheless, it will be noted from Table 1 that even with a roughness of 19 microns, the connection strength is still substantially superior to what is obtained when the roughness is 3 microns.

It will therefore be appreciated from the above that the most desirable roughness of the contact surface 7 is between 5 and 15 microns.

In Japanese Patent Application No. 59-17981 there is disclosed a method of forming a projection for making an electrical connection between, for example, an inner lead of a substrate and an electronic element. This method, as illustrated in the accompanying Figure 5, involves the steps of:-

a) coating a front surface 22a of a conductive layer 22 with a protective resist 27, the conductive layer 22 being provided on a circuit substrate 21 having an aperture 24 for housing an IC chip (not shown) and sprocket holes 25,

b) coating a back surface 22b of the conductive layer 22

with a photo-resist 23 and forming "bumps" or projections 26 by exposure, development and half etching.

c) removing the protective resist 27 and the photo-resist 23 on the front and the back surfaces 22a, 22b of the conductive layer 22,

d) coating the front surface 22a of the conductive layer 22 with a photo-resist 31 and patterning the latter by exposure and development,

e) coating the back surface 22b of the conductive layer 22 with a protective resist 32,

f) etching the front surface 22a of the conductive layer 22 to form a circuit pattern having inner leads 28, and

g) removing the photo-resist 31 and the protective resist 32 on the front and the back surfaces 22a, 22b of the conductive layer 22, to form the "bumps" 26 on the back surface 22b of the inner leads 28.

The method illustrated in Figure 5, however, has some defects. Since the front and the back surfaces 22a, 22b of the conductive layer 22 are exposed separately, the positioning of the conductive layer 22 for exposure is likely to be inaccurate, and therefore it is difficult to form the "bumps" 26 accurately at the predetermined positions on the inner leads 28. The patterns on the front and the back surfaces 22a, 22b of the conductive layer 22 can thus be

positioned in registration with each other only initially but it is impossible to maintain registration of the patterns on both surfaces of the subsequent individual substrates. Accordingly, if the accuracy of the positioning of the conductive layer 22 with respect to the exposure apparatus is poor, or if the sprocket holes 25 which are pilot holes, have become deformed, many defects occur such as the fact that the "bumps" fail to be formed and that errors occur in the positioning of the "bumps" and of the electrodes of the semiconductor element and consequently the connection therebetween is unsatisfactory.

Moreover, in the method of Figure 5, the half-etched conductive layer 22 is reduced in strength and since such a weakened layer is coated with the photo-resist, exposed, developed and subjected to other processes, it is likely to become deformed. Consequently cracks of the photo-resist cause the disconnection of the wiring, thereby making it impossible to form the desired patterns with certainty.

Reference is now made to Figure 6 which illustrates successive steps in the production of an embodiment of the present invention in which "bumps" for electrical connection are formed on the inner leads of a substrate.

Figure 6(a) illustrates the step of coating photo-resist 43 onto opposite surfaces 42a, 42b of a conductive layer 42 attached to an insulating layer 41. The insulating layer 41

may be a flexible tape of a material such as polyimide or glass-reinforced epoxy resin having for instance a thickness of between 25 and 125 microns. The insulating layer 41 is provided with an aperture 44 for holding a electronic element such as a semiconductor chip. The insulating layer 41 is also provided with sprocket holes 45 for positioning or carrying the insulating layer 41 and with other holes (not shown) for the passage therethrough of wires (not shown) which are necessary for the circuits employed.

The conductive layer 42 is generally a copper foil having a thickness of between 35 and 70 microns. The back surface 42b is treated to have a roughness as herein defined of about 10 microns in order to improve its adhesiveness with respect to the insulating layer 41. This roughness is retained on the surface of the bumps 46 which are formed in a later step. This roughness is of importance, as discussed above, when connecting an aluminium pad of the semiconductor chip to a bump 46. Accordingly, it is important to maintain the initial surface roughness. Consequently, the thickness of the photo-resist 43 on the back surface 42b of the conductive layer 42 must be sufficient for the convex projecting portions of the surface not to be etched during the subsequent half-etching process and must not be too thick to become non-uniform. Thus the most suitable thickness of the photo-resist 43 on the back surface 42b of the conductive

layer 42 is between 1.5 and 4 microns. The thickness of other photo-resist layer 43 on the front surface 42a of the conductive layer 42 is generally between 1 and 3 microns.

The photo-resists 43 on the surfaces 42a, 42b may be coated by a roller coater, spraying and so on.

In the step shown in Figure 6(b), both surfaces 42a, 42b of the conductive layer 42 are simultaneously exposed to form a circuit pattern including inner leads on the front surface 42a. This may be done by using the photo-mask shown in Figure 7 and to form the "bump" pattern on the back surface 42b by using the photo-mask shown in Figure 8. This simultaneous exposure is performed by using a two-sided exposure apparatus which has been adjusted to form the patterns at the predetermined positions on both surfaces 42a, 42b. Then the two surfaces 42a, 42b are simultaneously developed by spraying or dipping in a specific development solution.

The photo-mask of Figure 7 is designed to be thoroughly conductive so that the circuit pattern including the inner leads are electrically plated in a later step.

With regard to the photo-mask for forming the "bump" pattern, in addition to the one shown in Figure 8 in which separate projection patterns are provided correspondingly to the inner leads, another mask as shown in Figure 9 can also be used in which a part of or all of the "bumps" are connected.

In order to make the condition of both surfaces 42a, 42b of the conductive layer 42 an optimum for development simultaneously, the degree of exposure is adjusted so that, when the thickness of the photo-resists 43 on both surfaces 42a, 42b are equal, the amount of light for the back surface 42b which has a high degree of roughness and which is difficult to develop is 1.5 to 2.5 times as large as that for the front surface 42a.

In the step shown in Figure 6(c), both surfaces 42a, 42b of the conductive layer 42 are partially etched by spraying an etching solution such as ferric chloride. The height of the "bumps" 46 on the back surface 42b of the conductive layer 42 depends on the thickness of the used conductive layer. Generally, when the conductive layer 42 is a copper foil having a thickness of 35 microns, the height is desirably between 5 and 20 microns in order to prevent an edge short circuit of the semiconductor chip and to assure the strength of the inner leads.

Furthermore, in order to prevent the disconnection of the conductive layer 42 at the corners of the partially etched portion on which the stress is concentrated, the spray pressure may be reduced and a side etch effected, mainly to form a large round curve at the corners of the partially etched portion as shown in Figure 10.

Usually, the partial-etching is carried out by

spraying a solution of ferric chloride at a solution temperature of between 25 and 40°C, the solution having a specific gravity of between 30 to 60Bé (Baumé) at a spraying pressure of 0.5kgf/cm^2 or less. However, if the height of the "bumps" 46 is smaller than half of the thickness of the conductive layer 42, partial etching by a dipping method is also applicable.

In order to obtain adequate strength of the inner leads, it may sometimes be desirable for the photo-mask used when the "bump" pattern is formed on the back surface 42b of the conductive layer 42 by exposure and development to be modified so as progressively to vary the amount of partial etching, as shown in Figure 11 or to make the partially etched portion as short as possible as shown in Figure 12.

With respect to the partial etching of the front surface 42a of the conductive layer 42, in order to avoid non-uniform etching caused by undesirable flow of the etching solution used for the partial etching of the back surface 42b, the etching solution may be sprayed in the same manner as for the back surface. At this time, it is necessary to adjust the spray pressure and so on so that the portion of the conductive layer 42 which is etched from both surfaces 42a, 42b is not etched sufficiently to form a hole.

In Figure 6(d), the back surface 42b of the conductive layer 42 is coated by means of a roller coater or spraying, with a protective resist 47 such as an etching resist or a photo-resist which can be removed by the same removing solution

used for removing the photo-resist formed in the step of Figure 6(a).

In Figure 6(e), the etching solution is sprayed on the front surface 42a of the conductive layer 42 to etch away the unnecessary conductive layer which has remained without being etched in the step of Figure 6(c). Thus a circuit pattern having inner leads 48 is formed.

In Figure 6(f), the photo-resist 43 and the protective resist 47 are removed with a specific removing solution. Finally, there is formed a circuit substrate 41 having inner leads 48 with the "bumps" 46 for electrical connection.

Generally, although not shown in the drawings, the projections or "bumps" 46 are plated with nickel having a thickness of between 0 to 3 microns and then with gold having a thickness of 0.5 to 4 microns, and the "bumps" 46 are positioned in registration with the aluminium pads of the semi-conductor chip and are thermally bonded thereto to make electrical connections therebetween.

Figure 13 shows a structure in which a semiconductor chip 51 is connected to "bumps" 53 on the front surfaces of leads 54, the leads 54 being mounted on a substrate 50 and being formed by the method illustrated in Figure 6. 52 is a resin sealing agent.

Figure 14 illustrates a construction generally similar to that of Figure 13, like reference numerals indicating like parts. In the Figure 14 construction, however, the leads 54 have "bumps" 53a on the rear surfaces, as opposed to the front surfaces, of the leads 54.

The invention is of course applicable to all kinds of print substrates having leads for connection to an electrical element.

By using the method illustrated in Figure 6, the inner leads and the "bump" pattern are formed simultaneously on the front and the back surfaces 42a, 42b of the conductive layer 42 by the common exposure apparatus. Accordingly, if the patterns on both surfaces are initially registered with each other, no relative positioning error between the patterns on the two surfaces occurs thereafter and consequently the formation of the patterns is not affected by the accuracy of the positioning of the substrate with respect to the exposure apparatus and the accuracy of the positioning of the holes in the substrate itself. Thus, the "bumps" are always formed accurately at the predetermined position on the inner leads. Moreover, it is easy to position the "bumps" in registration with the electrodes of the electronic element and stable connections therebetween are obtained.

Furthermore, the number of steps in the method illustrated in Figure 6 are greatly reduced in comparison with those employed in the prior art. In particular, after the partial etching of the conductive layer 42, there is only the single step of coating the back surface 42b of the conductive layer 42 with the protective resist 47 before the final etching, and therefore the conductive layer 42 is not likely to be deformed. For this reason, no cracking occurs in the photo-resist and good stable patterns are easily formed.

It is another advantage that the simplification referred to above leads to a large reduction in manufacturing costs.

Referring once again to Figure 2, the "bumps" 6 may be formed by half-etching the middle portions of the finger leads 4 and the plating of the surface of the "bumps" 6 may be such as to increase the roughness of the base material.

As indicated above when the aluminium pads 10 of the IC chip 9 and the "bumps" 6 are connected together, the rough contact surface 7 of each "bump" 6 eats into the surface of the respective aluminium pad 10 and is deformed while the oxide film on the surface of the aluminium pad 10 is destroyed, and then the metal forming the "bump" 6 and the clean metal surface of the aluminium pad 10 beneath the oxide film are made into an alloy, thereby providing a strong connection.

Thus, the roughness of the contact surface 7 of the "bump" 6 has a great effect onto the strength of the connection. As mentioned later, the maximum surface roughness (hereinafter referred to as "Rmax") is preferred to be between 5 and 20 microns which allows the surface of the "bump" to be provided with fine grooves.

In one particular embodiment, the conductive material forming the conductive pattern 3 on the base substrate 1 is constituted by an electrolytic copper foil. The back surface of the copper foil which later becomes the contact surface

of the "bump" 6 in contact with the aluminium pad 10 can be made to have a roughness Rmax of between 5 and 12 microns during the deposition of the electrolytic copper plating when manufacturing the copper foil. As indicated above, this improves the adhesion strength between the back surface of the copper foil and the substrate 1 through the intermediary of the adhesive 2, the substrate 1 being formed, for example, of polyimide or glass-reinforced epoxy resin. This roughness Rmax of between 5 and 12 microns is, however, reduced to a roughness of between 3 and 8 microns through subsequent processes, such as surface treatment, etching and so on, which are employed in manufacturing the circuit substrate 1 with the "bumps" 6.

However, the phenomenon that the electric current used in plating the "bump" 6 is concentrated at the projecting portions of the contact surface 7 can be utilised so that, when the "bump" 6 is plated with nickel and then with gold, the fine projecting portions on the contact surface 7 can be enlarged.

Figure 15 is an enlarged cross sectional view of the "bump" portion 65 of a finger lead 64 which corresponds to the finger lead 4 of Figure 2. The finger lead 64 and the "bump" 65 are formed from a copper foil 66. The surface of the copper foil 66 is plated with a nickel layer 68 and with a gold layer 69. These plating layers 68, 69 are relatively thick at the projecting portions or crests 67 of the contact surface of the "bump" 65 at which the electrical current is concentrated and are relatively thin around the troughs 70,

thus increasing the roughness of the contact surface. Such a phenomenon is more pronounced when the electrical current density employed during the plating is high. Accordingly, it is desirable to make the electrical current density as high as possible but is not so high as to produce plating stains.

In the embodiment illustrated in Figure 15 , the nickel layer 68 can have a thickness of between 0.5 and 1 micron, and gold can be plated thereon at an electrical current density of 2.5A/dm for 1 minute. The mean total thickness of the nickel and gold platings collectively may be 1.5 microns and the increase in the roughness Rmax of various portions of the contact surface of the "bump" is between 2 and 6 microns.

The plating conditions are not limited to those mentioned above and the conditions depend on the plating apparatus or the plating solution used. When a plating layer of the same thickness as that mentioned above is to be obtained, if the plating is effected with an electric current whose current density is almost at the upper limit of the practically tolerated current density for a short time, a large degree of surface roughness can be provided.

Table 2 shows data concerning the total surface roughness (Rmax) of the "bump" at its roughest portion, the connection strength and the connection yield when the gold is plated to

a thickness of 1.5 microns under various conditions (electrical current density) upon the copper foils having four different roughnesses (Rmax).

TABLE 2

Electrical Current Density (A/dm^2)	Copper Foil Surface Roughness (microns)	Total Surface Roughness (microns)	Connection Strength (grams)	Connection Yield (%)
0.5	3	3	12.5	80
1.5	3	5	19.8	95
2.5	3	6	21.5	96
0.5	7	7	21.2	96
1.5	7	9	23.6	99
2.5	7	10	24.3	99
0.5	11	12	21.4	98
1.5	11	14	22.4	98
2.5	11	15	23.0	99
0.5	15	16	19.2	95
1.5	15	18	19.5	96
2.5	15	20	18.5	96

In Table 2, the data relates to a "bump" which is 60 microns square, and a nickel plating having a thickness of 1 micron. The "connection strength" means the strength at the time when either the connection between the finger lead and the pad of the IC chip or the finger lead itself is destroyed by pulling the middle portion of the finger lead vertically upwards.

As seen from TABLE 2, provided that the electrical current density is lower than $2.5A/dm^2$, the higher the density, the greater will be the surface roughness and the connection strength. In particular, when the total surface roughness Rmax is 5 microns or larger, the connection is a stable one. When the surface roughness of the base material is small, it is particularly effective to increase the roughness (e.g. by at least 25%) by plating. On the other hand, when the surface roughness Rmax of the copper foil is 15 microns, the copper foil surface is so rough that the strength of the finger lead itself is decreased thereby. Taking the optimum thickness of the gold plating into account, the upper limit of the total surface roughness Rmax should preferably not exceed 20 microns. Accordingly, the total surface roughness is desirably between 5 and 20 microns.

The above embodiment concerns the case where the "bump" is formed on the back surface of the electrolytic copper foil 66 which has a large surface roughness. In the case

where a "bump" is to be formed on the front surface of a copper foil whose roughness is less than 3 microns or where a rolled copper foil is used, the surface can be made rough by a mechanical method such as using brush-polishing or sand blasting or by a chemical method such as using an aqueous solution of ammonium persulfate or sodium persulfate and by increasing the roughness by plating thereafter. By performing such a treatment, a stable connection between the "bump" and the aluminium pad can be provided which is as good as what can be provided when the bump is formed on the back surface of the electrolytic copper foil.

Thus it is within the scope of the present invention that, in contrast to what is shown in Figure 4, the "bump" 6 of each finger lead 4 is provided on the side of the latter opposite to the substrate 1, the pad 10 of the IC chip 9 being mounted on the "bump" 6 and bonded thereto. An arrangement of this kind is illustrated in Figure 14.

Although the above description refers to the pads 10 as being made of aluminium, they may also be made of an aluminium alloy or of some other metal.

In our co-pending British patent application No. 8901925 (P/8141201), which contains subject matter divided out of the present application, we have claimed a method of forming an integrated circuit assembly or part thereof comprising providing a conductive layer on and extending from an insulating substrate; providing front and back surfaces of the conductive layer with photo-resist layers; patterning both the photo-resist layers by simultaneous exposure and development; subjecting portions of the said front and back surfaces to partial etching; applying a protective resist layer to the said back surface; completing the etching of the conductive layer by effecting further etching of the said front surface; and removing the photo-resist and protective resist layers.



C L A I M S

1, A method of forming at least a part of an integrated circuit assembly comprising forming said part with at least one lead whose distal end is provided with a contact surface at least a portion of which has a roughness as herein defined of at least 5 microns, the or each contact surface being adapted to be connected to a connector portion of an electronic element.

2. A method as claimed in claim 1 in which the roughness is between 5 and 20 microns.

3. A method as claimed in claim 2 in which the roughness is between 5 and 15 microns.

4. A method as claimed in any preceding claim in which the or each said distal end is provided with a projection having the said contact surface.

5. A method as claimed in claim 4 in which the or each lead has a recessed portion immediately adjacent to its projection.

6. A method as claimed in any preceding claim in which the or each contact surface is constituted by the surface of a gold plating.

* C L M S *

7. A method as claimed in claim 6 in which the gold plating is provided on a nickel plating which is itself provided on the distal end of the respective lead.

8. A method as claimed in any preceding claim in which the or each contact surface is chemically etched to produce the said roughness.

9. A method as claimed in any of claims 1-7 in which the or each said distal end is plated to provide a contact surface having a roughness greater than that of the distal end prior to plating.

10. A method as claimed in claim 9 in which the roughness of the contact surface of the plating is at least 25% greater than that of the distal end prior to the plating.

11. A method as claimed in any preceding claim in which the method comprises connecting the or each said contact surface to a connector portion of an electronic element.

12. A method as claimed in claim 11 in which at least the surface of the or each connector portion is formed of aluminium or an aluminium alloy.

13. A method as claimed in claim 11 or 12 in which the or each contact surface is connected to its respective connector portion by the application of heat and pressure so as to produce an alloy connection therebetween.



14. A method as claimed in any preceding claim in which the said part is constituted by an insulating film of resin which forms a circuit substrate, there being a plurality of separate leads whcih are formed from a conductive layer of metal foil which is mounted on the circuit substrate.

15. A method as claimed in claim 14 in which the metal foil is made of copper.

16. A method as claimed in claim 14 or 15 in which the circuit substrate is provided with an opening for housing an electronic element, the said conductive layer extending over said opening.

17. A method as claimed in any of claims 14-16 comprising providing front and back surfaces of the conductive layer with photo-resist layers; patterning both the photo-resist layers by simultaneous exposure and development so as to form lead patterns; subjecting portions of the said front and back surfaces to partial etching; applying a protective resist layer to the said back surface; completing the etching of the conductive layer by further etching of the said front surface so as to provide the conductive layer with the said plurality of separate leads; and removing the photo-resist and protective resist layers.

18. A method as claimed in claim 17 in which the partial etching is effected with ferric chloride solution.

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19. A method as claimed in claim 17 or 18 when dependent upon claim 4 in which the back surface of each lead is etched to produce a curved surface adjacent its projection.

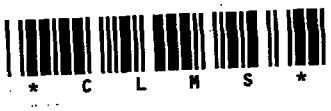
20. A method as cliamed in any of claims 17-19 when dependent upon claim 4 in which the back surface of each lead is etched to provide a lead which tapers towards its projection.

21. A method of forming an integrated circuit assembly or part thereof as claimed in claim 1 and substantially as hereinbefore described with reference to Figures 2-4 and 6-14 of the accompanying drawings.

22. An integrated circuit assembly or part thereof when made by the method claimed in any preceding claim.

23. A method of forming an integrated circuit assembly or part thereof comprising forming a circuit substrate with at least one lead whcih extends from the circuit substrate, and plating the distal end of the or each lead so as to provide on said plating a contact surface whose roughness as herein defined is greater than that of the distal end prior to plating, the contact surface being adapted to be connected to a connector portion of an electronic element.

24. A circuit substrate which includes leads on which integrated circuit devices are mounted, and which includes bumps at the end portions of the leads in registration with pads of integrated circuit chips mounted on said substrate, the surface of said bumps having a roughness of between 5 and 15 microns.



25. A circuit substrate which includes leads on which integrated circuit devices are mounted, and which includes bumps at the end portions of the leads in registration with pads of integrated circuit chips mounted on said substrate, the roughness of the surface of said bumps having been increased by plating.