

WHAT IS CLAIMED IS:

1. An integrated circuit device comprising:

a substrate having a cell array area and a peripheral circuit area, the cell array area comprising a first active region, and the peripheral circuit area comprising a second active region;

a direct contact connected to the first active region in the cell array area;

a bit line structure connected to the direct contact in the cell array area; and

a peripheral circuit gate structure on the second active region in the peripheral circuit area,

wherein the peripheral circuit gate structure comprises two doped semiconductor layers each being doped with a charge carrier impurity having different doping concentrations from each other, and

wherein the direct contact comprises a contact semiconductor layer having a doping concentration that is lower than a doping concentration of each of the two doped semiconductor layers comprised in the peripheral circuit gate structure.

2. The integrated circuit device according to claim 1,

wherein the two doped semiconductor layers comprised in the peripheral circuit gate structure comprise a first gate semiconductor layer having a first doping concentration,

wherein the direct contact comprises a contact semiconductor layer having a second doping concentration that is lower than the first doping concentration, and

wherein the bit line structure comprises a bit line semiconductor layer having a third doping concentration that is higher than the second doping concentration.

3. The integrated circuit device according to claim 2, wherein the two doped semiconductor layers comprised in the peripheral circuit gate structure further comprise a second gate semiconductor layer having a doping concentration that is equal to the third doping concentration.

4. The integrated circuit device according to any one of claims 1 to 3, further comprising:

a direct contact spacer covering sidewalls of the direct contact,
wherein each of the direct contact and the direct contact spacer comprises a semiconductor layer.

5. The integrated circuit device according to claim 4,
wherein the direct contact spacer comprises undoped polysilicon having no charge carrier impurity doped thereon, and
wherein the contact semiconductor layer comprises doped polysilicon.

6. The integrated circuit device according to claim 4 or claim 5,
wherein the bit line structure extends along the substrate in a first direction, and
wherein the direct contact spacer covers both sidewalls of the direct contact on opposite sides to each other in the first direction and does not cover both sidewalls of the direct contact on opposite sides to each other in a second direction that is orthogonal to the first direction.

7. The integrated circuit device according to any one of claims 4 to 6, wherein each of the direct contact and the direct contact spacer comprises a portion buried in the substrate.

8. The integrated circuit device according to any one of claims 1 to 3, further comprising:

a buffer insulating film between the substrate and the bit line structure in the cell array area, the buffer insulating film having a hole penetrated by the direct contact; and

a direct contact spacer in the hole, the direct contact spacer being between the direct contact and the buffer insulating film,

wherein the direct contact spacer comprises undoped polysilicon having no charge carrier impurity doped thereon, and

the direct contact comprises doped polysilicon having a charge carrier impurity doped thereon.

9. The integrated circuit device according to claim 8, further comprising:

a semiconductor oxide film between the buffer insulating film and the bit line structure in the cell array area,

wherein the semiconductor oxide film comprises a dopant comprising B, In, P, As, Sb, or combinations thereof.

10. An integrated circuit device comprising:

a substrate having a cell array area and a peripheral circuit area, the cell array area comprising a plurality of first active regions spaced apart from each other, and the peripheral circuit area comprising a second active region;

a plurality of direct contacts each connected to a corresponding one of the plurality of first active regions in the cell array area;

a plurality of bit line structures extending parallel to each other in a first direction in the cell array area, each of the plurality of bit line structures is connected to a corresponding one of the plurality of direct contacts; and

a peripheral circuit gate structure on the second active region in the peripheral circuit area,

wherein the peripheral circuit gate structure comprises two doped semiconductor layers each doped with a charge carrier impurity and having different doping concentrations from each other, and

wherein each of the plurality of direct contacts comprises a contact semiconductor layer,

wherein the peripheral circuit gate structure comprises a first gate semiconductor layer having a first doping concentration, and a second gate semiconductor layer having a second doping concentration and spaced apart from the substrate with the first gate semiconductor layer therebetween, and

wherein the contact semiconductor layer has a doping concentration that is lower than the first doping concentration and lower than the second doping concentration.

11. The integrated circuit device according to claim 10, further comprising:

a plurality of buried contacts between the plurality of bit line structures;

a plurality of direct contact spacers each contacting corresponding first sidewall portion of sidewalls of each of the plurality of direct contacts, each of the first sidewall portion being in a region between corresponding one of the plurality of bit line structures and the substrate; and

a plurality of insulating spacers each arranged between corresponding one of the plurality of buried contacts and the plurality of direct contacts and each contacting corresponding second sidewall portion of the sidewalls of each of the plurality of direct contacts, each of the second sidewall portion facing the plurality of buried contacts.

12. The integrated circuit device according to claim 10 or claim 11, further comprising:

a buffer insulating film and a semiconductor oxide film, which are between the substrate and the plurality of bit line structures in the cell array area and stacked on the substrate in this stated order;

a plurality of direct contact spacers penetrating the buffer insulating film and the semiconductor oxide film and contacting first sidewall portions of the plurality of direct contacts in the substrate; and

a plurality of insulating spacers penetrating the buffer insulating film and the semiconductor oxide film and contacting second sidewall portions of the plurality of direct contacts in the substrate.

13. The integrated circuit device according to any one of claims 10 to 12, further comprising:

a device isolation film in an interface area between the cell array area and the peripheral circuit area in the substrate;

a buffer insulating film extending, on the substrate, from the cell array area to the interface area, the buffer insulating film covering a top surface of the device isolation film to define an undercut region over the top surface of the device isolation film in the interface area; and

a filling insulating pattern filling the undercut region,

wherein each of the buffer insulating film and the filling insulating pattern comprises an oxide film.

14. An integrated circuit device comprising:

a substrate having a cell array area and a peripheral circuit area, the cell array area comprising a first active region, and the peripheral circuit area comprising a second active region;

a direct contact connected to the first active region in the cell array area and comprising a doped contact semiconductor layer doped with a charge carrier impurity that has a first doping concentration;

a bit line structure over the substrate in the cell array area, the bit line structure comprising a bit line semiconductor layer that contacts a top surface of the direct contact and has a doping concentration higher than the first doping concentration;

a direct contact spacer contacting a first sidewall portion of a sidewall of the direct contact and comprising an undoped semiconductor having no charge carrier impurity doped thereon, the first sidewall portion being between the substrate and the bit line structure;

an insulating spacer contacting a second sidewall portion of the sidewall of the direct contact and covering a sidewall of the bit line structure; and

a peripheral circuit gate structure on the second active region in the peripheral circuit area, wherein the peripheral circuit gate structure comprises a first gate semiconductor layer and a second gate semiconductor layer, the first gate semiconductor layer having a doping concentration that is equal to or higher than the first doping concentration, and the second gate semiconductor layer having a doping concentration that is higher than the first doping concentration.

15. The integrated circuit device according to claim 14,
wherein the doping concentration of the first gate semiconductor layer is higher than the first doping concentration, and
wherein the bit line semiconductor layer and the second gate semiconductor layer have an equal doping concentration.

16. The integrated circuit device according to claim 14,
wherein the doping concentration of the first gate semiconductor layer is equal to the first doping concentration, and
wherein the bit line semiconductor layer and the second gate semiconductor layer have an equal doping concentration.