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(54) ELECTRONIC ALARM TIMEPIECE

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese Company of 6-31-1 Kameido Koto-ku Tokyo Japan do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:

This invention relates to electronic alarm timepieces.

In conventional electronic alarm timepieces, coincidence between the count in a time counting circuit and a pre-determined alarm time set in a memory circuit is continuously detected. The count in the time counting circuit and the count in the memory circuit are applied to a coincidence detecting circuit which generates a coincidence signal when coincidence occurs.

In the case of a conventional multi-alarm electronic timepiece it is necessary to provide a coincidence detecting circuit for each memory circuit in which a predetermined alarm time is set. The circuitry therefore becomes complicated. Moreover, in the conventional multi-alarm timepiece is a wrist-watch, a display device selectively displays the time indication and alarm times.

According to the present invention there is provided an electronic alarm timepiece comprising: a timekeeping circuit for producing an actual time of day indication; a plurality of memory circuits each of which is arranged to memorise an alarm time; a coincidence detecting circuit for detecting coincidence between the actual time of day indication and each alarm time; and circuit means arranged to be controlled by an output signal from the timekeeping circuit for sequentially and periodically signalling the contents of the memory circuits to the coincidence detecting circuit.

Preferably the timepiece includes a display device for selectively displaying the actual time of day indication and the alarm times.

In one embodiment the display device is a liquid crystal display device, the period of the said output signal from the timekeeping circuit being less than the response period of the display device.

In another embodiment the display device is composed of light emitting diodes, the period of said output signal from the timekeeping circuit being less than the response time of the eye.

Preferably the timepiece includes audible warning means for producing an audible warning when the actual time of day indication coincides with each alarm time.

The invention is illustrated, merely by way of example, in the accompanying drawing which is a block diagram of one embodiment of an electronic alarm timepiece according to the present invention.

An output signal from an oscillator circuit, including a quartz crystal element (not shown) is applied to a frequency dividing circuit 2 the output signal of which is applied to a seconds counting circuit 3. The seconds counting circuit 3 produces a 1-minute signal having a frequency of 1/60Hz. The 1-minute signal is applied to a wave-shaping circuit 24 composed of a latch circuit for producing a narrow pulse width signal. The output signal from the wave-shaping circuit 24 is applied to a minutes counting circuit 4. The output signal from which is applied to an hours counting circuit 5.

The electronic alarm timepiece also includes a channel selecting/controlling circuit composed of D-type flip-flop circuits 20, 21, 22, a coincidence detecting switch circuit 26, minutes and hours memory circuits 6, 7 constituting a first channel in which a first alarm time is memorised, minutes and hours memory circuits 8, 9 constituting a second channel in which a second alarm time is memorised, a circuit composed of OR circuits 31, 32 and AND circuits 27, 28, 29, 30, for periodically and sequentially signalling

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the contents of the memory circuits 6, 7, 8, 9 to a coincidence detecting circuit 14 for determining coincidence between the actual time of day indication and an alarm time, a time/channel selecting switch circuit 33 for causing a display device 12 to display selectively an actual time of day indication and an alarm time, a decoder 10 and a driving circuit 11 for converting a binary coded decimal (BCD) to segment signals to drive the display device 12, and a buzzer driving circuit 13 for generating an audible alarm signal when the coincidence deciding circuit 14 produces a coincidence signal.

The channel selecting/controlling circuit constituted by the flip-flop circuits 20, 21, 22 is a three-stage ring counter controlled by a mechanical switch (not shown).

When an output signal from the flip-flop circuit 20 is logic 1 the output signals from the flip-flop circuits 21, 22 are logic 0 so that a NOR circuit 23 produces a control signal of logic 1. The control signal from the NOR circuit 23 is fed to the time/channel selecting circuit 33, composed of transmission gates, which causes the actual time of day indication to be displayed by the display device 12.

When the output of the flip-flop circuit 20 is logic 0, and the output of the flip-flop circuit 21 is logic 1, the control signal from the NOR circuit 23 becomes logic 0, whereby the first alarm time set in the first channel is displayed by the display device 12.

When the output signal from the flip-flop circuit 22 is logic 1 the second alarm time set in the second channel is displayed by the display device 12. When the output signal from the flip-flop circuit 22 is logic 1, the control signal from the NOR circuit 23 is logic 0 and is applied to a NOR circuit 25. Since the output signal from a NOR circuit 26A of the wave-shaping circuit 24 is normally maintained at logic 0, the output signal from the NOR circuit 25 is logic 1 and this output signal forms a control signal for the coincidence detecting switch circuit 26. The output signal of logic 1 from the flip-flop circuit 22 is also applied to the AND circuits 29, 30, via the coincidence detecting switch circuit 26, so that the contents of the memory circuits 8, 9 are displayed by the display device 12.

The 1-minute signal from the seconds counting circuit 3 is applied to the wave-shaping circuit 24 in addition to a control signal having a frequency of 32Hz from an intermediate stage of the dividing circuit 2. The output signal of the NOR circuit 26A is, therefore, a pulse signal each pulse having a width of 15msec. Therefore, the output of the NOR circuit 25 is logic 0 for a period of 15msec and this causes the coincidence detecting switch circuit 26 to pass an output signal having a frequency of 128Hz from an intermediate stage of the dividing circuit 2 to

the memory circuits 6, 7, 8, 9. The first alarm time set in the first channel and the second alarm time set in the second channel are successively sampled during this 15msec period, an output signal from the circuit 26 being applied to the coincidence detecting circuit 14. The coincidence detecting circuit 14 is composed of an exclusive OR circuit and an OR circuit and produces a coincidence signal when the time indication coincides with the first alarm time or the second alarm time and this coincidence signal energises the buzzer driving circuit 13.

According to the present invention it is not necessary to continuously detect the coincidence between the actual time of day indication and the set alarm. The coincidence is detected whenever the minute signal is produced, whereby the circuit construction is able to be simplified.

If the display device 12 is a liquid crystal display device the circuit 26 is operated for a period of time which is less than the response time of the liquid crystal display device to eliminate flickering. If the display device 12 is composed of light emitting diodes, the circuit 26 is operated for a period of time which is shorter than the response time of the eye, so that any flickering of the display device is not apparent.

We direct attention to our co-pending Application Numbers 50225/75 (Serial No. 1493640) and 41951/76 (Serial No. 1524139).

WHAT WE CLAIM IS:-

1. An electronic alarm timepiece comprising: a timekeeping circuit for producing an actual time of day indication; a plurality of memory circuits each of which is arranged to memorise an alarm time; a coincidence detecting circuit for detecting coincidence between the actual time of day indication and each alarm time; and circuit means arranged to be controlled by an output signal from the timekeeping circuit for sequentially and periodically signalling the contents of the memory circuits to the coincidence detecting circuit.

2. A timepiece as claimed in claim 1 including a display device for selectively displaying the actual time of day indication and the alarm times.

3. A timepiece as claimed in claim 2 in which the display device is a liquid crystal display device, the period of the said output signal from the timekeeping circuit being less than the response period of the display device.

4. A timepiece as claimed in claim 2 in which the display device is composed of light emitting diodes, the period of said output signal from the timekeeping circuit being less than the response time of the eye.

5. A timepiece as claimed in any preceding claim including audible warning means



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the contents of the memory circuits 6, 7, 8, 9 to a coincidence detecting circuit 14 for determining coincidence between the actual time of day indication and an alarm time, a time/channel selecting switch circuit 33 for causing a display device 12 to display selectively an actual time of day indication and an alarm time, a decoder 10 and a driving circuit 11 for converting a binary boded decimal (BCD) to segment signals to drive the display device 12, and a buzzer driving circuit 13 for generating an audible alarm signal when the coincidence deciding circuit 14 produces a coincidence signal.

The channel selecting/controlling circuit constituted by the flip-flop circuits 20, 21, 22 is a three-stage ring counter controlled by a mechanical switch (not shown).

When an output signal from the flip-flop circuit 20 is logic 1 the output signals from the flip-flop circuits 21, 22 are logic 0 so that a NOR circuit 23 produces a control signal of logic 1. The control signal from the NOR circuit 23 is fed to the time/channel selecting circuit 33, composed of transmission gates, which causes the actual time of day indication to be displayed by the display device 12.

When the output of the flip-flop circuit 20 is logic 0, and the output of the flip-flop circuit 21 is logic 1, the control signal from the NOR circuit 23 becomes logic 0, whereby the first alarm time set in the first channel is displayed by the display device 12.

When the output signal from the flip-flop circuit 22 is logic 1 the second alarm time set in the second channel is displayed by the display device 12. When the output signal from the flip-flop circuit 22 is logic 1, the control signal from the NOR circuit 23 is logic 0 and is applied to a NOR circuit 25. Since the output signal from a NOR circuit 26A of the wave-shaping circuit 24 is normally maintained at logic 0, the output signal from the NOR circuit 25 is logic 1 and this output signal forms a control signal for the coincidence detecting switch circuit 26. The output signal of logic 1 from the flip-flop circuit 22 is also applied to the AND circuits 29, 30, via the coincidence detecting switch circuit 26, so that the contents of the memory circuits 8, 9 are displayed by the display device 12.

The 1-minute signal from the seconds counting circuit 3 is applied to the wave-shaping circuit 24 in addition to a control signal having a frequency of 32Hz from an intermediate stage of the dividing circuit 2. The output signal of the NOR circuit 26A is, therefore, a pulse signal each pulse having a width of 15msec. Therefore, the output of the NOR circuit 25 is logic 0 for a period of 15msec and this causes the coincidence detecting switch circuit 26 to pass an output signal having a frequency of 128Hz from an intermediate stage of the dividing circuit 2 to

the memory circuits 6, 7, 8, 9. The first alarm time set in the first channel and the second alarm time set in the second channel are successively sampled during this 15msec period, an output signal from the circuit 26 being applied to the coincidence detecting circuit 14. The coincidence detecting circuit 14 is composed of an exclusive OR circuit and an OR circuit and produces a coincidence signal when the time indication coincides with the first alarm time or the second alarm time and this coincidence signal energises the buzzer driving circuit 13.

According to the present invention it is not necessary to continuously detect the coincidence between the actual time of day indication and the set alarm. The coincidence is detected whenever the minute signal is produced, whereby the circuit construction is able to be simplified.

If the display device 12 is a liquid crystal display device the circuit 26 is operated for a period of time which is less than the response time of the liquid crystal display device to eliminate flickering. If the display device 12 is composed of light emitting diodes, the circuit 26 is operated for a period of time which is shorter than the response time of the eye, so that any flickering of the display device is not apparent.

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2. A timepiece as claimed in claim 1 including a display device for selectively displaying the actual time of day indication and the alarm times.

3. A timepiece as claimed in claim 2 in which the display device is a liquid crystal display device, the period of the said output signal from the timekeeping circuit being less than the response period of the display device.

4. A timepiece as claimed in claim 2 in which the display device is composed of light emitting diodes, the period of said output signal from the timekeeping circuit being less than the response time of the eye.

5. A timepiece as claimed in any preceding claim including audible warning means

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for producing an audible warning when the actual time of day indication coincides with each alarm time.

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6. An electronic alarm timepiece substantially as herein described with reference to and as shown in the accompanying drawing.

J. MILLER & CO.,
Agents for the Applicants,
Chartered Patent Agents,
LINCOLN HOUSE,
296-302 High Holborn,
LONDON, WC1V 7JH.

10

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