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(54) Title: METHOD FOR SUPPORTING A VARIETY OF INSTRUCTION FETCH UNITS IN A PIPELINE WITH A SINGLE MICROPROCESSOR CORE


(57) Abstract

A processor core suitable for use with a wide variety of instruction fetch units. The processor core contains a plurality of pipe stages including an instruction pointer generation stage (52) and a decoding stage (55). The core bundles all control necessary for downstream pipeline operation with an instruction address in a first stage. The bundle is transmitted outside the core to the instruction fetch unit (59). The instruction fetch unit (59) fetches the instruction and adds it to the bundle, before forwarding the bundle as modified back within the core and down the pipeline. In this way, an external pipeline is introduced providing a connection between discontinuous pipe stages in the core. Additionally, by bundling the control signals and address information in a single bundle that traverses the external pipe stage as a group, synchronization concerns are reduced or eliminated.


