

WAFER PROCESSING METHOD

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a wafer processing method.

Description of the Related Art

While reductions of device chips in thickness and size have been progressing, enhancement of die strength has always been demanded. When a semiconductor device wafer is thinned, a crushed layer formed by a grindstone lowers the die strength, and, therefore, a technique of removing the crushed layer by polishing to thereby enhance the die strength has been carried out. When the crushed layer is removed, however, a gettering effect of the chips is lost, and, in the case of memory devices or the like, it would lead to device defects. In view of this, a technique called gettering dry polish has been devised (see, for example, Japanese Patent No. 4871617).

The technique described in Japanese Patent No. 4871617 is a technique of performing dry polishing by use of a polishing pad containing abrasive grains, in which minute scratches such as to exhibit a gettering effect are formed while the crushed layer is removed by

polishing.

SUMMARY OF THE INVENTION

However, further enhancement of die strength of device chips is desired.

It is an object of the present invention to provide a wafer processing method by which die strength of device chips can be enhanced.

In accordance with an aspect of the present invention, there is provided a wafer processing method of processing a wafer having a semiconductor substrate formed on a front surface thereof with a plurality of streets in a grid pattern and with a device in each of regions partitioned by the streets, the wafer processing method including: a protective member adhering step of adhering a protective member to a front surface side of the wafer; a grinding step of holding the wafer by a chuck table, with the protective member interposed therebetween, and grinding a back surface side of the wafer to thin the wafer to a predetermined thickness; a polishing step of polishing the back surface side of the wafer having been ground in the grinding step, by a polishing pad to remove a crushed layer formed in the grinding step; and a plasma processing step of supplying

a plasmatized inert gas to the back surface side of the wafer, having been polished in the polishing step, to remove a surface layer on the back surface side of the wafer.

Preferably, in the polishing step, while polishing the back surface side of the wafer by use of the polishing pad containing abrasive grains and thereby removing the crushed layer formed in the grinding step, minute processing strains to be a gettering layer are formed by the abrasive grains.

Preferably, in the plasma processing step, a preliminary gettering layer including an amorphous layer is formed at a surface layer on the back surface side of the wafer.

Preferably, the wafer processing method further includes a modified layer forming step of applying a laser beam of such a wavelength as to be transmitted through the semiconductor substrate along the streets to form modified layers inside the wafer along the streets, before carrying out the grinding step. The wafer is divided by a grinding stress by the grinding step, with the modified layers as breakage start points.

Preferably, the wafer processing method includes a cutting step of forming cut grooves of a depth in excess

of a finished thickness by a cutting blade along the streets from the front surface side of the wafer, before carrying out the grinding step. In the grinding step, the cut grooves are exposed to the back surface side, whereby the wafer is divided.

The wafer processing method of the present invention produces an effect that die strength of device chips can be enhanced.

The above and other objects, features and advantages of the present invention and the manner of realizing them will become more apparent, and the invention itself will best be understood from a study of the following description and appended claims with reference to the attached drawings showing some preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view depicting an example of a wafer to be processed by a wafer processing method according to a first embodiment of the present invention;

FIG. 2 is a flow chart depicting the flow of the wafer processing method according to the first embodiment;

FIG. 3 is a perspective view illustrating a

protective member adhering step of the wafer processing method depicted in FIG. 2;

FIG. 4 is a perspective view of the wafer obtained after the protective member adhering step of the wafer processing method depicted in FIG. 2;

FIG. 5 is a side sectional view depicting a preliminary grinding step of the wafer processing method depicted in FIG. 2;

FIG. 6 is a side sectional view depicting a modified layer forming step of the wafer processing method depicted in FIG. 2;

FIG. 7 is a perspective view illustrating a configuration example of a grinding and polishing apparatus for carrying out a grinding step and a polishing step of the wafer processing method depicted in FIG. 2;

FIG. 8 is a side sectional view illustrating the grinding step of the wafer processing method depicted in FIG. 2;

FIG. 9 is a side sectional view illustrating the polishing step of the wafer processing method depicted in FIG. 2;

FIG. 10 is a sectional view illustrating, in an enlarged form, a major part of the wafer after the

polishing step of the wafer processing method depicted in FIG. 2;

FIG. 11 is a sectional view illustrating a configuration of a plasma apparatus used in a plasma processing step of the wafer processing method depicted in FIG. 2;

FIG. 12 is a sectional view illustrating, in an enlarged form, a major part of the wafer undergoing the plasma processing step of the wafer processing method depicted in FIG. 2;

FIG. 13 is a sectional view illustrating, in an enlarged form, a major part of the wafer after the plasma processing step of the wafer processing method depicted in FIG. 2;

FIG. 14 is a flow chart depicting the flow of a wafer processing method according to a second embodiment of the present invention; and

FIG. 15 is a side sectional view depicting a cutting step of the wafer processing method depicted in FIG. 14.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described in detail below, referring to the drawings. The

present invention is not limited by the contents of the description of the following embodiments. In addition, the constituent elements described below include those which can easily be conceived by a person skilled in the art and those substantially equal thereto. Further, the configurations described below can be combined appropriately. Besides, various kinds of omission, substitution, and modification of the configurations are possible within such ranges as not to depart from the gist of the present invention.

(First Embodiment)

A wafer processing method according to a first embodiment of the present invention will be described based on the drawings. FIG. 1 is a perspective view depicting an example of a wafer to be processed by the wafer processing method according to the first embodiment. FIG. 2 is a flow chart depicting the flow of the wafer processing method according to the first embodiment.

The wafer processing method according to the first embodiment is a method of processing a wafer 1 illustrated in FIG. 1. The wafer 1 is a disk-shaped semiconductor wafer or optical device wafer including a semiconductor substrate 2 of silicon, sapphire, gallium arsenide or the like. Note that in the first embodiment,

the semiconductor substrate 2 of the wafer 1 includes silicon. As depicted in FIG. 1, the wafer 1 includes streets 4 formed in a grid pattern on a front surface 3 of the semiconductor substrate 2, and devices 5 formed in regions partitioned by the streets 4.

The devices 5 are each, for example, an integrated circuit such as an integrated circuit (IC) and a large scale integration (LSI) or an image sensor such as a charge-coupled device (CCD) and a complementary metal oxide semiconductor (CMOS).

The wafer processing method according to the first embodiment is a method by which the wafer 1 is divided along the streets 4 into individual device chips 6, and the device chips 6 are thinned to a finished thickness 100. Note that the device chip 6 includes part of the semiconductor substrate 2 and the device 5 formed on the front surface 3 of the semiconductor substrate 2. As depicted in FIG. 2, the wafer processing method includes a protective member adhering step ST1, a preliminary grinding step ST2, a modified layer forming step ST3, a grinding step ST4, a polishing step ST5, and a plasma processing step ST6.

(Protective Member Adhering Step)

FIG. 3 is a perspective view illustrating the

protective member adhering step of the wafer processing method depicted in FIG. 2. FIG. 4 is a perspective view of the wafer obtained after the protective member adhering step of the wafer processing method depicted in FIG. 2. The protective member adhering step ST1 is a step of adhering a protective tape 20 as a protective member to the front surface 3 side of the wafer 1.

In the first embodiment, in the protective member adhering step ST1, the protective tape 20 the same in diameter as the wafer 1 is adhered to the front surface 3 of the wafer 1, as illustrated in FIGS. 3 and 4. While the protective tape 20 is used as the protective member in the first embodiment, the protective member in the present invention is not limited to the protective tape 20. After the protective tape 20 is adhered to the front surface 3 of the wafer 1, as depicted in FIG. 4, the wafer processing method proceeds to the preliminary grinding step ST2.

(Preliminary Grinding Step)

FIG. 5 is a side sectional view illustrating the preliminary grinding step of the wafer processing method depicted in FIG. 2. The preliminary step ST2 is a step of preliminarily grinding a back surface 7 of the semiconductor substrate 2 of the wafer 1, before the

modified layer forming step ST3, the grinding step ST4, and the polishing step ST5.

In the first embodiment, in the preliminary grinding step ST2, a grinding apparatus 30 holds under suction the front surface 3 side of the semiconductor substrate 2 of the wafer 1 on a holding surface 32 of a chuck table 31, with the protective tape 20 interposed therebetween. As illustrated in FIG. 5, in the preliminary grinding step ST2, while a grinding wheel 34 for preliminary grinding is rotated by a spindle 33 and the chuck table 31 is rotated around an axis and while a grinding liquid 36 is supplied from a grinding liquid nozzle 35, a preliminary grinding grindstone 37 of the grinding wheel 34 is put into contact with the back surface 7 of the semiconductor substrate 2 of the wafer 1, and is brought closer to the chuck table 31 at a predetermined feed speed, to grind the back surface 7 of the wafer 1 by the preliminary grinding grindstone 37.

In the preliminary grinding step ST2, the wafer 1 is ground to a predetermined thickness such that modified layers 8 can be formed by focusing a laser beam 44 (described later) to a desired depth (height) inside the wafer 1 close to the front surface 3 of the wafer 1. In the first embodiment, after the wafer 1 is ground to the

predetermined thickness, the wafer processing method proceeds to the modified layer forming step ST3.

(Modified Layer Forming Step)

FIG. 6 is a side sectional view illustrating the modified layer forming step of the wafer processing method depicted in FIG. 2. The modified layer forming step ST3 is a step of applying the laser beam 44 of such a wavelength (in the embodiment, 1300 to 1064 nm) as to be transmitted through the semiconductor substrate 2 of the wafer 1 along the streets 4 from the back surface 7 side of the semiconductor substrate 2 of the wafer 1, to form modified layers 8 inside the semiconductor substrate 2 of the wafer 1 along the streets 4, before carrying out the grinding step ST4.

Note that the modified layer 8 means a region where density, refractive index, mechanical strength, or other physical property is in a state different from that in the surroundings, and examples thereof include a melting treatment region, a cracked region, a dielectric breakdown region, a refractive index change region, and a region in which these regions are mixedly present. In addition, the modified layer 8 is lower than the other parts of the wafer 1 in mechanical strength or the like.

In the first embodiment, in the modified layer

forming step ST3, a laser processing apparatus 40 holds under suction the front surface 3 side of the semiconductor substrate 2 of the wafer 1 on a holding surface 42 of a chuck table 41, with the protective tape 20 interposed therebetween. In the modified layer forming step ST3, the laser processing apparatus 40 applies the pulsed laser beam 44 along the streets 4 by setting a focal point 44-1 of a laser beam applying unit 43 to a position inside the semiconductor substrate 2, as depicted in FIG. 6, while relatively moving the chuck table 41 and the laser beam applying unit 43 along the streets 4.

In the first embodiment, in the modified layer forming step ST3, the laser processing apparatus 40 applies the laser beam 44 while moving the chuck table 41 in such a manner that the laser beam applying unit 43 is moved from the position indicated by a dotted line in FIG. 6 toward the position indicated by a solid line in FIG. 6 in relation to the wafer 1 suction held by the chuck table 41. Since the laser beam 44 has such a wavelength as to be transmitted through the wafer 1, in the modified layer forming step ST3, as illustrated in FIG. 6, the modified layer 8 is formed inside the semiconductor substrate 2 along the street 4. In the modified layer

forming step ST3, the modified layers 8 are formed in those regions inside the wafer 1 which are to be removed in the grinding step ST4. In addition, in the present invention, before the modified layer forming step ST3 and before the protective member adhering step ST1, a functional layer at the front surface 3 of the semiconductor substrate 2 for forming the devices 5 may be subjected to ablation, to form laser processed grooves where the functional layer has been removed along the streets 4.

In the modified layer forming step ST3, after the modified layers 8 are formed inside the semiconductor substrate 2 along all the streets 4, the application of the laser beam 44 and the holding of the chuck table 41 under suction are released, and the laser processing method proceeds to the grinding step ST4. The grinding step ST4 is carried out by a grinding and polishing apparatus 50 illustrated in FIG. 7.

(Grinding and Polishing Apparatus)

FIG. 7 is a perspective view illustrating a configuration example of a grinding and polishing apparatus for carrying out the grinding step and the polishing step of the wafer processing method depicted in FIG. 2. As illustrated in FIG. 7, the grinding and

polishing apparatus 50 mainly includes an apparatus main body 51, a first grinding unit 52, a second grinding unit 53, a polishing unit 54, a chuck table 56, that is, for example, four in this drawing, and is disposed on a turntable 55, cassettes 57 and 58, an aligning unit 59, a conveying-in unit 60, a conveying-out unit 61, a cleaning unit 62, a conveying-in/out unit 63, and a control unit (not illustrated).

The first grinding unit 52 is for rough grinding the back surface 7 of the wafer 1 held by a chuck table 56 at a rough grinding position 302, by pressing a grinding wheel 52-2 having a grindstone 52-1 mounted to a lower end of a spindle against the back surface 7 of the wafer 1 along a Z axis direction parallel to the vertical direction while rotating the grinding wheel 52-2. Similarly, the second grinding unit 53 is for finish grinding the back surface 7 of the rough-ground wafer 1 held by the chuck table 56 located at a finish grinding position 303, by pressing a grinding wheel 53-2 having a grindstone 53-1 mounted to a lower end of a spindle against the back surface 7 of the rough-ground wafer 1 along the Z axis direction while rotating the grinding wheel 53-2.

Note that in the first embodiment, axes as

rotational centers of the grinding wheels 52-2 and 53-2 of the first grinding unit 52 and the second grinding unit 53 and an axis as a rotational center of the chuck table 56 are parallel to one another and are disposed at intervals in a horizontal direction. Note that in the first embodiment, the grinding units 52 and 53 grind the back surface 7 of the wafer 1 while supplying the wafer 1 with grinding liquids 52-4 and 53-4 (illustrated in FIG. 8) such as pure water.

As illustrated in FIG. 7, the polishing unit 54 has a polishing pad 54-1 of a polishing tool 54-2 mounted to a lower end of a spindle, the polishing pad 54-1 facing a holding surface of the chuck table 56. The polishing unit 54 presses the polishing tool 54-2 against the back surface 7 of the finish-ground wafer 1 held by the holding surface of the chuck table 56 located at a polishing position 304 along the Z axis direction while rotating the polishing tool 54-2. The polishing unit 54 is for polishing the back surface 7 of the wafer 1 by pressing the polishing pad 54-1 of the polishing tool 54-2 against the back surface 7 of the wafer 1 along the Z axis direction.

The polishing pad 54-1 includes abrasive grains dispersed in a flexible base material such as a polishing

cloth, rubber, or elastomer. In the first embodiment, the abrasive grains of the polishing pad 54-1 are conditioned to be equal to or higher than the wafer 1 in hardness, which means that the hardness of the abrasive grains is comparable to that of the wafer 1 or is higher than but not so different from that of the wafer 1, and which excludes the case where the hardness of the abrasive grains is much higher than that of the wafer 1. Next, the abrasive grains are conditioned to be blocky in shape with a grain diameter of 5 μm or less, which means that the grain diameter is minute and the grain shape is a polyhedron such as a cuboctahedron not having a sharp corner and comparatively close to a spherical shape. Incidentally, a shape having a sharp corner conversely to a blocky shape is called an angular shape, and abrasive grains having an angular shape are deemed as unsuitable in the present invention.

In addition, in the first embodiment, the abrasive grains are what is called general abrasive grains. Specifically, in the case where the semiconductor substrate 2 of the wafer 1 is silicon, general abrasive grains whose Mohs hardness is equal to or greater than the Mohs hardness 7 of silicon, and polycrystalline or single-crystal silicon oxide (SiO_2), for example, is used.

Besides, general abrasive grains such as abrasive grains of green carbon (GC) and white alundum (WA) having a Mohs hardness of 9 may be used, but abrasive grains of diamond having a Mohs hardness of 10 are too hard and are unsuitable.

Besides, in the first embodiment, the polishing unit 54 subjects the back surface 7 of the wafer 1 to dry polishing, or what is called dry polish, without supplying a processing liquid such as a polishing liquid.

The turntable 55 is a disk-shaped table provided at an upper surface of the apparatus main body 51, is provided to be rotatable in a horizontal plane, and is rotationally driven at a predetermined timing. For example, four chuck tables 56 are disposed on the turntable 55 at regular intervals of phase angle of 90 degrees, for example. Each of these four chuck tables 56 is of a chuck table structure having a vacuum chuck (suction chuck) at a holding surface thereof, and holds under vacuum (holds under suction) the wafer 1 whose front surface 3 side is disposed on the holding surface, with the protective tape 20 interposed therebetween. These chuck tables 56 are rotationally driven in a horizontal plane around axes parallel to the vertical direction as rotational axes by rotational driving

mechanisms, at the time of grinding and at the time of polishing. Such a chuck table 56 is moved sequentially to a conveying-in/out position 301, a rough grinding position 302, a finish grinding position 303, a polishing position 304, and the conveying-in/out position 301 by rotation of the turntable 55.

The cassettes 57 and 58 are accommodating units for accommodating the wafers 1 that have a plurality of slots. The cassette 57 on one side accommodates the wafers 1 which have the protective tapes 20 adhered to the front surfaces 3 thereof and which are yet to be ground and polished, while the cassette 58 on the other side accommodates the wafers 1 having been ground and polished. In addition, the aligning unit 59 is a table on which to temporarily place the wafer 1 taken out of the cassette 57 and which is for center alignment.

The conveying-in unit 60 has a suction pad, holds under suction the wafer 1 yet to be ground and polished which has been aligned by the aligning unit 59, and conveys the wafer 1 onto the chuck table 56 located at the conveying-in/out position 301. The conveying-out unit 61 holds under suction the wafer 1 having been ground and polished which is held on the chuck table 56 located at the conveying-in/out position 301, and conveys the wafer

1 out to the cleaning unit 62.

The conveying-in/out unit 63 is a robot pick having a circular type handle 63-1, for example, and holds under suction the wafer 1 by the circular type handle 63-1 and conveys the wafer 1. Specifically, the conveying-in/out unit 63 conveys out the wafer 1 yet to be ground and polished from the cassette 57 to the aligning unit 59, and conveys the wafer 1 having been ground and polished from the cleaning unit 62 into the cassette 58. The cleaning unit 62 cleans the wafer 1 having been ground and polished, to remove contaminations such as grinding swarf and polishing swarf adhering to the processed surface having been ground and polished.

The control unit is for controlling the above-mentioned components constituting the grinding and polishing apparatus 50. In other words, the control unit is for causing the grinding and polishing apparatus 50 to perform a polishing operation on the wafer 1. The control unit is a computer capable of executing a computer program. The control unit includes an arithmetic processing apparatus having a microprocessor such as a central processing unit (CPU), a storage apparatus having a memory such as a read only memory (ROM) and a random access memory (RAM), and an input/output interface

apparatus. The arithmetic processing apparatus of the control unit executes a computer program stored in the storage apparatus, and produces control signals for controlling the grinding and polishing apparatus 50. The arithmetic processing apparatus of the control unit outputs the produced control signals to the components of the grinding and polishing apparatus 50 through the input/output interface device.

(Grinding Step)

FIG. 8 is a side sectional view illustrating the grinding step of the wafer processing method depicted in FIG. 2. The grinding step ST4 is a step of holding of the wafer 1 on the holding surface of the chuck table 56 under suction, with the protective tape 20 interposed therebetween, and grinding the back surface 7 side of the wafer 1 to thin the wafer 1 to a predetermined thickness. In the first embodiment, in the grinding step ST4, the cassette 57 accommodating the wafers 1 having the protective tapes 20 adhered to the front surfaces 3 thereof and the cassette 58 not accommodating the wafers 1 are mounted to the apparatus main body 51 of the grinding and polishing apparatus 50, the operator registers processing contents information in the control unit, and, when a starting instruction for a processing

operation is inputted from the operator, the processing operation (grinding) is carried out by the grinding and polishing apparatus 50.

In the grinding step ST4, the grinding and polishing apparatus 50 causes the conveying-in/out unit 63 to take out the wafer 1 from the cassette 57, and to convey the wafer 1 to the aligning unit 59, and causes the aligning unit 59 to align the center of the wafer 1. In the grinding step ST4, the grinding and polishing apparatus 50 causes the conveying-in unit 60 to convey the wafer 1, whose center has been aligned, onto the chuck table 56 located at the conveying-in/out position 301.

In the grinding step ST4, the grinding and polishing apparatus 50 holds under suction the front surface 3 side of the wafer 1 on the chuck table 56, with the protective tape 20 interposed therebetween, to expose the back surface 7, and causes the turntable 55 to convey the wafer 1 sequentially to the rough grinding position 302 and the finish grinding position 303. In the grinding step ST4, as illustrated in FIG. 8, at the rough grinding position 302 and the finish grinding position 303, the grinding and polishing apparatus 50, while rotating the grinding wheels 52-2 and 53-2 by the spindles and

rotating the chuck tables 56 around axes, supplies the grinding liquids 52-4 and 53-4 from the grinding liquid nozzles 52-3 and 53-3, and puts the grindstones 52-1 and 53-1 into contact with the back surface 7 of the semiconductor substrate 2 of the wafer 1 and brings the grindstones 52-1 and 53-1 closer to the chuck tables 56, to thereby sequentially perform rough grinding and finish grinding on the back surface 7 of the wafer 1 by the grindstones 52-1 and 53-1. In the grinding step ST4, the wafer 1 is ground until a predetermined thickness is reached.

In addition, in the first embodiment, in the grinding step ST4, by grinding stresses exerted from the grinding wheels 52-2 and 53-2 of the first grinding unit 52 at the rough grinding position 302 in the grinding step ST4, the wafer 1 is divided along the streets into the individual device chips 6, with the modified layers 8 as breakage start points. In the first embodiment, after the wafer 1 is ground to the predetermined thickness, the wafer processing method proceeds to the polishing step ST5. Note that the wafer 1 after the grinding step ST4 has a crushed layer (not illustrated) formed at the surface layer of the back surface 7. The crushed layer is processing strains such as crystal defects and strains.

(Polishing Step)

FIG. 9 is a side sectional view illustrating the polishing step of the wafer processing method depicted in FIG. 2. FIG. 10 is a sectional view illustrating, in an enlarged form, a major part of the wafer after the polishing step of the wafer processing method depicted in FIG. 2. The polishing step ST5 is a step of polishing the back surface 7 side of the wafer 1, having been ground in the grinding step ST4, by the polishing pad 54-1, to remove the crushed layer formed in the grinding step ST4. In the first embodiment, the polishing step ST5 is a step of polishing the back surface 7 side of the wafer 1, having been ground in the grinding step ST4, by the polishing pad 54-1 containing the abrasive grains, to form minute processing strains 11 to be a gettering layer 10 by the abrasive grains while removing the crushed layer formed in the grinding step ST4.

In the first embodiment, the gettering layer 10 is a layer exhibiting what is called a gettering ability to capture impurities mainly including metals such as copper (Cu) ions adhering to the wafer 1 and to restrain metal contamination of the devices 5 by the impurities. The processing strains 11 are minute crystal defects and strains formed in the surface layer of the back surface 7

of the semiconductor substrate 2 of the wafer 1. The crystal defects and strains of the processing strains 11 are smaller than the crystal defects and strains of the crushed layer.

In the polishing step ST5, the grinding and polishing apparatus 50 rotates the turntable 55 to move the chuck table 56 holding thereon the wafer 1 having been finish ground to the polishing position 304, at which, while rotating the polishing tool 54-2 by a spindle and rotating the chuck table 56 around an axis, as depicted in FIG. 9, the polishing pad 54-1 is put into contact with the back surface 7 of the semiconductor substrate 2 of the wafer 1 and is brought closer to the chuck table 56 at a predetermined feed speed, whereby the back surface 7 of the wafer 1 is subjected to dry polishing by the polishing pad 54-1. In the polishing step ST5, after the grinding and polishing apparatus 50 performs dry polishing for a predetermined period of time, the polishing is finished by the polishing unit 54, the wafer 1 polished by the polishing unit 54 is positioned at the conveying-in/out position 301, is conveyed into the cleaning unit 62 by the conveying-out unit 61, and is cleaned by the cleaning unit 62, and the wafer 1 having been cleaned is conveyed into the cassette 58 by the

conveying-in/out unit 63.

The wafer processing method proceeds to the plasma processing step ST6. Note that as illustrated in FIG. 10, the wafer 1 after the polishing step ST5 has the minute processing strains 11 such as minute crystal defects and strains, to be the gettering layer 10, formed at the surface layer of the back surface 7.

In such a way, in the grinding step ST4 and the polishing step ST5, the grinding and polishing apparatus 50 conveys the wafer 1 sequentially to the rough grinding position 302, the finish grinding position 303, the polishing position 304, and the conveying-in/out position 301 by the turntable 55, and performs rough grinding, finish grinding, and polishing sequentially, to thereby planarize the back surface 7 of the wafer 1 with high accuracy. Note that in the grinding and polishing apparatus 50, each time the turntable 55 is rotated by 90 degrees, the wafer 1 yet to be ground and polished is conveyed onto the chuck table 56 at the conveying-in/out position 301. After all the wafers 1 in the cassette 57 are ground and polished, the grinding and polishing apparatus 50 finishes the processing operation.

(Plasma Processing Step)

FIG. 11 is a sectional view illustrating the

configuration of a plasma apparatus used in the plasma processing step of the wafer processing method depicted in FIG. 2. FIG. 12 is a sectional view illustrating, in an enlarged form, a major part of the wafer undergoing the plasma processing step of the wafer processing method depicted in FIG. 2. FIG. 13 is a sectional view illustrating, in an enlarged form, a major part of the wafer after the plasma processing step of the wafer processing method depicted in FIG. 2.

The plasma processing step ST6 is a step in which the plasma apparatus 70 illustrated in FIG. 11 supplies a plasmatized inert gas 400 (depicted in FIG. 12) to the back surface 7 side of the wafer 1 having been polished in the polishing step ST5, and subjects the wafer 1 to plasma processing, to remove silicon 401 constituting the surface layer on the back surface 7 side of the wafer 1 and to form the gettering layer 10. In the first embodiment, the plasma processing step ST6 is a step of plasma processing the wafer 1 to remove the silicon 401 constituting the surface layer of the processing strains 11 on the back surface 7 side of the wafer 1. In the plasma processing step ST6, the plasma apparatus 70 places the front surface 3 side of the wafer 1 on a chuck table 74 (electrostatic chuck (ESC)) constituting a lower

electrode 73 located in a hermetically sealed space 72 in a plasma etching chamber 71, with the protective tape 20 interposed therebetween, and impresses electric power to electrodes 75 and 76 to hold under suction the wafer 1 on the chuck table 74.

In the plasma processing step ST6, the plasma apparatus 70 hermetically seals the hermetically sealed space 72 in the plasma etching chamber 71, operates a gas discharge unit 77 to evacuate the inside of the hermetically sealed space 72, maintains the pressure inside the hermetically sealed space 72 at a predetermined pressure, and operates a coolant supply unit 78 to circulate a helium gas as a coolant in a coolant introduction passage 79, a cooling passage 80, and a coolant discharge passage 81 which are formed in the lower electrode 73, to thereby restrain an abnormal temperature rise of the lower electrode 73.

In the plasma processing step ST6, an inert gas supply unit 82 is operated to jet an inert gas from a plurality of jet ports 85 of an upper electrode 84 toward the wafer 1 held on the chuck table 74 of the lower electrode 73. Besides, in the plasma processing step ST6, in the state in which the inert gas is supplied, the plasma apparatus impresses high frequency electric power

for producing and maintaining plasma on the upper electrode 84 from a high frequency power source 83, and impresses high frequency electric power for drawing in ions on the lower electrode 73 from the high frequency power source 83. As a result, a plasmatized inert gas 400 (depicted in FIG. 12) is generated in a space between the lower electrode 73 and the upper electrode 84, and the plasmatized inert gas 400 impinges on the back surface 7 of the wafer 1. Note that the plasma apparatus 70 supplies an argon gas as the inert gas in the first embodiment, but the inert gas in the present invention is not limited to the argon gas.

In the first embodiment, in the plasma processing step ST6, as illustrated in FIG. 12, the surface layer of the holding surface of the chuck table 74 is electrified in minus 402, and the wafer 1 is suction held on the holding surface of the chuck table 74, whereas the plasmatized inert gas 400 electrified in plus is drawn toward the wafer 1, and impinges on the back surface 7. Then, in the plasma processing step ST6, silicon 401 of the surface layer of the processing strains 11 on the back surface 7 side of the wafer 1 is removed, the surface layer of the processing strains 11 is modified into an amorphous-formed amorphous layer 12-1 which is a

crystal strain layer, and a preliminary gettering layer 12 (depicted in FIG. 13) including the amorphous layer 12-1 is formed at the surface layer of the processing strains 11 on the back surface 7 side. The amorphous layer 12-1 is an amorphous-formed layer to which crystal defects and strains smaller than the processing strains 11 have been imparted, and the amorphous layer 12-1 exhibits what is called a gettering ability to capture impurities mainly including metals such as copper (Cu) ions contained in the wafer 1 and to restrain metal contamination of the devices 5 by the impurities. In such a way, in the wafer 1, a gettering layer 10 including the processing strains 11 and the preliminary gettering layer 12 is formed on the back surface 7 of the semiconductor substrate 2.

After the plasmatized inert gas 400 is caused to impinge on the back surface 7 of the wafer 1 for a predetermined period of time, the wafer processing method is finished. Note that as illustrated in FIG. 13, the wafer 1 after the plasma processing step has been thinned to the finished thickness 100, and has been formed, at the surface layer of the back surface 7 thereof, with the gettering layer 10 including the preliminary gettering layer 12 and the processing strains 11.

In the wafer processing method according to the first embodiment, the minute processing strains 11 to be the gettering layer 10 are formed in the polishing step ST5 in which dry polishing is conducted, and the plasma processing by use of the inert gas is conducted in the plasma processing step ST6, whereby the surface layer of the minute processing strains 11 on the back surface 7 of the polished wafer 1 is removed. As a result, the wafer processing method according to the first embodiment can enhance the die strength of the device chips 6, even though the gettering ability is imparted.

In addition, in the wafer processing method according to the first embodiment, the surface layer of the minute processing strains 11 is removed by the plasma processing and the preliminary gettering layer 12 smaller in crystal defects and strains than the processing strains 11 is formed in the plasma processing step ST6; therefore, the die strength can be enhanced as compared to device chips including a gettering layer 10 composed only of the processing strains 11 formed by the polishing step ST5.

Further, in the wafer processing method, the gettering layer 10 including the preliminary gettering layer 12 is formed on the back surface 7 of the

semiconductor substrate 2 by the plasma processing; therefore, there is obtained an effect that the gettering layer 10 can be formed all over the whole surface of the back surface 7, as compared to a processing strain layer in which minute scratches are formed at random.

Besides, in the wafer processing method, the grinding step ST4 and the polishing step ST5 are performed by the same grinding and polishing apparatus 50, and there is a risk of metal contamination of the wafer 1 during conveyance of the wafer 1 to the plasma apparatus after the polishing step ST5; however, there is obtained an effect that metal contamination of the device chips 6 can be avoided by the processing strains 11 already formed in the polishing step ST5.

In addition, in the wafer processing method, the plasma processing by use of the inert gas is conducted in the plasma processing step ST6; therefore, a detoxifying treatment for the discharged gas is unnecessary, and there is obtained an effect that equipment simplification is possible, as compared to the case where such a gas as SF_6 is used.

(Second Embodiment)

A wafer processing method according to a second embodiment of the present invention will be described,

based on the drawings. FIG. 14 is a flow chart depicting the flow of the wafer processing method according to the second embodiment. FIG. 15 is a side sectional view illustrating a cutting step of the wafer processing method depicted in FIG. 14. Note that in FIGS. 14 and 15, the parts which are the same as those in the first embodiment above are denoted by the same reference symbols as used above, and descriptions of them will be omitted.

As depicted in FIG. 14, the wafer processing method according to the second embodiment is the same as that in the first embodiment, except for including a cutting step ST10 in place of the modified layer forming step ST3. The cutting step ST10 is a step of forming cut grooves 9 of a depth in excess of a finished thickness 100 by a cutting blade 94 along streets 4 from the front surface 3 side of a semiconductor substrate 2 of a wafer 1, before carrying out a grinding step ST4. In the second embodiment, in the wafer processing method, the cutting step ST10 is conducted before a protective member adhering step ST1; however, in the present invention, the cutting step ST10 may be carried out after a preliminary grinding step ST2 insofar as it is carried out before the grinding step ST4.

In the second embodiment, in the cutting step ST10,

a dicing tape 21 is adhered to a back surface 7 of a wafer 1, and a cutting apparatus 90 holds under suction the back surface 7 side of the wafer 1 on a holding surface 92 of a chuck table 91, with the dicing tape 21 interposed therebetween. As depicted in FIG. 15, in the cutting step ST10, while relatively moving the chuck table 91 and the cutting blade 94 of a cutting unit 93 along the street 4, the cutting apparatus 90 causes the cutting blade 94 to cut into the wafer 1 from the front surface 3 to a depth in excess of the finished thickness 100, to form the cut groove 9. In the present invention, in the cutting step ST10, cutting may be conducted without adhering the dicing tape 21 to the back surface 7.

In the second embodiment, in the cutting step ST10, the cutting apparatus 90 causes the cutting blade 94 to cut into the wafer 1 suction held by the chuck table 91 along the street 4, while moving the chuck table 91 in such a manner that the cutting blade 94 goes from the position indicated by an alternate long and two short dashes line in FIG. 15 toward the position indicated by a solid line in FIG. 15.

In the cutting step ST10, after the cut grooves 9 are formed in the semiconductor substrate 2 along all the streets 4, the cutting by use of the cutting blade 94 and

the holding of the chuck table 91 under suction are released, and the wafer processing method proceeds to the protective member adhering step ST1. In the protective member adhering step ST1 of the wafer processing method according to the second embodiment, after the protective tape 20 is adhered to the front surface 3 of the wafer 1, the dicing tape 21 is peeled off from the back surface 7 side. In addition, in the grinding step ST4 of the wafer processing method according to the second embodiment, the cut grooves 9 are exposed on the back surface 7 side, and the wafer 1 is divided into individual device chips 6. Besides, in the present invention, a functional layer at the front surface 3 of the semiconductor substrate 2 for forming devices 5 may be subjected to ablation, to form laser processed grooves deprived of the functional layer along the streets 4, before the cutting step ST10 and before the protective member adhering step ST1. Note that in this case, the laser processed grooves are wider than the cut grooves 9.

In the wafer processing method according to the second embodiment, in the polishing step ST5 of performing dry polishing, minute processing strains 11 to be a gettering layer 10 are formed, and, in a plasma processing step ST6, plasma processing by use of an inert

gas is conducted, to remove a surface layer of the minute processing strains 11 on the back surface 7 of the polished wafer 1. As a result, the wafer processing method according to the second embodiment is capable of enhancing the die strength of the device chips 6, like that according to the first embodiment.

Next, the present inventors confirmed the effect of the wafer processing method according to the first embodiment. The results are set forth in Table 1 below.

[Table 1]

	Die strength
Comparative Example 1	1,350 MPa
Comparative Example 2	1,670 MPa
Present Invention Product 1	2,107 MPa
Present Invention Product 2	3,631 MPa

In the confirmation, die strength was measured for the device chips 6 of Comparative Example 1, Comparative Example 2, Present Invention Product 1, and Present Invention Product 2. Comparative Example 1 was obtained by a method in which the protective member adhering step ST1, the preliminary grinding step ST2, the modified layer forming step ST3, the grinding step ST4, and the polishing step ST5 were carried out using a polishing tool DPEG produced by DISCO Corporation, to form a

gettering layer 10 including only the processing strains 11. Comparative Example 2 was obtained by a method in which the protective member adhering step ST1, the preliminary grinding step ST2, the modified layer forming step ST3, the grinding step ST4, and the polishing step ST5 were carried out using a polishing tool DP08 produced by DISCO Corporation, to form a gettering layer 10 including only the processing strains 11.

Present Invention Product 1 was obtained by a method in which the protective member adhering step ST1, the preliminary grinding step ST2, the modified layer forming step ST3, the grinding step ST4, the polishing step ST5, and the plasma processing step ST6 were carried out using a polishing tool DPEG produced by DISCO Corporation, to form a gettering layer 10 including the processing strains 11 and the preliminary gettering layer 12. Present Invention Product 2 was obtained by a method in which the protective member adhering step ST1, the preliminary grinding step ST2, the modified layer forming step ST3, the grinding step ST4, the polishing step ST5, and the plasma processing step ST6 were carried out using a polishing tool DP08 produced by DISCO Corporation, to form a gettering layer 10 including the processing strains 11 and the preliminary gettering layer 12.

In addition, Table 1 indicates average values of die strength of a plurality of device chips 6 measuring 10 mm by 10 mm by 25 μ m (thickness) of Comparative Example 1, Comparative Example 2, Present Invention Product 1, and Present Invention Product 2, measured by three-point bending with an inter-fulcrum distance (span) of 1.4 mm.

According to Table 1, the die strength of Comparative Example 1 was 1,350 MPa, while the die strength of Present Invention Product 1 was 2,107 MPa; thus, the die strength of Present Invention Product 1 was beyond 1.5 times the die strength of Comparative Example 1. According to Table 1, the die strength of Comparative Example 2 was 1,670 MPa, while the die strength of Present Invention Product 2 was 3,631 MPa; thus, the die strength of Present Invention Product 2 was beyond 2.1 times the die strength of Comparative Example 2. According to Table 1, therefore, it is verified that it is possible, by carrying out the plasma processing step ST6 after the polishing step ST5, to enhance the die strength of the device chips 6.

Note that the present invention is not limited to the above-described embodiments. In other words, the present invention can be carried out with various

modifications within such ranges as not to depart from the gist of the invention. For example, in the above embodiments, in the polishing step ST5, what is called dry polishing was performed to form minute processing strains 11 in the back surface 7. However, in the present invention, in the polishing step ST5, the back surface 7 may be polished while a processing liquid is supplied for chemical mechanical polishing (CMP) or the like, to remove the crushed layer formed in the grinding step ST4, without forming the processing strains 11. In other words, the polishing step ST5 may be a step of polishing the back surface 7 side of the wafer, having been ground in the grinding step ST4, by a polishing pad, to remove the crushed layer formed in the grinding step ST4, and the plasma processing step ST6 may be a step of supplying the plasmatized inert gas 400 to the back surface 7 side of the wafer 1, having been polished in the polishing step ST5, to form the gettering layer 10 on the back surface 7 side of the wafer 1. In addition, the polishing step ST5 in the present invention is not limited to the CMP polishing, and may be dry polishing (dry polish) conducted using a polishing pad containing abrasive grains of silica or the like in a polishing cloth or an elastomer, particularly, a polishing pad containing

abrasive grains of one or more of silica, alumina, forsterite, steatite, mullite, cubic boron nitride, diamond, silicon nitride, silicon carbide, boron carbide, barium carbonate, calcium carbonate, iron oxide, magnesium oxide, zirconium oxide, cerium oxide, chromium oxide, tin oxide, and titanium oxide, as described in Japanese Patent Laid-Open No. 2002-283243.

The present invention is not limited to the details of the above described preferred embodiments. The scope of the invention is defined by the appended claims and all changes and modifications as fall within the equivalence of the scope of the claims are therefore to be embraced by the invention.

WHAT IS CLAIMED IS:

1. A wafer processing method of processing a wafer having a silicon semiconductor substrate formed on a front surface thereof with a plurality of streets in a grid pattern and with a device in each of regions partitioned by the streets, the wafer processing method comprising:

a protective member adhering step of adhering a protective member to a front surface side of the wafer;

a grinding step of holding the wafer by a chuck table, with the protective member interposed therebetween, and grinding a back surface side of the wafer to thin the wafer to a predetermined thickness;

a polishing step of polishing the back surface side of the wafer, having been ground in the grinding step, by a polishing pad containing abrasive grains to remove a crushed layer formed in the grinding step and at the same time, to form processing strains being a gettering layer on the back surface of the wafer; and

a plasma processing step of supplying a plasmatized inert gas to the back surface side of the wafer, having been polished in the polishing step, to remove silicon of a surface layer of the processing strains and to modify the surface layer of the processing strain into an amorphous-formed layer being a preliminary gettering layer so that the gettering layer processed after the plasma processing step includes processing

strains formed on the back surface of the wafer and a preliminary gettering layer formed at the surface of processing strains.

2. The wafer processing method according to claim 1, further comprising:

a modified layer forming step of applying a laser beam of such a wavelength as to be transmitted through the semiconductor substrate along the streets to form modified layers inside the wafer along the streets, before carrying out the grinding step, wherein

the wafer is divided by a grinding stress by the grinding step, with the modified layers as breakage start points.

3. The wafer processing method according to claim 1, further comprising:

a cutting step of forming cut grooves of a depth in excess of a finished thickness by a cutting blade along the streets from the front surface side of the wafer, before carrying out the grinding step, wherein,

in the grinding step, the cut grooves are exposed on the back surface side, whereby the wafer is divided.