

BARRIER LAYERS FOR SOLDER JOINTS

Field of the Invention

The present invention relates to fabrication of a solder joint for an interconnection
5 between a semiconductor chip and a temperature sensitive substrate. In particular, the
present invention relates to a fabrication of barrier layers between a solder ball/bump
and ball-limiting metallurgy.

Background of the Invention

10 US Patent No 5,937,320 provides a method of fabricating solder bumps on metallic pads
embedded in a semiconductor wafer. The invention described in the patent specification
attempts to overcome the problem of tin in the solder reacting with copper in the
underlying ball-limiting metallurgy to form intermetallics, particularly at the elevated
temperatures of solder reflow and joining. The copper dissolves in the tin forming a
15 layer of Cu/Sn intermetallics with a non-uniform thickness at the solder copper
interface. This US patent attempts to overcome this problem by providing a barrier
layer on the under-bump metallurgy (also referred to as ball-limiting metallurgy). The
under-bump metallurgy provides a surface that is wettable by the solder and reacts with
the solder to provide good adhesion and acceptable reliability under mechanical and
20 heat stress.

Unfortunately, the barrier layer described in US Patent No 5,937,320 is not always
sufficiently reliable in overcoming the problems of tin-copper intermetallics.

25 The present invention seeks to provide a method of fabricating a solder bump on
metallic pads in a semiconductor wafer that further reduces the problem of tin-copper
intermetallic formation.

Summary of the Invention

30 According to the present invention there is provided a method of forming a solder bump
on metallic pads in a semiconductor wafer, comprising the steps of:
depositing a plurality of blanket metal layers on a passivated surface of a

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semiconductor wafer having at least one metallic pad, the passivated surface including an opening above each metallic pad;

applying a photoresist material to the blanket metal layers;

5 patterning the photoresist material to provide a region for forming a plurality of metallic layers over each metallic pad;

electroplating a first electroplated metallic layer on the region;

electroplating a second electroplated metallic layer on the first electroplated metallic layer;

fabricating a solder bump on the second metallic layer;

10 removing the photoresist material; and

etching the plurality of blanket metal layers using the solder bump as a mask.

According to another aspect of the present invention there is provided a method of forming a solder bump on metallic pads in a semiconductor wafer, comprising the steps of:

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depositing a plurality of blanket metal layers on a passivated surface of a semiconductor wafer having at least one metallic pad, the passivated layer including an opening above each metallic pad;

20 applying a first photoresist material to provide a first region on the blanket metal layers;

patterning the photoresist material to provide the first region for forming a first electroplated metallic layer over each metallic pad;

electroplating the first electroplated metallic layer on the region;

removing the first photoresist material;

25 applying a second photoresist material to the blanket metal layers;

patterning the second photoresist material to provide a second region for forming a second electroplated metallic layer, the second photoresist material patterned so that the second electroplated metallic layer encapsulates the first electroplated metallic layer;

30 electroplating the second electroplated metallic layer so as to encapsulate the first electroplated metallic layer;

fabricating a solder bump on the second electroplated metallic layer;

removing the second photoresist material; and

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etching the plurality of blanket metal layers using the solder bump as a mask.

Preferably, the first electroplated metallic layer is formed of the same metal as the uppermost layer of the plurality of blanket metal layers. Preferably, the first
5 electroplated barrier layer and the uppermost layer of the plurality of blanket metal layers is formed of copper.

Preferably, the second electroplated barrier layer is formed of nickel. Alternatively, the second electroplated barrier layer is formed of a nickel iron alloy.

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Preferably, the blanket metal layers include an adhesion layer that adheres to the underlying metallic pad. Preferably, the blanket metal layer includes a deposited layer on top of the adhesion layer. Preferably, the adhesion layer is formed of Ti/W, Cr or alloys thereof. Preferably, the deposited layer is formed of copper, nickel, gold or alloys
15 thereof.

Preferably, the adhesion layer is formed by sputtering. Preferably, the deposited layer is formed by sputtering.

20 Preferably, the adhesion layer, deposited layer and the first electroplated layer form an under-bump metallurgy. Preferably, the second electroplated layer forms a barrier layer to reduce the formation of intermetallics by interaction with tin in solder. Preferably, the nickel barrier layer is formed to a thickness of between 1 and 5 microns. Preferably, the electroplated copper layer is plated to a thickness of between 1 and 10 microns.
25 Preferably, the nickel layer is formed by electrolytic or electroless plating. Preferably, the nickel barrier layer encapsulates the copper deposited layer and the copper electroplated layer, so that the solder bump does not make contact with the copper in either of these layers. Preferably, the solder is reflowed to form a substantially spherical solder ball.

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Preferably, the semiconductor wafer is formed of silicon. Alternatively, the semiconductor wafer is formed of germanium or gallium arsenide. Preferably, the

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metallic pads are formed of aluminium. Alternatively, the metallic pads are formed of aluminium doped with silicon and copper. Alternatively, the metallic pads are formed of aluminium doped with silicon. Alternatively, the metallic pads are formed of copper or copper doped with other materials. Preferably, the etching of the barrier metal layers
5 forms an under cut between the first electroplated layer and the semiconductor wafer.

Brief Description of the Drawings

In order to provide a better understanding of the present invention, preferred embodiments will now be described in detail, by way of example only, with reference to
10 the accompanying drawings, in which:

- Figure 1 is a schematic representation of a semiconductor wafer coated with blanket metal layers;
- Figure 2 is a schematic representation of the blanket metal layers having a photoresist material applied thereto;
- 15 Figure 3 is a schematic representation of the blanket metal layers having electroplated layers;
- Figure 4 shows a fabricated solder bump on top of the electroplated layers of Figure 3;
- Figure 5 shows the barrier layers, the electroplated layers and the fabricated solder bump without the photoresist material;
- 20 Figure 6 shows the blanket metal layers having been etched;
- Figure 7 shows the solder bump having been reflowed;
- Figure 8 is a schematic representation of a semiconductor wafer coated with blanket metal layers as first step of an alternative process;
- 25 Figure 9 shows the blanket metal layers of Figure 8 with photoresist material having been applied thereto;
- Figure 10 shows an electroplated layer being applied to the blanket metal layers;
- Figure 11 shows an electroplated layer on the blanket metal layers with the photoresist material having been removed;
- 30 Figure 12 shows a second photoresist material having been applied to the barrier layers either side of the electroplated layer;
- Figure 13 shows another electroplated layer having been plated on top of the first

- electroplated layer;
- Figure 14 shows a fabricated solder bump being applied on top of the electroplated layers;
- Figure 15 shows the barrier layers, the electroplated layers and the fabricated solder bump with the photoresist having been removed;
- Figure 16 shows the blanket metal layers having been etched away;
- Figure 17 shows the solder bump having been reflowed; .
- Figure 18 shows the blanket metal layers having been undercut;
- Figure 19 shows the semiconductor wafer with the etched blanket metal layers and electroplated layers, without the fabricated solder bump;
- Figure 20 shows an alternative second electroplated layer to that shown in Figure 19;
- Figure 21 shows a further alternative second electroplated layer to that shown in Figures 19 and 20; and
- Figure 22 shows that after the reflow process of the solder, the solder has flown over the top electroplated layer to make contact with underlying layers.

Referring to Figure 1, there is shown a semiconductor wafer with a plurality of blanket metal layers 10 deposited thereon. The semiconductor wafer is represented as 12. The semiconductor wafer 12 is typically formed of silicon, however it may comprise other materials such as germanium, gallium arsenide, silicon germanium or other suitable semiconductor materials. The wafer typically contains a plurality of integrated circuit devices. These devices are not shown for clarity purposes. Metallic pads are embedded within the semiconductor layer. These metallic pads form a contact for the integrated circuit devices. Metallic pads are typically aluminium, but may also include aluminium doped with silicon and copper, aluminium doped with silicon, copper, or copper doped with other materials. The metallic pads are indicated by 11 in Figure 1. The metallic pad 11 is not shown in the other figures for clarity purposes. However, throughout the rest of the description, it is assumed that the metallic pad is positioned beneath the location onto which electroplated metals will be applied.

Typically, a passivating layer (not shown) of a material such as polyamide, silicon

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dioxide or silicon nitrate is formed on the semi-conducting layer with gaps in the passivating layer above the surface of the metallic pads 11. Prior to the application of the blanket metal layers 10 the passivating layer is cleaned with de-ionised water or solvent.

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On top of the passivated semiconductor wafer 12 is a first blanket metal layer 14. The first blanket metal layer 14 has been known to be formed of Ti, W and Cr and alloys thereof. In the present invention it is preferred to be formed of Chromium. Typically, the Cr is sputtered on to the semiconductor layer. The sputtering process includes the well known steps of converting a condensed phase (generally a solid phase) Cr source into a gaseous or vapour phase, transporting the gaseous or vapour phase from the source to the semiconductor substrate and condensing the gas or vapour phase onto the substrate, which results in nucleation and growth of a film of the deposited metal.

15 A second blanket metal layer 16 is formed on the first barrier layer, again by a process of sputtering. It is preferred in the present invention to use copper, although other metals are known to be used in the prior art, such as nickel, cobalt, and alloys thereof. The copper is sputtered using a similar process as described in relation to the Cr layer.

20 The first layer is generally known as an adhesion layer as it provides adhesion between an interconnect and the wafer. Specifically, the sputtered Cr layer makes electrical contact with the underlying aluminium metallic pad so as to form a good electrical connection. The second blanket metal layer is generally known as the terminal layer as it acts as the terminal for the solder bump to adhere to.

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An intermediate blanket metal layer is known in the prior art to be included between the Cr and copper blanket layers. The intermediate layer is known to include a Cr-copper alloy composed predominantly of Cr at the interface with the Cr layer and predominantly copper at the opposite interface. Such an intermediate layer may be included in the present invention. The blanket metal layers are also known as ball-limiting metallurgy or under-bump metallurgy.

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Next, a thick layer of photoresist material is deposited on the blanket metal layers 10, generally by spin coating the photoresist material onto the surface of the copper layer 16. The photoresist is then developed using well known photolithographic techniques to leave a patterned layer on the photoresist material. Referring to Figure 2, the patterned photoresist material 18 is shown deposited on the blanket metal layers 10.

The pattern will include gaps 15 in the photoresist material so that a mask is provided for preventing the deposition of electroplated metals on top of the blanket metal layers 10 apart from the regions where gaps 15 are formed. The gaps 15 will correspond with the area above the metallic pads 11 so that the electroplated layers will be formed above the pads 11.

Referring to Figure 3, a first electroplated layer 20 is deposited on the blanket metal layers 10. The first electroplated layer 20 is preferably copper, typically plated to a thickness of 1 to 10 microns. Electroplating is conducted by standard electroplating techniques well known to those skilled in the art.

A second electroplated layer 22 is deposited on the first electroplated layer 20. It is preferred that the second electroplated layer 22 be formed of nickel deposited by electroless or electroplating techniques, which are common nickel plating processes. Typically, the nickel is plated to a thickness of between 1 and 5 microns.

The first copper electroplated layer provides extra thickness to the underlying sputtered layer, directly above the metallic pad. The second electroplated layer forms a barrier layer of thickness from about 0.2 to 10 (or more) microns, preferably between 1 and 5 microns.

Referring to Figure 4, a solder bump 24 is fabricated on top of the second electroplated layer 22. The solder bump is comprised of tin and lead. The preferred form of solder is eutectic solder consisting of 63% tin and 37% lead, although other forms of solder may also be used, such as high lead solder consisting of 5% tin and 95% lead. It is also known to use lead-free solder. It is common in the art to electroplate solder. The

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process of electroplating solder will be familiar to those skilled in the art. It is seen in Figure 4 that the solder bump 24 makes contact with the upper nickel electroplated layer 22 and also forms on the photoresist 18.

- 5 Referring to Figure 5, the photoresist 18 is removed using a liquid stripper, which is well known to those skilled in the art.

Referring to Figure 6, an etchant is used to etch the first and second blanket metal layers from the silicon substrate. The solder bump 24 forms a mask so that a portion of
10 blanket metal layers 14' and 16' remain beneath the solder bump 24 and the electroplated layers 20 and 22. Thus the solder bump 24, the electroplated layers 20 and 22 and the remaining part of the blanket layers 14' and 16' form a column of metals situated above and making layered contact with the metallic pad 11. Techniques for etching are well known in the art and include electrochemical etching, chemical etching
15 or a combination thereof.

Blanket flux may be applied to assist the solder in adhering to the sides of the blanket metal layers 10. Referring to Figure 7, the solder bump 24 may then be reflowed to form a solder ball 24'. The second electroplated nickel layer acts as a barrier between
20 tin in the solder 24 and the copper in the etched blanket layer 16' and the electroplated copper layer 20. The electroplated copper layer 20 in combination with the etched blanket layer 16' forms a thicker copper layer that is more resilient to attack from the tin in the solder. Clearly, electroplating additional copper to form an area of extra thick copper is more selective than producing a thicker layer by a sputtering process then
25 etching the majority of it away.

An alternative method of forming a solder bump on metallic pads in a semiconductor wafer is now described. Referring to Figure 8, the alternative method begins with depositing a blanket metal layer 14 of Cr or other suitable metals (as described
30 previously) onto a semiconductor wafer formed of the suitable material (as described previously), having at least one metallic pad formed therein (as described previously). A second blanket metal layer 16 is formed on the layer 14. Preferably, the layer 16 is

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sputtered copper, but may be other suitable metals as described above. The layers 14 and 16 form a plurality of blanket layers 10.

Referring to Figure 9, similar to that described in relation to Figure 2, photoresist material 18 is applied to the surface of the blanket metal layers 10 in accordance with the predetermined pattern with gaps 15 being provided above the metallic pads.

Referring to Figure 10, the first electroplated layer 20 is deposited on the blanket metal layers 10 as described above in relation to Figure 3. The first electroplated layer is formed of the same metal as the metal layer 16. Preferably the metal is copper.

Referring to Figure 11, the photoresist 18 is stripped away using a liquid stripper. This leaves the copper electroplated layer 20 on top of the copper blanket metal layer 16.

Referring to Figure 12, a second photoresist material 28 is spin coated on the blanket metal layers 10. It is exposed and developed to form the pattern required using standard lithographic techniques. A gap 17 in the photoresist material 28 is provided around the electroplated copper layer 20. The gap 17 is larger than the gap 15 so that the photoresist 28 is spaced from the electroplated copper layer 20. This will allow a second electroplated layer 26 to be electroplated so as to encapsulate the electroplated copper layer 20.

The second electroplated layer 26 is then applied as described before, but this time, as seen in Figure 13, the encapsulating electroplated layer 26 covers the electroplated copper 20. Again it is preferred that the second electroplated layer 26 be formed of nickel. Other suitable metals, as described above, may be used.

Referring to Figure 14, solder is then fabricated onto the electroplated layer 26 similarly to the process described in relation to Figure 4.

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Referring to Figure 15, the photoresist material 28 is removed using a liquid stripper as described above in relation to Figure 5.

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Referring to Figure 16, an etchant is applied to the blanket metal layers 10 so as to etch away the layers, apart from a remaining portion 14' and 16' masked by the solder bump 24. This process is conducted as described above in relation to Figure 6.

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Referring to Figure 17, blanket flux may be applied and the wafer sent to reflow the solder so as to release stress from the plated bump and allow the molten solder, through surface tension, to form a substantially spherical shape. As shown in Figure 17 the reflow bump is indicated by 24'. The wafer is then cleaned using di-ionised water or solvent. The process of reflowing is described above in relation to Figure 7.

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Referring to Figure 18, it is preferred that undercutting occurs during the wet chemical etching process to ensure cleanliness of the etching. In US 5,937,320 undercutting is used to relieve stress in the under-bump metallurgy. However, the electroplating of copper layer 20 is thought to relieve stress in the under-bump metallurgy as well as improve the mechanical strength of the bump. Undercut layers are indicated as 14'' and 16''. The solder bump 24 and the second electroplated layer 22 are not shown in Figure 18 for convenience.

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Referring to Figures 19, 20 and 21, alternative forms of the second electroplated layer 26, 26', 26'' are shown. In Figure 19 the layers 14', 16', 20 and 26 are as described in relation to Figure 16, with the solder bump 24 not shown for convenience. In Figure 20, the electroplated nickel 26' includes a flange 30. The flange 30 may be formed by a two-step application of photoresist and plating process. In Figure 21, the electroplated nickel 26'' encapsulates the electroplated copper 20 and the remaining sputtered copper 16'. This may be formed by a process of etching the copper blanket layer 16, applying another layer of photoresist and then the electroplated copper 26'', removing the other layer of photoresist and then etching the Cr blanket layer 14 so as to provide an undercut in the remaining Cr 14'' of the blanket layer.

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Referring to Figure 22, a solder bump 24 has been reflowed to form a solder ball 24' where the electroplated copper (indicated as 36) and the sputtered copper (indicated as

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16') are subject to the formation of intermetallics by contact with tin in the solder ball 24'. The nickel barrier layer 26''' is known to form a slower intermetallic that stops once a certain thickness has been reached. The tin nickel intermetallic is more uniform compared to a copper tin intermetallic. Due to the extra thickness of the copper, comprising sputtered copper 16' and electroplated copper 36, the solder bump is more resilient against the formation of intermetallics. With the addition of the encapsulating nickel barrier layer further protection is provided to the copper.

It will be clear to the skilled addressee that the present invention has at least the following advantages:

1. The encapsulating second electroplated barrier layers further reduces the amount of intermetallic;
2. Stress relief is addressed through the electroplated copper layer which also helps improve the mechanical strength of the bump; and
3. The electroplating of additional thickness to the terminal layer of the ball-limiting metallurgy is more selective than sputtering to an additional thickness.

Modifications and variations can be made to the present invention without departing from the basic inventive concept. Such modifications may include the use of other suitable metals in the various layers other than the preferred metals described herein or by the use of other suitable techniques in forming the respective metal layers. Such modification and variations are intended to be within the scope of the present invention, the nature of which is to be determined from the foregoing description.

Claims

1. A method of forming a solder bump on metallic pads in a semiconductor wafer, comprising the steps of:

5 depositing a plurality of blanket metal layers on a passivated surface of a semiconductor wafer having at least one metallic pad, the passivated surface including an opening above each metallic pad;

applying a photoresist material to the blanket metal layers;

patterning the photoresist material to provide a region for forming a plurality of metallic layers over each metallic pad;

10 electroplating a first electroplated metallic layer on the region;

electroplating a second electroplated metallic layer on the first electroplated metallic layer;

fabricating a solder bump on the second metallic layer;

removing the photoresist material; and

15 etching the plurality of blanket metal layers using the solder bump as a mask.

2. A method of forming a solder bump on metallic pads in a semiconductor wafer, comprising the steps of:

20 depositing a plurality of blanket metal layers on a passivated surface of a semiconductor wafer having at least one metallic pad, the passivated layer including an opening above each metallic pad;

applying a first photoresist material to provide a first region on the blanket metal layers;

25 patterning the photoresist material to provide the first region for forming a first electroplated metallic layer over each metallic pad;

electroplating the first electroplated metallic layer on the region;

removing the first photoresist material;

applying a second photoresist material to the blanket metal layers;

30 patterning the second photoresist material to provide a second region for forming a second electroplated metallic layer, the second photoresist material patterned so that the second electroplated metallic layer encapsulates the first electroplated metallic layer;

electroplating the second electroplated metallic layer so as to encapsulate the

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first electroplated metallic layer;

fabricating a solder bump on the second electroplated metallic layer;

removing the second photoresist material; and

etching the plurality of blanket metal layers using the solder bump as a mask.

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3. A method according to claims 1 or 2, wherein the first electroplated metallic layer is formed of the same metal as the uppermost layer of the plurality of blanket metal layers.

10 4. A method according to claims 1 or 2, wherein the first electroplated barrier layer and the uppermost layer of the plurality of blanket metal layers is formed of copper.

5. A method according to claims 1 or 2, wherein the second electroplated barrier layer is formed of nickel.

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6. A method according to claims 1 or 2, wherein the second electroplated barrier layer is formed of a nickel alloy.

20 7. A method according to claims 1 or 2, wherein the blanket metal layers include an adhesion layer that adheres to the underlying metallic pad.

8. A method according to claim 7, wherein the blanket metal layer includes a deposited layer on top of the adhesion layer.

25 9. A method according to claim 7, wherein the adhesion layer is formed of Ti/W, Cr or alloys thereof.

10. A method according to claim 8, wherein the deposited layer is formed of copper, nickel, gold or alloys thereof.

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11. A method according to claim 7, wherein the adhesion layer is formed by sputtering.

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12. A method according to claim 8, wherein the deposited layer is formed by sputtering.

13. A method according to claim 8, wherein the adhesion layer, deposited layer and the first electroplated layer form an under-bump metallurgy.

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14. A method according to claims 1 or 2, wherein the second electroplated layer forms a barrier layer to reduce the formation of intermetallics by interaction with tin in solder.

15. A method according to claim 14, wherein the nickel barrier layer is formed to a thickness of between 1 and 5 microns.

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16. A method according to claims 1 or 2, wherein the electroplated copper layer is plated to a thickness of between 1 and 10 microns.

15 17. A method according to claim 13, wherein the second electroplated layer encapsulates the deposited layer and the first electroplated layer, so that the solder bump does not make contact with these layers.

18. A method according to claims 1 or 2, wherein the solder is reflowed to form a substantially spherical solder ball.

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19. A method according to claims 1 or 2, wherein the semiconductor wafer is formed of silicon.

25 20. A method according to claims 1 or 2, wherein the metallic pads include aluminium.

21. A method according to claims 1 or 2, wherein the metallic pads include copper.

22. A method according to claims 1 or 2, wherein the etching of the barrier metal layers forms an under cut between the first electroplated layer and the semiconductor wafer.

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