

# SEMICONDUCTOR DEVICE WITH ELECTROSTATIC DISCHARGE PROTECTION

## Field of the Invention

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This invention relates to the protection of semiconductor devices against damage by high voltages. In the present application, the term semiconductor device includes all types of electronic devices based on semiconductor elements, including discrete components with only one, or a few, such elements and integrated circuits with many elements.

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## Background of the Invention

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Semiconductor devices are susceptible to damage if high voltages are applied to the device leads. Although careful circuit design may eliminate the possibility of damage during normal operation, the chance that a high voltage pulse may be applied to a device terminal, for example during handling of the device by an operator, cannot be completely excluded. Occurrences of this type are called electrostatic discharge (ESD) and may result in a potential of several thousand volts on a device lead for a short period, leading to damage or destruction of the affected circuits. Output circuits are particularly vulnerable to ESD pulses, and it is therefore necessary to provide ESD protection for such circuits.

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It is known to connect a resistor and/or diode between a lead of a semiconductor device and ground in order to bypass a vulnerable circuit element connected to the lead in the event of a high voltage pulse. However, although effective, this approach is inherently restricted for output circuits to low current, low frequency applications due to the presence of the resistor.

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Alternatively, a switch such as a transistor may be connected to a lead of a device to provide active switching of high voltage ESD pulses through the transistor rather than sensitive circuit elements. This approach, though, has not proven successful in protecting the output transistors of MOS circuits, in particular n-channel field effect (NMOS) transistors, which are susceptible to ESD damage caused either by excess current due to secondary breakdown, or by gate oxide rupture caused by the high voltage on the gate oxide. The

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problem is particularly acute for positive voltage pulses to ground (for negative pulses the parasitic pn diode is forward biased).

5 By increasing the size of the NMOS output transistor it is possible to increase the failure threshold with respect to secondary breakdown; however, this measure reduces the tolerance of the transistor to gate oxide rupture, as the larger transistor is slower to turn on when an ESD strikes, so that the charge in the ESD pulse is dissipated to ground more slowly and therefore the gate oxide is exposed to a high voltage for a longer period of time.

10 It is also known to use devices employing a thick gate oxide, which are inherently robust against oxide rupture. However, such devices have a low drive capability and are therefore slow to dissipate the charge in an ESD pulse. Moreover, this approach ignores the trend in semiconductor technology  
15 towards devices with thinner gate oxides. Such devices have a reduced resistance to gate oxide rupture and therefore require a more efficient protection against ESD pulses than has been possible in the prior art.

This invention therefore seeks to provide a semiconductor device having  
20 improved ESD protection that mitigates the above mentioned disadvantages and is also applicable to MOS output circuits.

### Summary of the Invention

25 According to the present invention there is provided a semiconductor device with electrostatic discharge protection comprising circuit means coupled to an external terminal of said device; a protective switch having a first current electrode coupled to said external terminal and a second current electrode  
30 coupled to a reference potential, said protective switch providing electrostatic discharge protection for said circuit means; characterised in that a control electrode of said protective switch is capacitively coupled to said external terminal.

35 In this manner, the protective switch rapidly responds to any high voltages applied to the external terminal of the semiconductor device, providing enhanced ESD protection.

In a preferred embodiment of the present invention, the first circuit means and the protective switch are n-channel field effect transistors. This combination has proved particularly effective in combating damage due to ESD pulses.

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In a further embodiment of the invention, the semiconductor device further comprises an RC network coupled to the control electrode of the protective switch. In this way the ESD protection may be tuned to a particular combination of circuit elements and ESD pulse type.

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### Brief Description of the Drawings

An exemplary embodiment of the invention will now be described with reference to the drawings in which:

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FIG.1 is a representation of the current signal from a high-voltage pulse through an NMOS output transistor with no ESD protection.

20 FIG.2 is a circuit diagram of a conventional output circuit incorporating ESD protection.

25 FIG.3 is a representation of the current signal from a high-voltage pulse: (i) through the output transistor and (ii) through the protective transistor of the circuit of FIG.2.

FIG.4 is a circuit diagram of an output circuit representing the preferred embodiment of the invention.

30 FIG.5 is a representation of the current signal from a high-voltage pulse: (i) through the output transistor and (ii) through the protective transistor of the circuit of FIG.4.

35 FIG.6 is a representation of the initial part of FIG.5, expanded along the time axis.

FIG.7 is a representation of the voltage level at the gate of the protective transistor in the circuit of FIG.4 during an ESD event.

FIG.8 is a representation of the integral of dissipated charge versus time: (i) for the output transistor and (ii) for the protective transistor of the circuit of FIG.4 during an ESD event.

#### Detailed Description of a Preferred Embodiment

10 The effect of a human body touching the lead of a semiconductor device may be simulated by a 4000V transient (HBM pulse) applied to the device. FIG.1 shows the current forced to flow through an unprotected NMOS output transistor by an HBM pulse; the result of this event would generally be the destruction of the transistor due to secondary breakdown or gate oxide  
15 rupture.

FIG.2 shows a conventional ESD protection circuit for circuit means, represented by an NMOS output transistor 2, the ESD protection being provided by a switch 1. In the example shown the switch is a protective NMOS  
20 transistor that is connected in parallel with the output transistor 2 and has the gate and source electrodes tied together. As may be seen from FIG.3, in which curve (i) represents the current through output transistor 2 and curve (ii) represents the current through protective transistor 1, this arrangement provides increased protection of the output transistor 2 against secondary  
25 breakdown, but not against gate rupture, as the protective NMOS does not turn on any faster than the output transistor 2 and will fail at the same voltage threshold; hence the output transistor 2 is still exposed to high gate voltages. Moreover, the protective NMOS transistor 1 increases the space requirements of the device significantly, because in order to avoid premature  
30 secondary breakdown the protective NMOS must have a size similar to that of the output transistor.

Referring to FIG.4, there is shown part of a semiconductor device having ESD protection in accordance with the invention. As in FIG.2, the principle of the  
35 invention is illustrated by showing an output stage of a semiconductor device in which protection against ESD events is provided by protective transistor 11. However, as will be clear to the skilled reader, the advantages of the

invention are not restricted to this example, but may include any suitable circuit element that is coupled to an external terminal and requires ESD protection, including thin and thick gate oxide MOS devices or bipolar devices.

5 Similarly, although in the preferred embodiment the protective switch is an NMOS transistor, the invention is not restricted to a particular type of transistor, but may encompass any suitable switching element incorporating MOS technology, either thick film or thin film. It is even envisaged to employ a thick-film capacitively coupled MOS transistor to provide ESD protection for a  
10 bipolar integrated circuit.

Moreover, the external terminal may be any external device terminal that is coupled to circuits that it is desired to protect against ESD damage, including either input or output terminals or even power supply terminals.

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As shown in the circuit of FIG.4, the protective transistor 11 is connected in parallel with output transistor 12, with the gate 13 of protective transistor 11 coupled to the output terminal 14 via a capacitive element 15.

20 During normal operation of the circuit, protective NMOS 11 is disabled; however, a positive ESD pulse will push a positive charge through the capacitive element 15 and turn this transistor on. The response of the protective NMOS 11 is faster than that of the output transistor 12 and therefore this semiconductor device in accordance with the invention has  
25 optimal ESD protection. FIG.5 shows in curve (i) the current through the output transistor and in curve (ii) the current through the protective transistor in the circuit of FIG.4 for a 4000V HBM ESD when the capacitive element 15 is selected to have a capacitance of about 10fF. It has been found that capacitance values of from about 1fF to about 1pF for element 15 result  
30 in a useful level of ESD protection; as the value of capacitance increases, the rapid turn-on effect of the protective switch is enhanced, but at the cost of reduced gate protection.

Although the inclusion of capacitive element 15 in FIG.4 is on its own  
35 sufficient to provide the desired fast turn on of transistor 13, an optional integrating and delaying RC network 16 may be coupled to the gate electrode 13 of the protective transistor 11 in order to optimise the response of the

protection circuit to the ESD pulse. In the circuit of FIG.4, a capacitance of 10fF and a resistance of 4k $\Omega$  in the RC network produced the response shown in FIG.5, although any capacitance value less than about 1pF was found to be suitable.

5 The ESD protection circuit of the present invention offers the following advantages:

- 10 a). By using capacitive gate coupling, the protective switch will be turned on very fast by the rising edge of the ESD pulse. The time for turn-on is found to be much faster than that of the output transistor or of a conventional protective transistor. The fast turn-on time is illustrated by FIG.6, which shows an expanded view of the first 20ns of the curves of FIG.5.
- 15 b) The response of the protective switch is proportional to the rise time of an ESD pulse; hence the faster the ESD pulse arrives, the faster the protection circuit will react.
- 20 c) The protective switch is protected from secondary breakdown due to excess current flowing, because it is turned off after the ESD pulse has reached its peak. Moreover, any desired delay in the action of this circuit can be pre-programmed by selecting the components of the RC network to optimise the response time of the protection circuit.
- 25 d) If the protective switch is an MOS transistor, the gate oxide is not liable to rupture during an ESD pulse, because the voltage levels appearing at this part of the circuit are only moderate. FIG.7 illustrates the evolution of the gate voltage of the protective NMOS of FIG.4 during a 4000V HBM ESD.

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The protective NMOS described in the present embodiment can be kept to a small size compared to the conventional protective transistor and therefore results in a reduction of the space required by the output circuit.

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The coupling capacitance necessary for the successful operation of the protection circuit is very small, of the order of 10fF, and may be realised either

by an overlapping area of metallisation layers, or metallisation and polysilicon layers. The values of R and C in the RC network may be selected to provide an even distribution of absorbed charge, and hence even power dissipation, between the output transistor 12 and the protective transistor 11 whilst  
5 permitting a compact circuit layout.

The ability to select the relative power dissipated in each transistor by the choice of R and C is a useful advantage of this embodiment of the present invention. This is because the power that a transistor can dissipate before it  
10 fails is directly proportional to the width of the transistor channel. In the example shown in FIG.5 the ratio of the area of the output transistor to the area of the protective transistor is 5:1, which compares with a ratio of dissipated power of the transistors of 4:1 illustrated in FIG.8 as the integral of the charge dissipated by each transistor over time (corresponding to the  
15 dissipated power).

Hence, although the peak currents through the output transistor and the protective transistor are comparable - as shown in FIG.5 - the power dissipated by each element can be predetermined by the choice of R and C in  
20 the RC network. This means that the protection circuit can be adapted to different circuit layouts and transistor sizes and may be applied to a wide range of devices, such as CMOS and MOS circuits.



Claims

1. A semiconductor device with electrostatic discharge protection  
5 comprising:  
    circuit means coupled to an external terminal of said device;  
    a protective switch having a first current electrode coupled to said  
external terminal and a second current electrode coupled to a reference  
potential, said protective switch providing electrostatic discharge protection  
10 for said circuit means;  
    characterised in that a control electrode of said protective switch is  
capacitively coupled to said external terminal.
2. A semiconductor device according to claim 1, wherein:  
15 said circuit means comprise an output transistor and said external  
terminal is an output terminal.
3. A semiconductor device according to claim 1 or 2, wherein:  
said circuit means and said protective switch are n-channel field effect  
20 transistors.
4. A semiconductor device according to any one of the preceding claims  
wherein:  
said control electrode of said protective switch is coupled to said external  
25 terminal by a capacitance of between about 1fF and about 1pF.
5. A semiconductor device according to any one of the preceding claims  
and further comprising:  
an RC network coupled to the control electrode of said protective switch.  
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6. A semiconductor device substantially as hereinbefore described with  
reference to FIGs.4-8.