

Title

METHOD FOR FABRICATING TRANSISTOR

5 Background of the Invention

1. Field of the Invention

The present invention relates generally to a method for fabricating semiconductor devices. More particularly, the present invention relates
10 to a method for fabricating a metal-oxide-semiconductor (MOS) transistor.

2. Description of the Prior Art

15 Fabrication of a transistor is known in the art. FIGS. 1–4 demonstrate a conventional method for fabricating a transistor. As shown in FIG. 1, a gate structure 100 is provided on a main surface of a semiconductor substrate 10. The gate structure 100 typically comprises a gate
electrode 102 such as polysilicon. A gate dielectric layer 104 is
20 interposed between the gate electrode 102 and the semiconductor substrate 10. A pair of sidewall spacers 105 is formed on two opposite sidewalls of the gate electrode 102. Prior to the formation of the pair of sidewall spacers 105, lightly doped drain (LDD) regions 112 may be
implanted into the semiconductor substrate 10 next to the side edges of
25 the gate electrode 102.

As shown in FIG. 2, using the gate electrode 102 and the spacer 105 as an implant mask, a source/drain ion implant is then carried out to
implant dopants into the unmasked regions of the semiconductor
30 substrate 10, thereby forming heavily doped source/drain regions 114.

As shown in FIGS. 3 and 4, after the source/drain ion implant, a conventional salicide block (SAB) process is performed. The SAB process includes conformally depositing a silicon oxide layer 122 overlying the
35 semiconductor substrate 10 and the gate structure 100, depositing a silicon nitride layer 124 overlying the silicon oxide layer 122, and selectively etching the silicon nitride layer 124 and the silicon oxide

layer 124 to form a SAB pattern 126, wherein the silicon oxide layer 122 acts as an etch stop layer. The SAB pattern 126 masks the regions where the silicide does not form. A silicide process is then performed to form silicide layer 130 on the unmasked regions of the semiconductor substrate 10 or gate structure 100.

In order to provide lower poly-gate resistance, higher energy and higher dose have been utilized during the source/drain ion implant. However, the high-energy ion implant may damage poly gate and the spacer, resulting in deteriorated device I_{off} performance, especially for NMOS transistors. Further, the high-energy ion implant may cause poly/gate channeling effect, resulting in threshold voltage (V_t) mismatch and channel leakage.

Summary of the Invention

One objective of the present invention is to provide a method for fabricating a metal-oxide-semiconductor (MOS) transistor that is capable of avoiding the above-mentioned prior art problems.

According to the claimed invention, in one aspect, a method for fabricating a transistor includes providing a gate structure on a main surface of a semiconductor substrate; lining the gate structure and the main surface of the semiconductor substrate with a screen layer; performing a source/drain ion implantation to implant dopants into the semiconductor substrate, thereby forming heavily doped source/drain regions; and performing a silicide block (SAB) process comprising depositing a silicon nitride layer overlying the screen layer, and selectively etching the silicon nitride layer and the screen layer to form a SAB pattern.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:

FIGS. 1–4 are schematic, cross-sectional diagrams showing a conventional method for fabricating a MOS transistor; and

FIGS. 5–9 are schematic, cross-sectional diagrams showing an exemplary method for fabricating a MOS transistor in accordance with one preferred embodiment of this invention.

It should be noted that all the Figures are diagrammatic. Relative dimensions and proportions of parts of the drawings have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings. The same reference signs are generally used to refer to corresponding or similar features in modified and different embodiments.

Detailed Description

The present invention has been particularly shown and described with respect to certain embodiments and specific features thereof. The embodiments set forth hereinbelow are to be taken as illustrative rather than limiting. It should be readily apparent to those of ordinary skill in the art that various changes and modifications in form and detail may be made without departing from the spirit and scope of the invention.

FIGS. 5–9 are schematic, cross-sectional diagrams showing an exemplary method for fabricating a metal–oxide–semiconductor (MOS) transistor in accordance with one embodiment of this invention, wherein like numeral numbers designate like regions, layers or elements. As shown in FIG. 5, a semiconductor substrate 10 is provided. The semiconductor substrate 10 may include but not limited to silicon substrate, silicon substrate with an epitaxial layer, SiGe substrate, silicon–on–insulator (SOI) substrate, gallium arsenide (GaAs) substrate,

gallium arsenide-phosphide (GaAsP) substrate, indium phosphide (InP) substrate, gallium aluminum arsenic (GaAlAs) substrate, or indium gallium phosphide (InGaP) substrate. Optionally, an ion well (not explicitly shown) such as N well or P well may be formed in the semiconductor substrate 10 in some cases. For example, a PMOS transistor device is typically fabricated in an N well.

A gate structure 100 is provided on a main surface 10a of a semiconductor substrate 10. The gate structure 100 may comprise a gate electrode 102 such as polysilicon. A gate dielectric layer 104 is interposed between the gate electrode 102 and the semiconductor substrate 10. A pair of sidewall spacers 105 is formed on two opposite sidewalls of the gate electrode 102. The gate electrode 102 may include but not limited to polysilicon, metal, composite metal or silicide. A cap layer (not explicitly shown) such as silicon nitride cap may be provided as a part of the gate electrode 102 in some embodiments. It is understood that although not explicitly shown in the figures, liners, offset spacers or "first spacers" may be formed on the sidewalls of the gate electrode 102 along with the sidewall spacers 105 that are normally referred to as the "second spacers" or "spacer-2". The gate dielectric layer 104 may comprise silicon dioxide or high-k material. Prior to the formation of the pair of sidewall spacers 105, lightly doped drain (LDD) regions 112 may be implanted into the semiconductor substrate 10 next to the side edges of the gate electrode 102.

As shown in FIG. 6, subsequently, a screen layer 222 such as silicon oxide is conformally deposited over the semiconductor substrate 10 and the gate structure 100. In other embodiments, the screen layer 222 may be made of other dielectric materials. According to the embodiment of the invention, the screen layer 222 may have a deposited thickness t_1 that is greater than 100 angstroms, preferably about 150 angstroms. According to the embodiment of the invention, the screen layer 222 may be formed by chemical vapor deposition (CVD), atomic layer deposition (ALD) or any suitable methods known in the art.

As shown in FIG. 7, using the gate electrode 102 and the spacer 105 as an implant mask, a source/drain ion implant is then carried out to

implant dopants into the semiconductor substrate 10, thereby forming heavily doped source/drain regions 114. The source/drain ion implant may be performed with high energy and high dose. During the ion implantation of the heavily doped source/drain regions 114, the presence of the screen layer 222 alleviates the poly/gate channeling effect and avoids damages to the gate electrode 102 or sidewall spacers 105. Accordingly, the device performance such as I_{off} is significantly improved.

As shown in FIGS. 8–9, after the source/drain ion implant, a photoresist stripping process and/or RCA cleaning process may be performed to clean or remove unwanted substances from the main surface 10a of the semiconductor substrate 10. During the RCA cleaning process, an upper portion of the screen layer 222 is also removed. Preferably, the remaining thickness or post-clean thickness t_2 of the screen layer 222 may range between 40–100 angstroms. Thereafter, a salicide block (SAB) process is performed. According to the embodiment of the invention, the SAB process includes conformally depositing a silicon nitride layer 124 overlying the screen layer 222, and selectively etching the silicon nitride layer 224 and the screen layer 222 to form a SAB pattern 226, wherein the screen layer 222 acts as an etch stop layer during the SAB process. The SAB pattern 226 masks the regions where the silicide does not form. A salicide process is then performed to form silicide layer 130 on the unmasked regions of the semiconductor substrate 10 or gate structure 100.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention.

Claims

What is claimed is:

- 5 1. A method for fabricating a transistor, comprising:
providing a gate structure on a main surface of a semiconductor
substrate;
lining the gate structure and the main surface of the semiconductor
substrate with a screen layer;
10 performing a source/drain ion implantation to implant dopants into
the semiconductor substrate, thereby forming heavily doped
source/drain regions; and
performing a salicide block (SAB) process comprising depositing a
silicon nitride layer overlying the screen layer, and selectively etching
15 the silicon nitride layer and the screen layer to form a SAB pattern.
2. The method for fabricating a transistor according to claim 1
wherein the screen layer comprises silicon oxide.
- 20 3. The method for fabricating a transistor according to claim 1
wherein the screen layer has a deposited thickness that is greater than
100 angstroms.
4. The method for fabricating a transistor according to claim 1
25 wherein after performing the source/drain ion implantation, the method
further comprises performing a photoresist stripping process and/or
RCA cleaning process.
5. The method for fabricating a transistor according to claim 4
30 wherein during the RCA cleaning process, an upper portion of the
screen layer is removed.
6. The method for fabricating a transistor according to claim 5
wherein a post-clean thickness of the screen layer ranges between
35 40–100 angstroms.
7. The method for fabricating a transistor according to claim 1

wherein the screen layer acts as an etch stop layer during the SAB process.

5 8. The method for fabricating a transistor according to claim 1 wherein after the SAB process, a salicide process is performed to form silicide layer on unmasked regions of the semiconductor substrate.

10 9. The method for fabricating a transistor according to claim 1 wherein the gate structure 100 comprises a gate electrode.

10. The method for fabricating a transistor according to claim 9 wherein the gate electrode comprises polysilicon.

15 11. The method for fabricating a transistor according to claim 9 wherein a gate dielectric layer is interposed between the gate electrode and the semiconductor substrate.

20 12. The method for fabricating a transistor according to claim 9 wherein a pair of sidewall spacers is formed on two opposite sidewalls of the gate electrode.