METHOD AND APPARATUS UTILIZING FIELD RATIOING DEMODULATION TECHNIQUES FOR A NULL-TYPE SERVO PATTERN

FIELD OF THE INVENTION

The present invention relates to storage devices. In particular, the present invention relates to servo systems in storage devices.

BACKGROUND OF THE INVENTION

A storage device, such as a disc drive, typically uses a servo system to position a read or write head over a recording track were digital information is stored. The servo system relies on servo information stored either on a dedicated disc surface in a multidisc system or in servo sectors that are radialy dispersed throughout each disc. The servo information gives coarse position information such as the track number of the track that the head is positioned over and possibly the angular sector that the head is positioned over. The servo information also includes fine position information that describes the radial location of the head within a track.

The fine position information is generally stored using a servo field pattern that is a combination of several servo fields. There are several types of servo field patterns, including "null-type" servo patterns, "split-burst amplitude" servo patterns, and "phase type " servo patterns.

A null-type servo pattern includes at least two fields, which are written at a known phase relation to one another. The first field is a "Phase" or "Sync" field, which is used to lock the phase and frequency of the read channel to the phase and frequency of the read signal. The

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field, and this phase information is used for demodulating the position error field signal. The phase field must therefore be sufficiently long to enable the PLL to lock on to the phase and frequency of the read signal. For example, the phase field may be 3 to 4 times longer than the position error field.

Ensuring a consistent phase relationship between the phase field and the position error field in each servo sector of a disc is critical to accurate positioning of the head. If the phase between these two fields is not consistent at each servo field, a different position error value will be obtained at two different servo fields even though the head remains in the same radial position within the track. To insure this consistency, great effort and expense has been expended toward building consistent phase locked loops that operate the same in every servo field.

The position error value generated by the servo system ideally changes linearly as the head moves radially across the track. Such linear changes simplify the calculations needed to determine the amount by which the head must be moved to bring it to a desired location. In general, servo systems do not produce position error values that change linearly as the head moves radially across a track. In particular, as a head moves radially across a track, the read signal generated by the read head tends to fluctuate due to the geometry of the head. To reduce the effects of such fluctuations, the prior art has used automatic gain control systems to automatically adjust the gain of the servo loop so that it remains constant at all track positions for the head. The amount of gain that must be introduced by the automatic gain control is set by a control circuit that must be initialized either at disc burn-in or periodically during the life of the disc drive.

FIG. 8 is a block diagram of a digital demodulator of the prior art.

FIG. 9 is a pattern layout of a servo pattern of the present invention.

FIG. 10 is a read signal generated by a read head as it passes over the servo pattern of FIG. 9.

FIG. 11 is a read signal generated by a read head as it passes over the servo pattern of FIG. 9.

FIG. 12 is a read signal generated by a read head as it passes over the servo pattern of FIG. 9.

FIGS. 13-1 through 13-5 are signal diagrams of signals associated with a digital demodulator of the present invention.

FIG. 14 is a block diagram of a digital demodulator of the present invention.

FIGS. 15-1 through 15-2 are timing diagrams showing the relationship between rectification values and a read signal for one embodiment of the invention.

FIGS. 16-1 through 16-2 are timing diagrams showing the relationship between rectification values and a read signal for a second embodiment of the invention.

FIG. 17 is a block diagram of an analog demodulator of the present invention.

FIGS. 18-1 through 18-11 are timing diagrams showing signals associated with the block diagram of FIG. 17.

FIG. 19 is a block diagram of an analog division circuit used in FIG. 17.

of operation (read, write, or track seek). In addition, microprocessor 233 provides write data along data bus 237 and receives read data along a data bus. The recovered data is provided to the host through host interface 234.

Microprocessor 233 controls the movement of head 112 over the disc through servo logic 232, which is connected to microprocessor 233 through an address bus 241 and a bi-directional data bus 243. Using address bus 241 and data bus 243, microprocessor 233 is able to store a desired location for the head in a memory location within servo logic 232. This memory location is accessed by servo logic 232, which issues a current command 236 to plant 230 based upon the stored value and the current position of the head. Microprocessor 233 is also able to retrieve head position information stored in servo logic 232's memory locations using address bus 241 and data bus 243.

Within plant 230, current command 236 is received by power amplifier 238, which converts the voltage of current command 236 into a current signal 240. Current signal 240 is provided to and controls an actuator 242, which includes voice coil motor 134 of FIG. 1 that is driven by, and accelerates at a rate determined by, the current of current signal 240. Actuator 242 translates the current of current signal 240 into mechanical movement 244, which moves head 112 relative to the medium.

Head 112 detects data and servo patterns embedded within the medium as it moves relative to the medium. The servo patterns contain information about the position of the head relative to the medium and cause the head to produce a low-level signal 248 that contains encoded position information. A head amplifier 250 amplifies the low-level signal 248 to produce amplified signal 252, which is less susceptible to noise and which is easier to decode. Amplified signal 252 is input to demodulator

The servo loop described above has a frequency dependent response to irregularities in the track in the sense that its ability to respond to irregularities in the track decreases as the frequencies of those irregularities increases. In this sense, the irregularities of the track can by thought of as an input signal to the servo loop and the servo loop's response to those irregularities can be thought of as the gain of the servo loop. For certain types of head 112, specifically magnetoresistive heads, the frequency response of the servo loop changes as the position of head 112 changes within a track. Thus, the head will respond faster to track irregularities in different parts of a track.

FIG. 3 is a diagram showing the essential portions of a null-type servo magnetization pattern for a servo section 180 used in the prior art. The radial dimension of disc 122 is shown vertically, and the angular dimension of disc 122 is shown horizontally. Arrow 182 indicates a down-track direction, or angular dimension, of disc 122. Arrow 184 indicates a cross-track direction, or radial dimension, of disc 122. FIG. 2 shows four track centers 190, 191, 192 and 193, which are labeled "1", "2", "3" and "4", respectively. Head 134 is aligned with track center "2" along cross-track direction 184.

The shaded regions in FIG. 3 correspond to regions of opposite magnetic polarity as compared to the non-shaded regions. For example, in a longitudinal recording system, if the longitudinal magnetization in the non-shaded regions were right to left in the figure, then the longitudinal magnetization in the shaded regions would be left to right. Within these regions, the magnetic medium is saturated in either longitudinal direction, as is standard practice in digital magnetic recording.

read signal 210, normal position error field signal 212 is substantially zeroed.

FIG. 5 is a waveform diagram showing a portion of a read signal 216 when head 134 is halfway between centerlines 190 and 191 of tracks 1 and 2, respectively. Read signal 216 can be divided into phase field signal 218, normal position error field signal 220, and quadrature position error field signal 222, which are created by head 134 as it passes over phase field 202, normal position error field 205 and quadrature position error field 206, respectively. FIG. 6 is a waveform diagram showing a portion of a read signal 224 when head 134 is half-way between centerlines 191 and 192 of tracks 2 and 3, respectively. Read signal 224 can be divided into phase field signal 226, normal position error field signal 228 and quadrature position error field signal 230. Note that normal position error field signal 220 in FIG. 5 is 180° out of phase from normal position error field signal 228 in FIG. 6.

FIG. 7 is a block diagram of a demodulator 300 that represents one embodiment of demodulator 254 of FIG. 2 of the prior art. Demodulator 300 receives amplified signal 252 at an input to an automatic gain control 302. Automatic gain control 302 is part of a feedback loop that includes a summing circuit 304, which is connected to the output of automatic gain control 302. Summing circuit 304 also receives a reference value 306 created by servo logic 232 of FIG. 2. Reference value 306 is calculated by servo logic 232 to ensure that the gain of the servo loop remains constant at all track locations. Summing circuit 304 subtracts the reference value 306 from the magnitude of the output of automatic gain control 302 to produce a feedback value 308 that is fed back to automatic gain control 302. Based on feedback value

After the normal position error signal, the next signal on gain control output 310 is the quadrature position error signal. The quadrature position error signal is also provided to multiplier 318, which multiplies the quadrature signal by clock signal 316 to produce product signal 320. Product signal 320 is then integrated by integrator 322 to produce a quadrature position error value at the output of integrator 322. The quadrature position error value is then routed by multiplexer 323 to output 328. The quadrature position error value on output 328 and the normal position error value on output 326 are then used to calculate the position of the head within the track. Such calculations are well known in the art.

FIG. 8 is a block diagram of a digital demodulator 350, which is one embodiment of a prior art demodulator 254 of FIG. 2. Amplified signal 252 of FIG. 2 is provided to automatic gain control 352, which operates in a manner similar to automatic gain control 302 of FIG. 7. Gain control output 354 of automatic gain control 352 is provided to a summer 356 which subtracts a reference value 358 from the magnitude of gain control output 354 to provide a feedback value 360. Based on feedback value 360, automatic gain control 352 applies the proper gain to amplified signal 352. Gain control output 354 is also provided to a phase locked loop 362, which generates a clock signal 364 based on the phase field portion of the read signal. The sign of the clock signal is determined by a signum circuit 366, which provides a digital value representative of the sign of clock signal 364.

The clock signal generated by phase locked loop 362 continues even after the phase field portion of gain control output 354 ends and the normal position error signal and quadrature position error

FIG. 9 is a pattern layout for a servo region 400 used in the present invention. In FIG. 9, the cross track direction is shown vertically and the down track direction is shown horizontally with a head 134 moving from left to right across the figure. Servo region 400 includes leading field 402, phase field 404, middle field 406, normal position error field 408, quadrature position error field 410 and trailing field 412. Leading field 402, middle field 406, and trailing field 412 are identical to the same named fields in the servo region of the prior art shown in FIG. 3. Phase field 404 in FIG. 9 is similar to phase field 202 in FIG. 3, except that, in general, phase field 404 has fewer transitions then phase field 202 of the prior art. Phase field 404 is shorter than phase field 202 because the present invention does not need the accurate phase locked loop that is found in the prior art and thus does not require as many transitions in the phase field as the prior art. Normal position error field 408 and quadrature position error field 410 are similar to prior art normal and quadrature position error fields 205 and 206, respectively, with the exception that normal position error field 408 and quadrature position error field 410 both include a set of radially coherent transitions 414 and 416 near the beginning of the respective fields. Radially coherent transitions 414 and 416 are similar to the transitions found in phase field 404. The use of these transitions is discussed further below.

FIGS. 10, 11, and 12 are timing diagrams of example read signals 450, 452, and 454, respectively, which are produced by head 134 as it passes through servo region 400 of FIG. 9 at different track locations. In particular, servo read signal 452 of FIG. 11 is produced as head 134 passes along the centerline of track 418 of FIG. 9. Read signal 452 can be divided into three regions consisting of a phase field signal 456, a normal

Read signal 454 of FIG. 12 is generated when head 134 is positioned half-way between track centers 418 and 422 of FIG. 9. Read signal 454 may be divided into three separate portions including a phase field signal 490, a normal position error signal 492, and a quadrature position error signal 494. Normal position error signal 492 may be further divided into a trigger oscillation portion 496 and a null pattern portion 498. Similarly, quadrature position error signal 494 may be divided into a trigger oscillation portion 500 and a null pattern portion 502.

Since both read signal 454 and read signal 450 are generated when head 134 is positioned half-way between respective track center lines, they have common features. For example, null pattern portions 482 and 502 of read signals 450 and 454, respectively, are both substantially equal to zero. In addition, null pattern portions 478 and 498 of read signals 450 and 454, respectively, have maximum amplitudes. Read signals 450 and 454 are not identical, because null pattern portion 478 is 180 degrees out of phase with null pattern portion 498. This is similar to the phase shift found in null type patterns of the prior art. Read signals 450 and 454 differ from the prior art in that trigger oscillation portions 476 and 496 are the same in normal position error signal 472 and normal position error signal 492 even though the null pattern portions are shifted 180 degrees out of phase from each other. In fact, the trigger oscillation portion of any normal position error field signal generated from servo region 400 of FIG. 9 is the same. Similarly the trigger oscillation portion found in a quadrature position error signal of the present invention would be the same at all head locations in servo

Triggered oscillator 526 generates sample clock signal 528 based on control signals from a sequencer 534. Sequencer 534 includes a zero phase restart circuit, that is commonly known in the art, which uses portions of read signal 522 to generate an enable voltage controlled oscillator (VCO) signal 536 of FIG. 13-3 and a start voltage controlled oscillator (VCO) signal 538 of FIG. 13-4. To generate enable VCO signal 536 and start VCO signal 538, sequencer 534 uses the respective transitions located at the beginning of the phase field, the normal position error field, and the quadrature position error field of the servo region. Thus, referring to FIG. 9, sequencer 534 uses the first four transitions associated with phase field 404, and radially coherent transitions 414 and 416 of normal position error field 408 and quadrature position error field 410, respectively. Sequencer 534 insures that triggered oscillator 526 starts at a consistent phase relationship in each of the fields of servo region 400. To insure this phase relationship, sequencer 534 disables triggered oscillator 526 at the end of each field and re-enables triggered oscillator 526 at the beginning of each field.

Sample clock signal 528 is also provided to a rectification value generator 540 of Fig. 14, which produces a rectification value with each positive going transition in sample clock signal 528. The rectification values produced by rectification value generator 540 are provided to a multiplier 542, which also receives the digital values produced by analog-to-digital converter 524. Multiplier 542 multiplies the rectification values by the sampled data values to produce a series of product values 544 that are input to a summing circuit 546. Together, rectification value generator 540 and multiplier 542 rectify the values produced by analog-to-digital converter 524. This rectification can

present invention since these low magnitude values can often be corrupted by noise. By suppressing them, the noise associated with these low magnitude values is also suppressed.

FIGS. 16-1 and 16-2 show a second embodiment of the invention where the rectification values are used to suppress undesirable samples taken from a read signal 620. Read signal 620 has peaks such as peaks 622 and 624 as well as shoulders 626 and 628. Shoulders 626 and 628 represent non-ideal portions of read signal 620. Thus, samples taken from shoulders 626 and 628 do not accurately represent the transitions stored in the medium. Under the embodiment of the invention shown in FIGS. 16-1 and 16-2, rectification values of zero are used to suppress samples taken from the shoulders. Thus, the samples associated with shoulders 626 and 628 are multiplied by rectification values of zero. The remaining rectification values are chosen to rectify the samples taken from the peaks. Thus, samples having negatives values are multiplied by negative one and samples having positive values are multiplied by positive one.

Those skilled in the art will recognize that the embodiments shown in FIGS. 15-1, 15-2, 16-1, and 16-2 are only examples of possible embodiments for the rectification values. Other sequences of rectification values are possible and are considered within the scope of the present invention.

Returning to FIG. 14, summing circuit 546 sums together a series of product values 544 for each of the fields in the servo region. Specifically, summing circuit 546 sums values for phase field 404, normal position error field 408, and quadrature position error field 410. In most embodiments, the time period over which the sum is taken is the same

ratioing that divides the sum associated with the normal position error field and the sum associated with the quadrature position error field by the sum associated with the phase field. By dividing each of the position error field sums by the phase field sum, the present invention normalizes these sums and eliminates gain factors that are common to all three fields. The division of the normal position error field sum by the phase field sum is performed by a division circuit 566 to produce a first position error signal estimate. The division of the quadrature position error field sum by the phase field sum is performed by a division circuit 568 to produce a second position error signal estimate. The first and second position error signal estimates are then combined using known techniques to determine the location of the head within the track.

The normalization performed by the demodulator of the present invention shown in FIG. 14 removes certain errors in the position error sample that would otherwise arise due to the demodulation hardware. To show this, the sampled read data produced by analog-to-digital converter 524 can be defined as:

$$y^*(t) = Y(t) \cdot \delta(t - nT_S) \qquad \text{EQ. 1}$$

where y*(t) is the sampled read data, Y(t) is the amplified signal received by analog-to-digital converter 524, t is time, δ is an impulse function, n is the number of this sample, and (T_S) is the sample clock period.

The steps of multiplying the samples by a rectification value and summing the product can be represented by:

$$S_x = \sum_{n=1}^{N} Y(t) \cdot \delta(t - nT_S) \cdot R_n \qquad \text{EQ. 2}$$

where S_x is the sum produced by summing circuit 546 of Fig. 14, R_n is the rectification value associated with the nth sample, and N is the number

$$PES1 = \frac{A_{nPEF}}{A_{PF}} \qquad \text{EQ. 7}$$

Similiarly, the division performed by division circuit 568 can be represented by:

$$PES2 = \frac{\sum_{n=1}^{N} A_{qPEF} f(t) \cdot \delta(t - nT_S) \cdot R_n}{\sum_{n=1}^{N} A_{PF} f(t) \cdot \delta(t - nT_S) \cdot R_n} \qquad \text{EQ. 8}$$

where PES2 represents the second position error signal produced by division circuit 568. Using the assumptions described above, equation 8 can also be simplified to:

$$PES2 = \frac{A_{qPEF}}{A_{PF}} \qquad \text{EQ. 9}$$

Equations 7 and 9 show that any errors that consistently appear in f(t) are removed by the divisions performed at division circuits 566 and 568. In addition, since the sampling period T_s is cancelled out in Equations 7 and 9 if the sampling period is the same in each field of a servo region, it can be seen that the sampling period does not need to be the same for each servo region as long as the sampling period is consistent in all of the fields within a single servo region. Thus, a highly accurate phase locked loop is not needed since the sampling clock does not need to be the same at each servo region. Instead, a consistent triggered oscillator can be used as shown in FIG. 14. It should also be noted that R_n can have any values as long as R_n is consistent in all three fields in the servo region. Thus, the values of R_n can be chosen to eliminate noisy samples without impacting the position error signal estimate. In addition, different R_n values can be used at different servo regions to maximize the performance of the demodulator.

signals on amplified signal 252, an example of which is shown in the timing diagram of FIG. 18-1. Two of the signals generated by sequencer 702 are an enable voltage controlled oscillator (VCO) signal 704 shown in the timing diagram of FIG. 18-3 and a start voltage controlled oscillator (VCO) 706 shown in the timing diagram of FIG. 18-4. Enable (VCO) signal 704 is provided to a triggered oscillator 708, which produces a multiplier clock signal 710 shown in FIG. 18-2. Triggered oscillator 708 also receives start VCO 706 from sequencer 702. With enable VCO 704 high, triggered oscillator 708 will begin to produce multiplier clock signal 710 after start VCO 706 goes high. Triggered oscillator 708 will continue to produce multiplier clock signal 710 until enable VCO signal 704 returns to low. In most embodiments of the invention, multiplier clock signal 710 is a square-wave clock signal oscillating between negative one and positive one.

Through enable VCO signal 704 and start VCO signal 706, sequencer 702 restarts clock signal 710 at each field in the servo region. Specifically, clock signal 710 is restarted each time the head enters a phase field, a normal position error field, and a quadrature position error field. Sequencer 702 generates enable VCO 704 and start VCO 706 based on the first sets of transitions in each field. In particular, sequencer 702 uses the first sets of transistions in the phase field, and the sets of transitions associated with the oscillation trigger portions of the normal position error field and the quadrature position error field such as oscillation trigger portions 414 and 416 of FIG. 9. Since sequencer 702 uses radially coherent transitions to start triggered oscillator 708, the clock signal produced by triggered oscillator 708 will have the same

the phase field is the same as the period of integration for the normal position error field and the quadrature position error field.

After each integration, integrator 716 produces an analog value resulting in a sequence of integrands 720 at its output. The first integrand in the sequence of integrands 720 is a phase field integrand, which is directed by a multiplexer 722 to an analog phase field sample-and-hold circuit 724. Multiplexer 722 directs the integrand to phase field sample and hold circuit 724 based on a multiplexer control signal 726 shown in FIG. 18-6. Multiplexer control signal 726 is high during the period of time when integrator 716 is producing the integrand for the phase field and is low during the periods of time when integrator 716 is producing integrands for the normal position error field and the quadrature position error field.

Phase field sample-and-hold circuit 724 receives a phase load signal 728 and a phase reset signal 730 from sequencer 702. Examples of phase load signal 728 and phase reset signal 730 are shown in FIGS. 18-9 and 18-10, respectively. Phase reset signal 730 resets phase field sample-and-hold circuit 724 just before the phase integrand is produced by integrator 716. Phase load signal 728 places phase field sample-and-hold circuit 724 in a state to receive the phase integrand from multiplexer 722 just after integrator 716 produces the phase integrand. This is shown in FIGS. 18-9 and 18-5 where phase load signal 728 goes high just as enable integrator signal 718 goes low for the phase field. Once the phase field integrand has been loaded into phase field sample-and-hold circuit 724, phase field sample-and-hold circuit 724 produces the phase integrand at its output 732 until it is reset.

quadrature position error field integrand by the phase field integrand to produce a second position error field estimate that is provided to analog-to-digital converter 746. The second position error signal estimate is converted by analog-to-digital converter 746 into a digital second position error signal estimate. As in the digital version of the present invention, the division of the normal position error signal integrand and the quadrature position error signal integrand by the phase field integrand eliminates common errors introduced by the servo system into each integrand. This allows for the elimination of the AGC circuit and the phase locked loop under the present invention.

FIG. 19 shows one embodiment of division circuit 742 of FIG. 17. In FIG. 19, the output 740 of position error signal sample-and-hold circuit 734 is provided to the inverting input of an operational amplifier 750. The output of operational amplifier 750 is fed to a multiplier 752, which also receives output 732 of phase field sample-and-hold circuit 724. The output of multiplier 752 is provided to the non-inventing input of amplifier 750.

Although the description of analog demodulator 700 found above shows that the analog values are not converted into digital values until after the position error field integrand has been divided by the phase field integrand, in other embodiments, the integrands may be converted into digital values at any point after integrator 716.

In summary, the present invention provides a method of determining a location of a read head 110 over a storage medium 106 based on a servo signal 522 generated by the read head 110 as the read head 110 passes over a phase field 404 and a position error field 408, 410. The method includes performing a demodulating set of operations 542,

712 for rectifying a phase field signal 456, 470, 490 and a position error field signal 458, 460, 472, 474, 492, 494 to produce a rectified phase field signal and a rectified position error field signal. The demodulation circuit also includes a summing circuit 546, 716 coupled to the rectification circuit and capable of summing values of the rectified phase field signal over time to produce a normalization factor 732 and capable of summing the values of the position error field signal over time to produce an unscaled position error field value. A division circuit 566, 568, 742 is capable of receiving the normalization factor 732 and the unscaled position error field value and is capable of dividing the unscaled position error field value by the normalization value to produce a position error signal value 744.

Although the present invention has been described with reference to eliminating the phase locked loop and automatic gain control, those skilled in the art will recognize that the present invention may be practiced in a disc drive that retains a phase locked loop and an automatic gain control.

It is to be understood that even though numerous characteristics and advantages of various embodiments of the present invention have been set forth in the foregoing description, together with details of the structure and function of various embodiments of the invention, this disclosure is illustrative only, and changes may be made in details, especially in matters of structure and arrangement of parts within the principles of the present invention to the full extent indicated by the broad general meaning of the terms in which the appended claims are expressed. For example, demodulation of the phase and position error fields can be performed sequentially with the same circuitry or can

WHAT IS CLAIMED IS:

1. A method of determining a location of a read head over a storage medium in a storage device based on a servo signal generated by the read head as the read head passes over a phase field and a position error field on the storage medium, the method comprising steps of:

(a) performing a demodulating set of operations on a portion of the servo signal associated with the phase field to produce a phase field value;

(b) performing the demodulating set of operations on a portion of the servo signal associated with the position error field to produce a position error field value; and

(c) dividing the position error field value by the phase field value to produce a position error estimate indicative of the location of the read head over the storage medium.

2. The method of claim 1 wherein the read head passes over a second position error field and the method further comprises steps of:

(d) performing the demodulating set of operations on a portion of the servo signal associated with the second position error field to produce a second position error field value; and

(e) dividing the second position error field value by the phase field value to produce a second position error estimate indicative of the location of the read head over the storage medium.

9. A demodulation circuit for demodulating a servo signal in a data storage device to produce a position error signal value, the servo signal comprising a phase field signal and a position error field signal, the demodulation circuit comprising:

a rectification circuit capable of receiving and at least partially rectifying the phase field signal and the position error field signal to produce a rectified phase field signal and a rectified position error field signal;

a summing circuit coupled to the rectification circuit and capable of summing values of the rectified phase field signal over time to produce a normalization factor and capable of summing values of the position error field signal over time to produce an unscaled position error field value; and

a division circuit capable of receiving the normalization factor and the unscaled position error field value and of dividing the unscaled position error field value by the normalization factor to produce a position error signal value.

10. The demodulation circuit of claim 9 wherein the summing circuit comprises an analog integrator.