

Fig.1

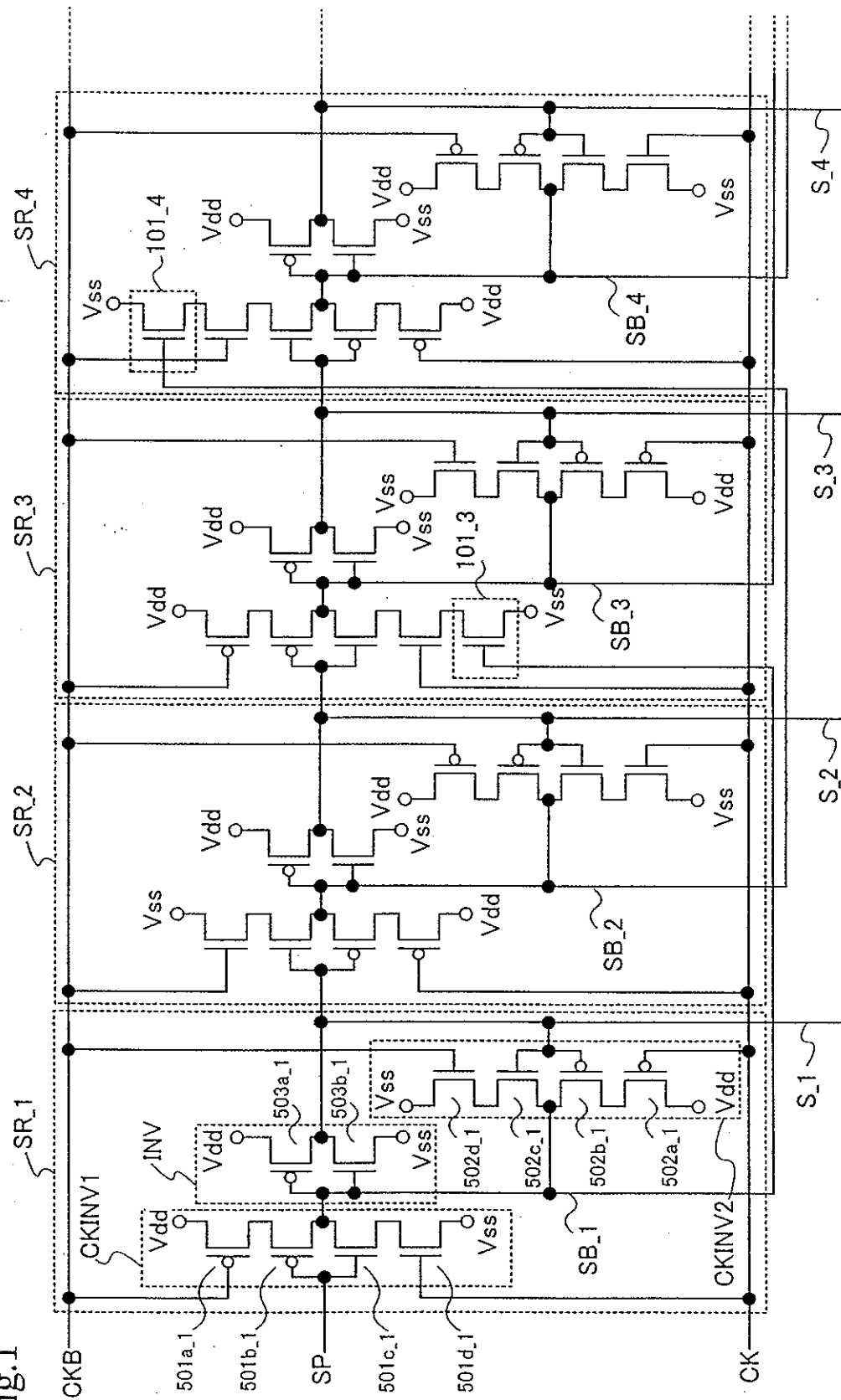


Fig.2

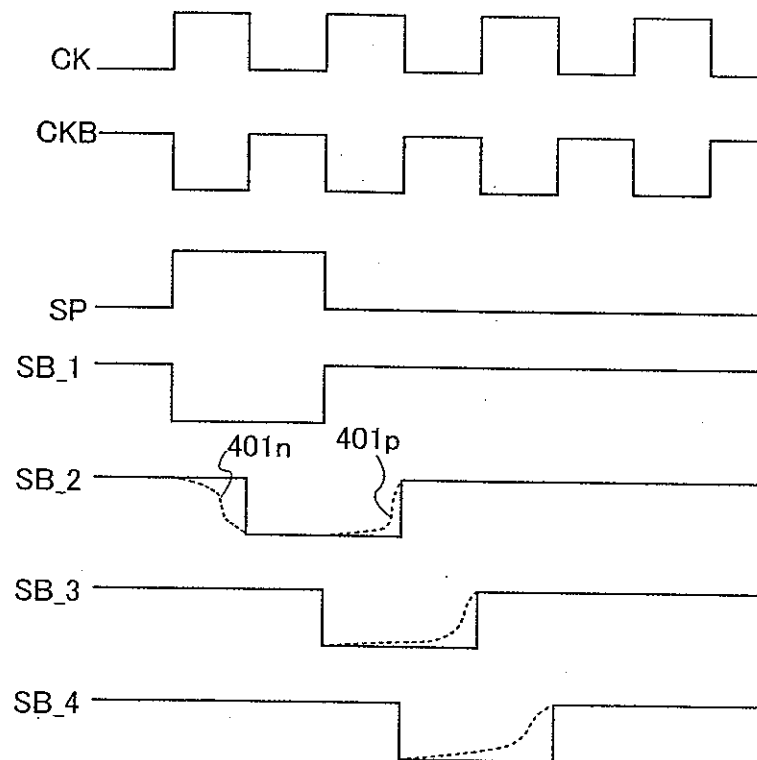


Fig.3

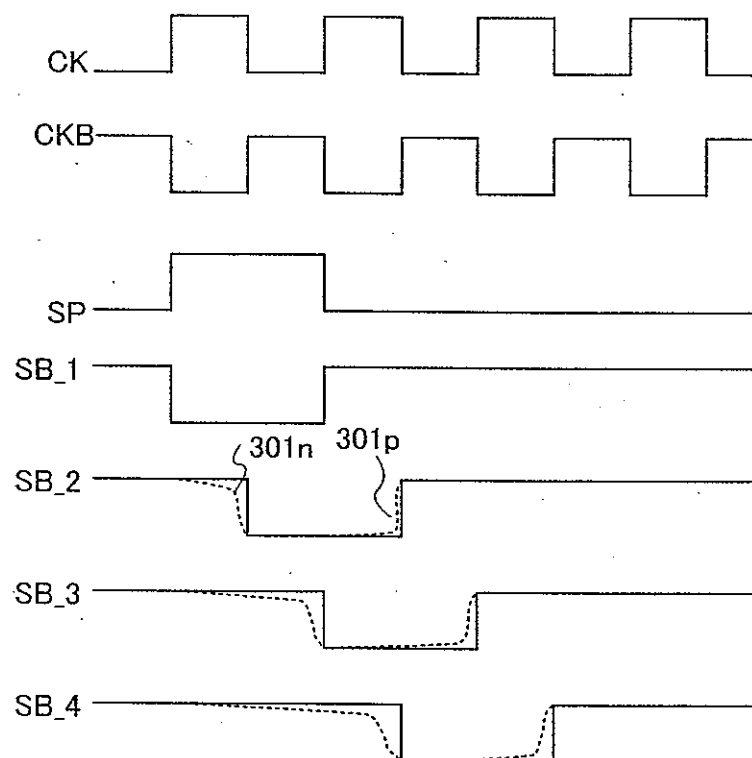


Fig.4

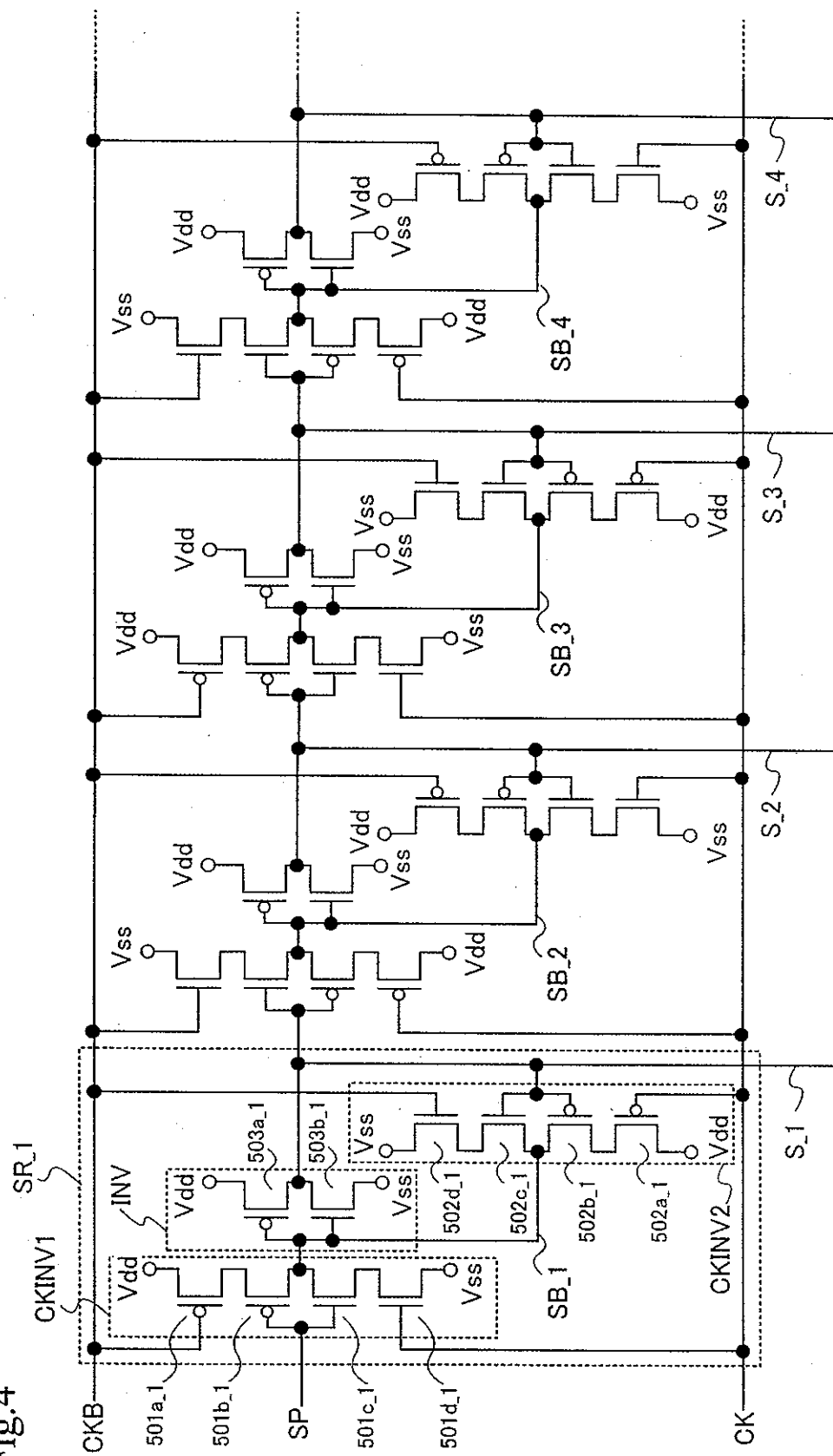


Fig.5

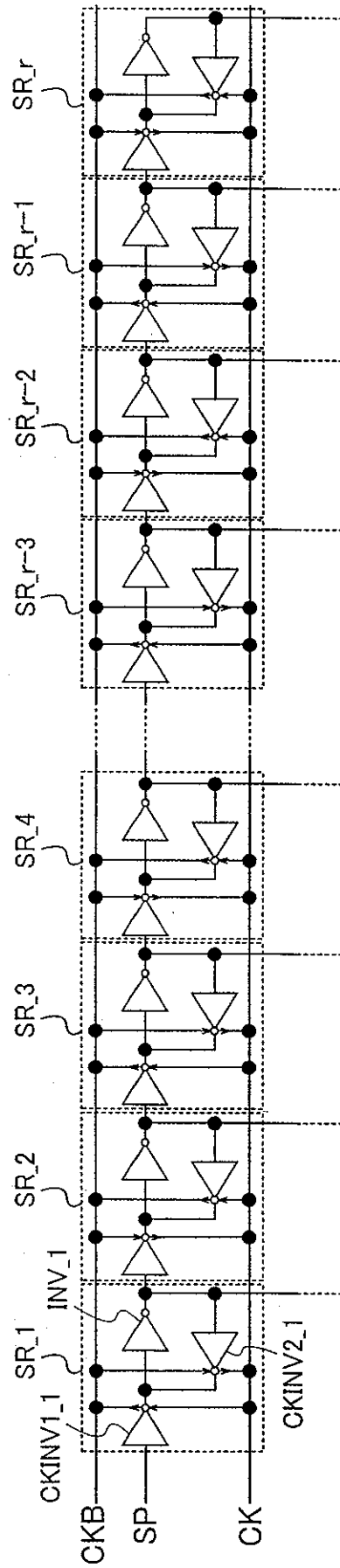


Fig.6

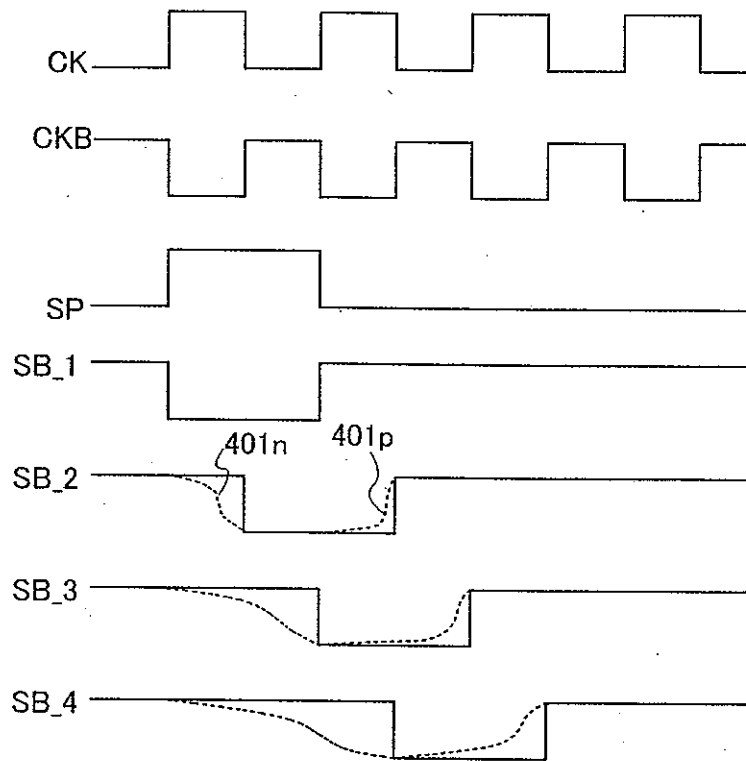
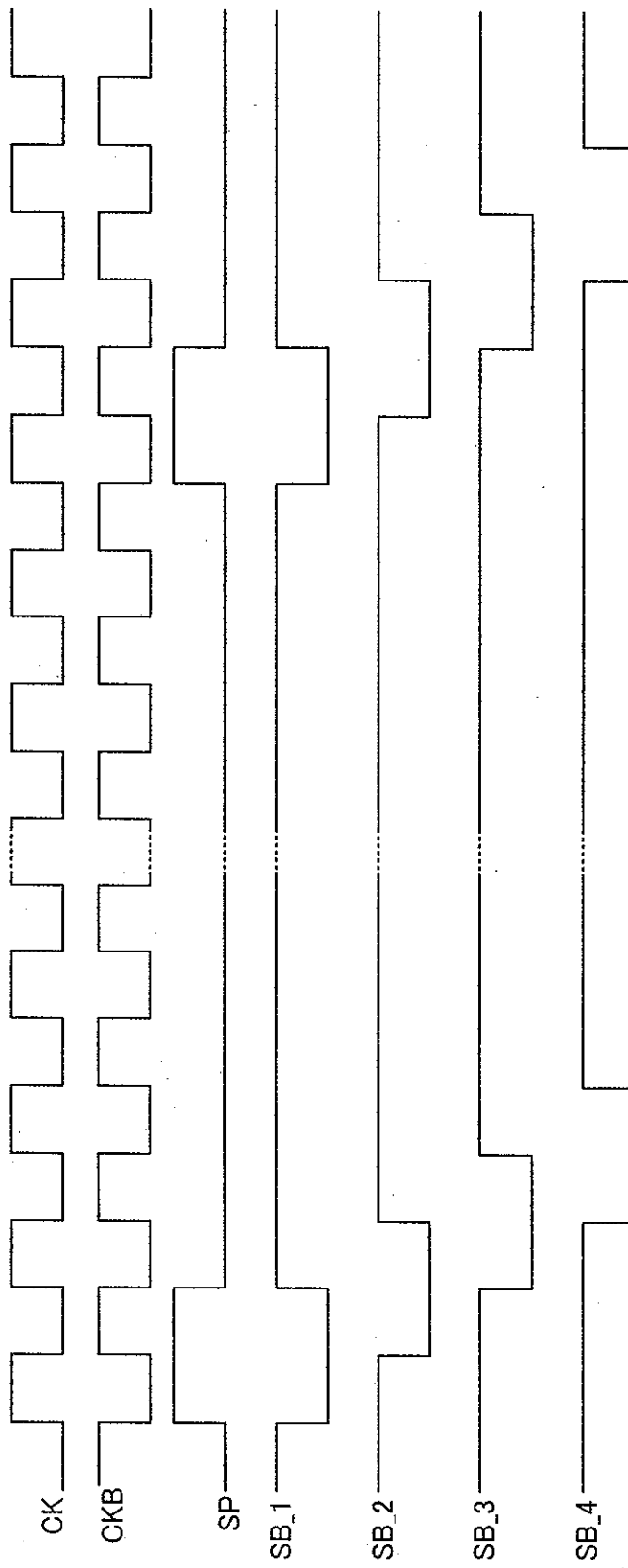


Fig.7



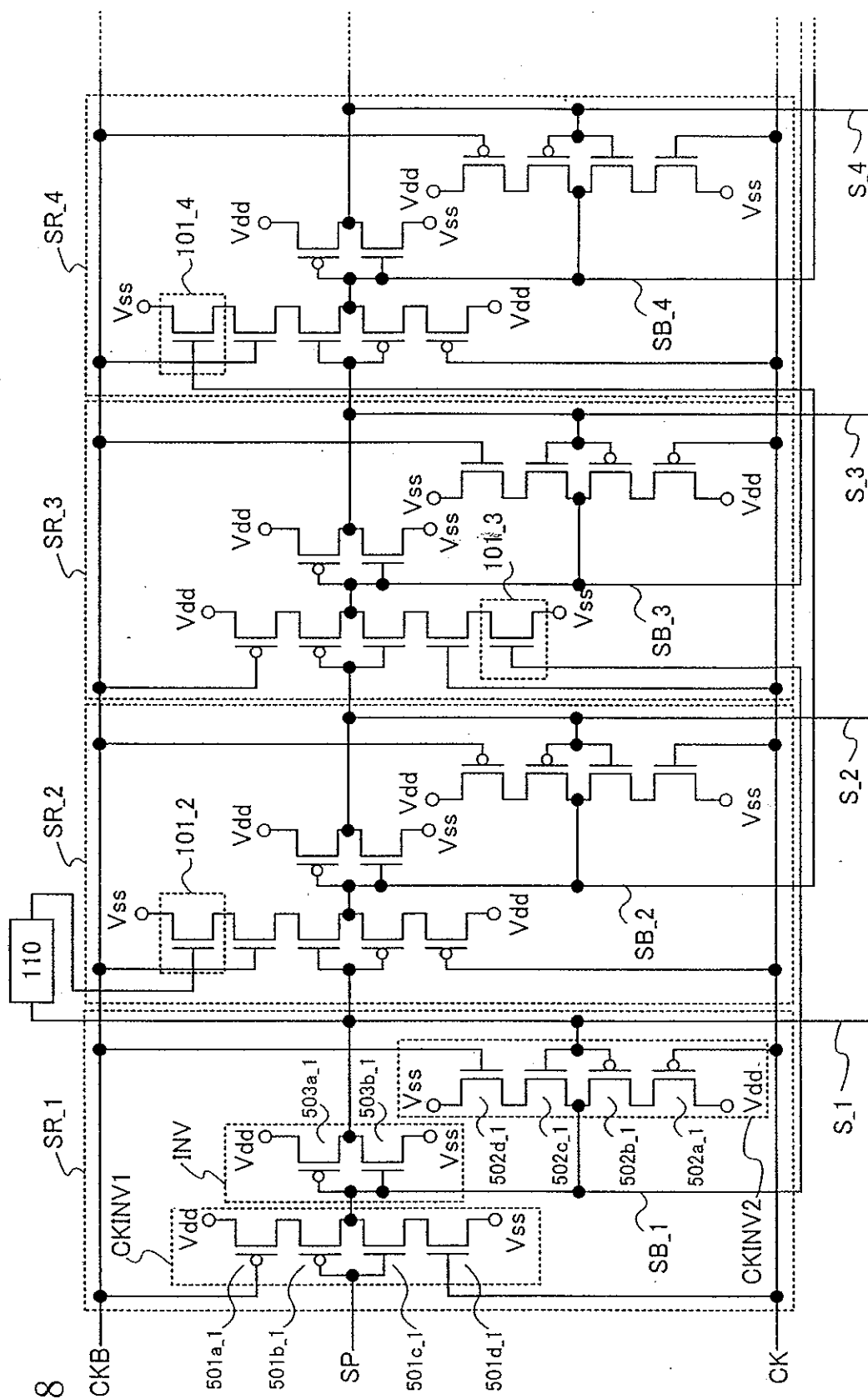


Fig.8

Fig.9

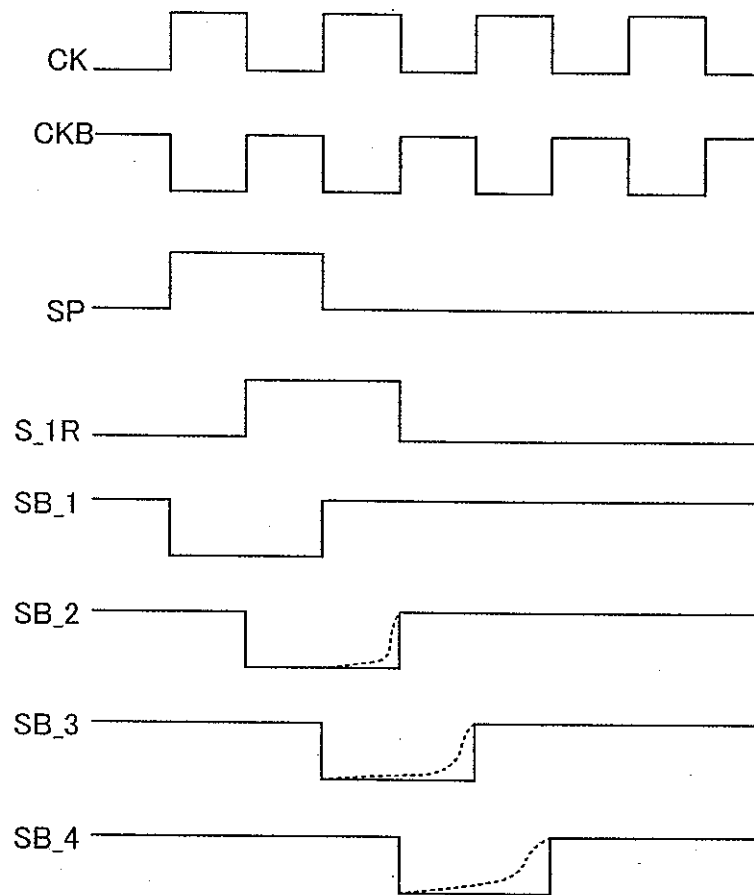


Fig.10

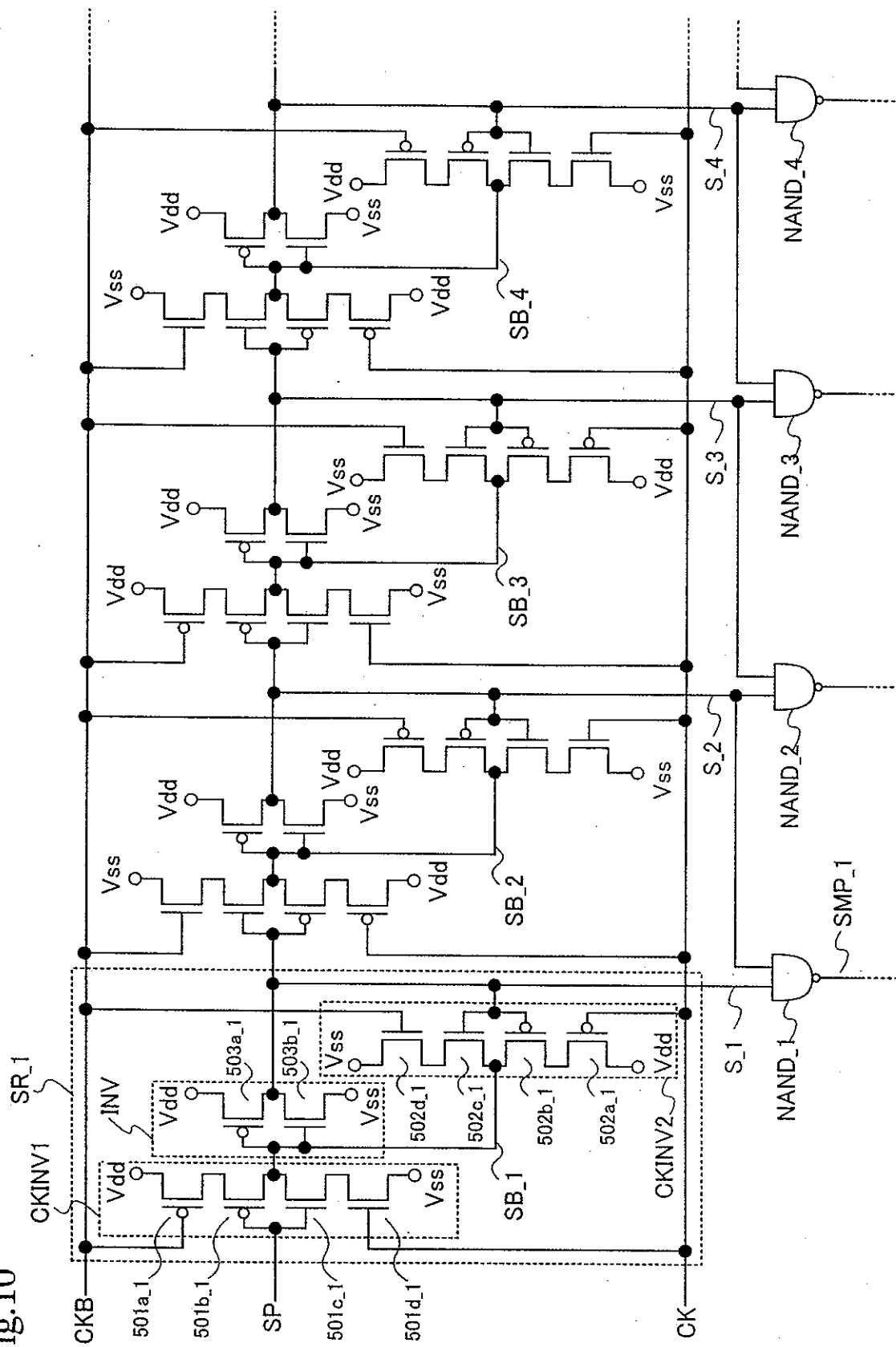


Fig.11

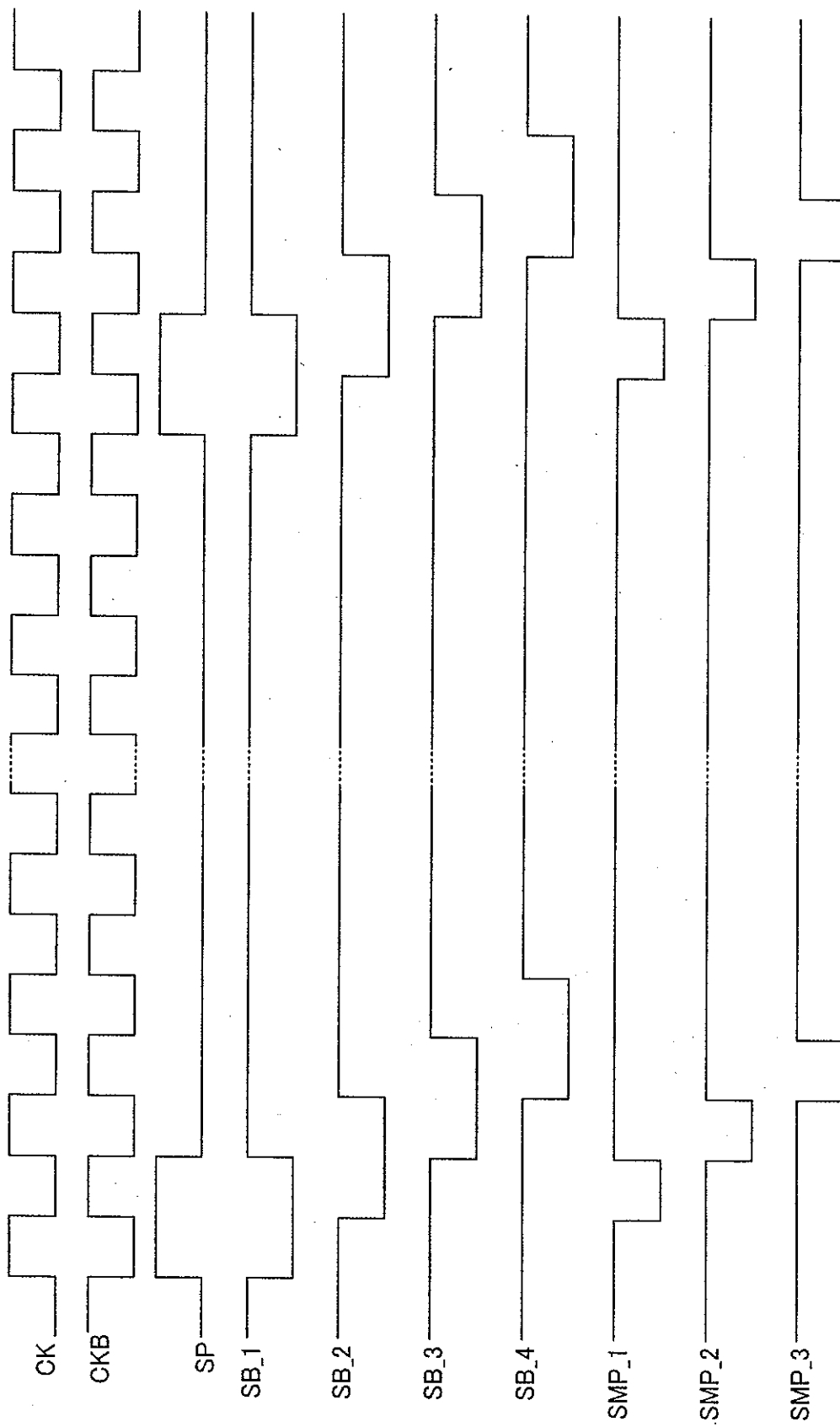


Fig.12

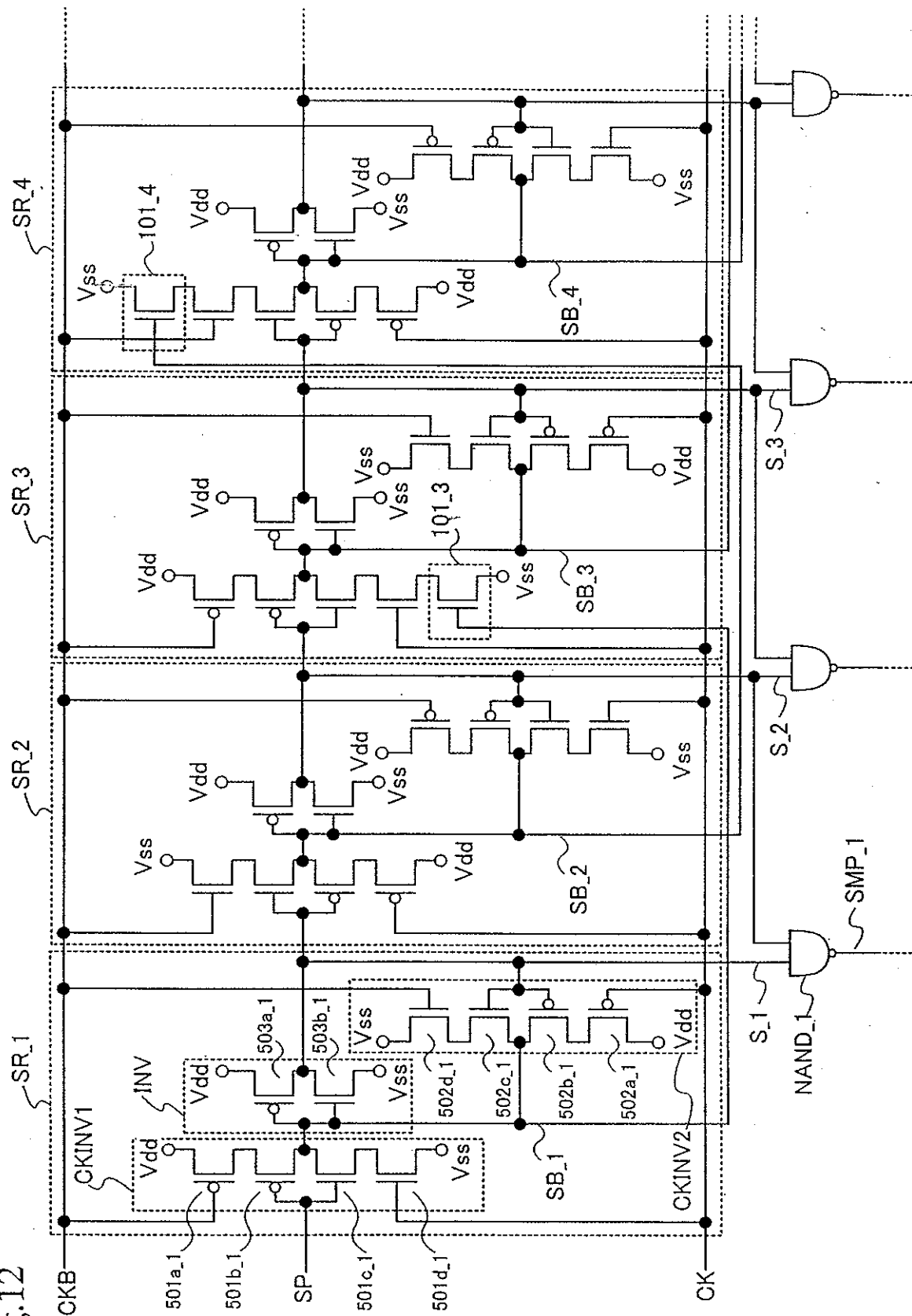
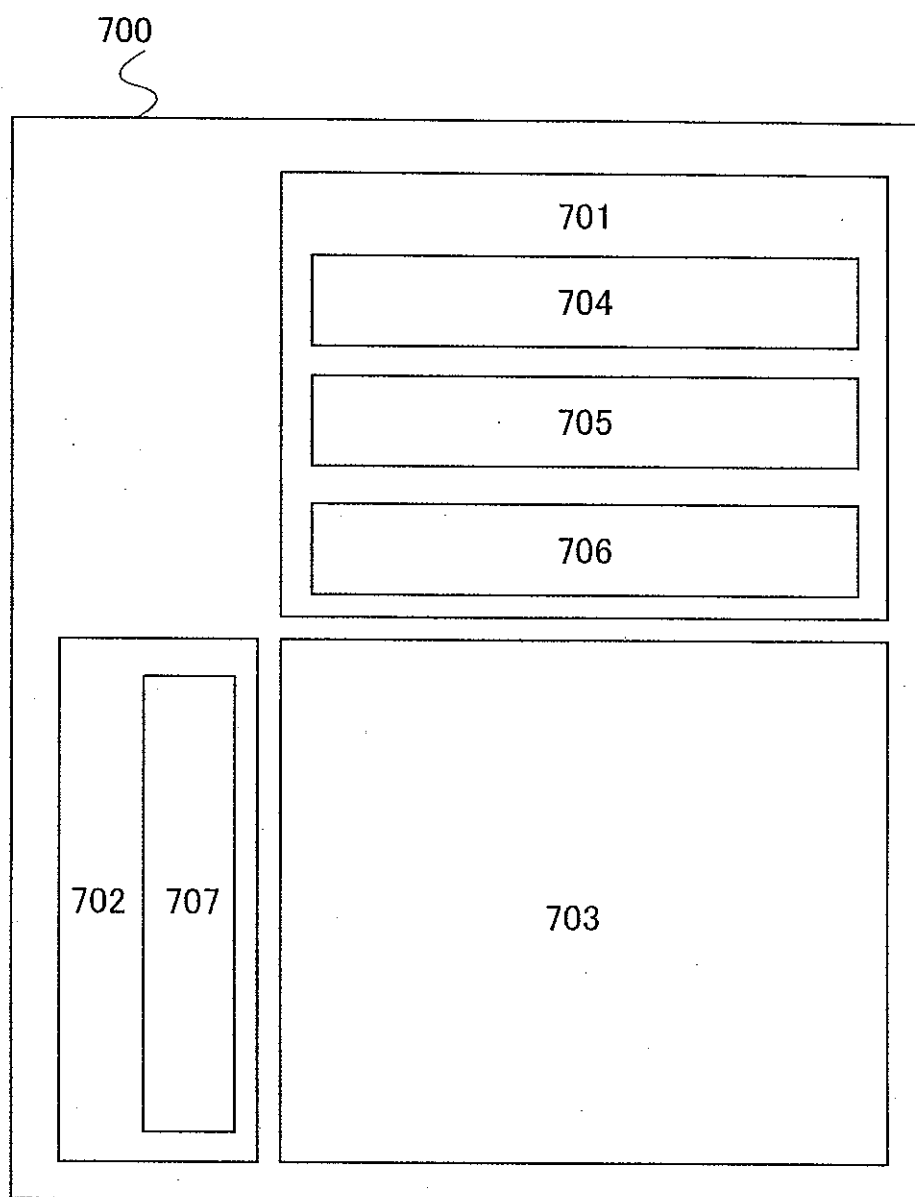


Fig.13



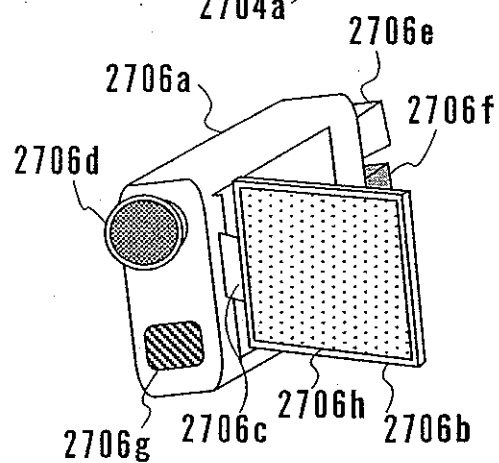
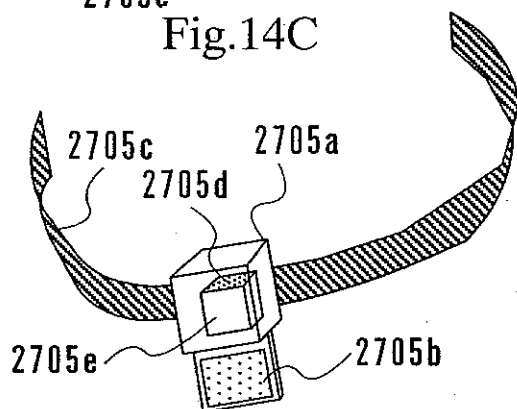
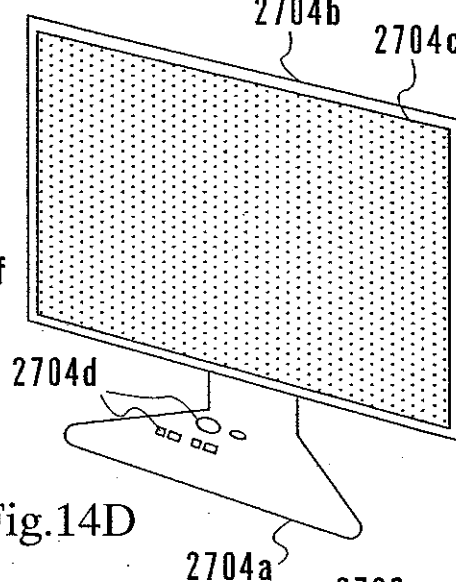
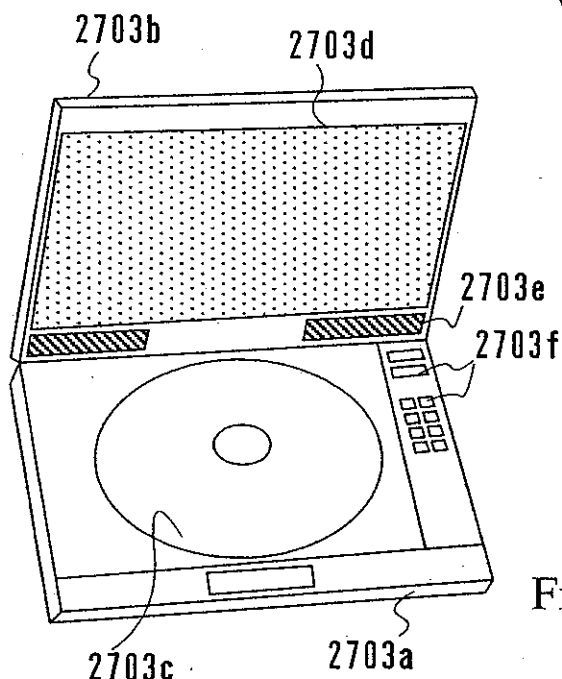
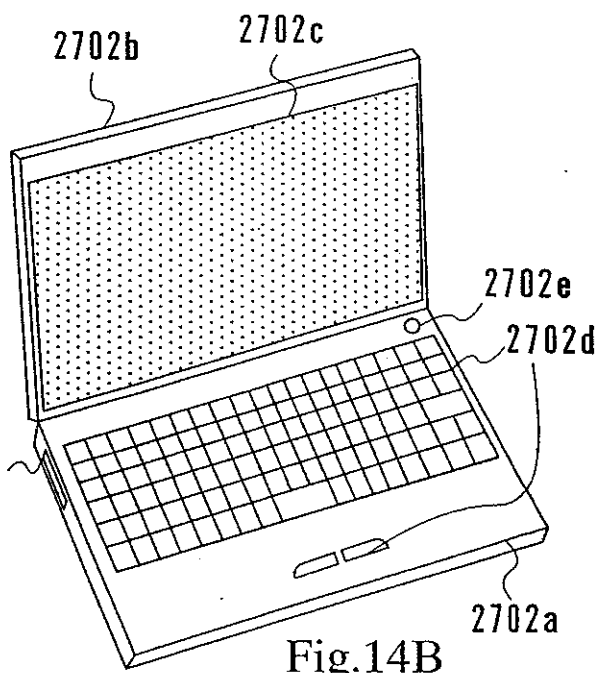
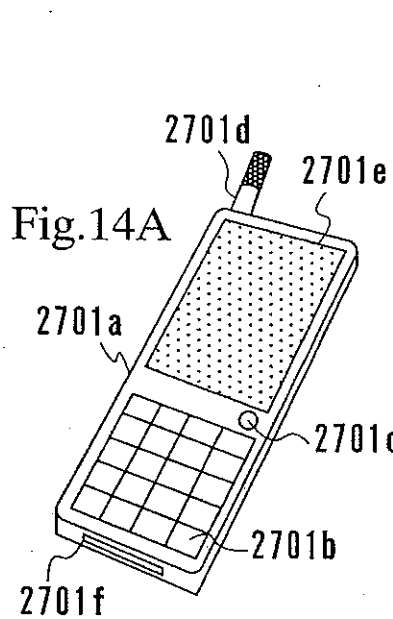


Fig.15

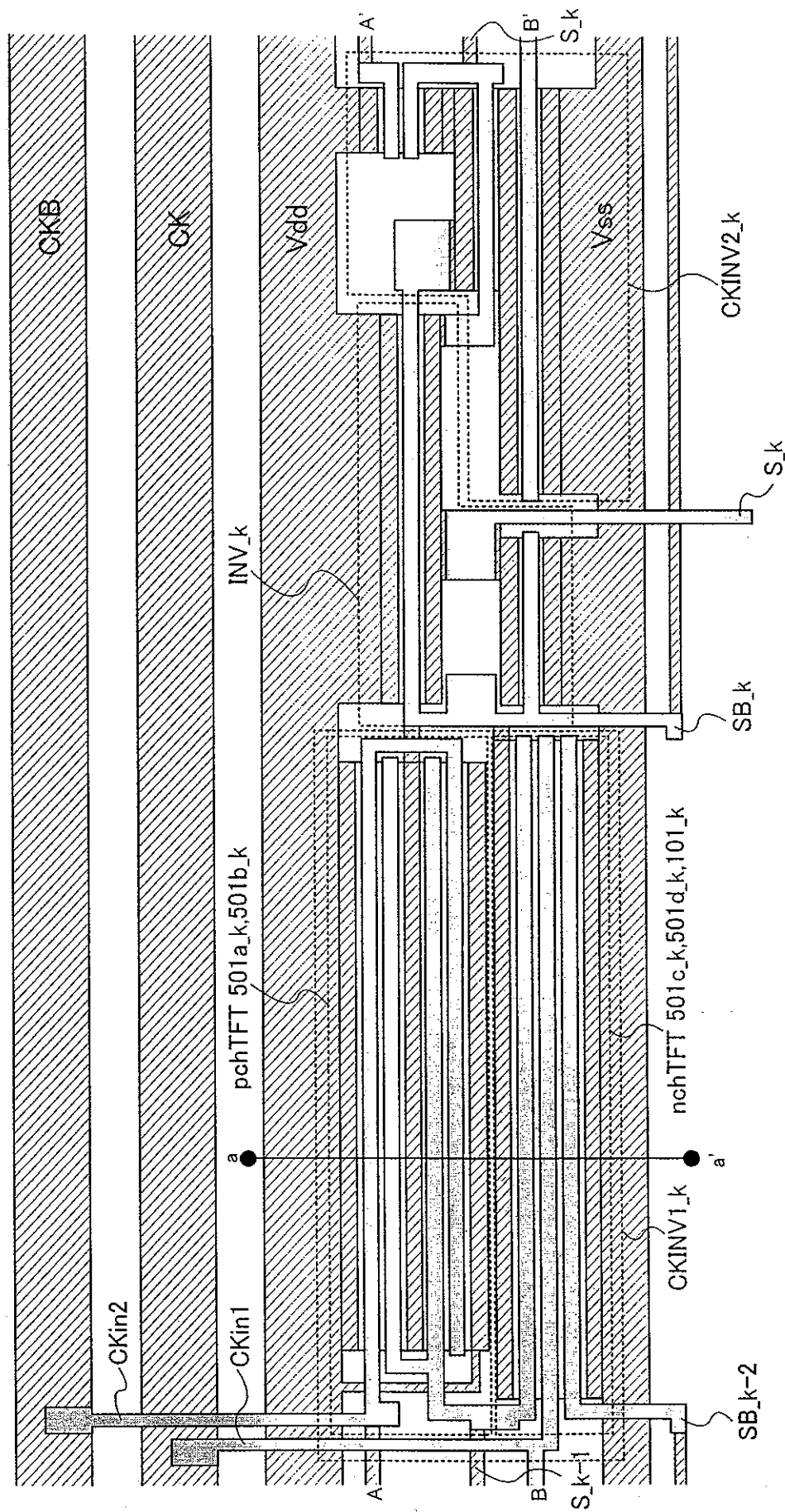


Fig.16

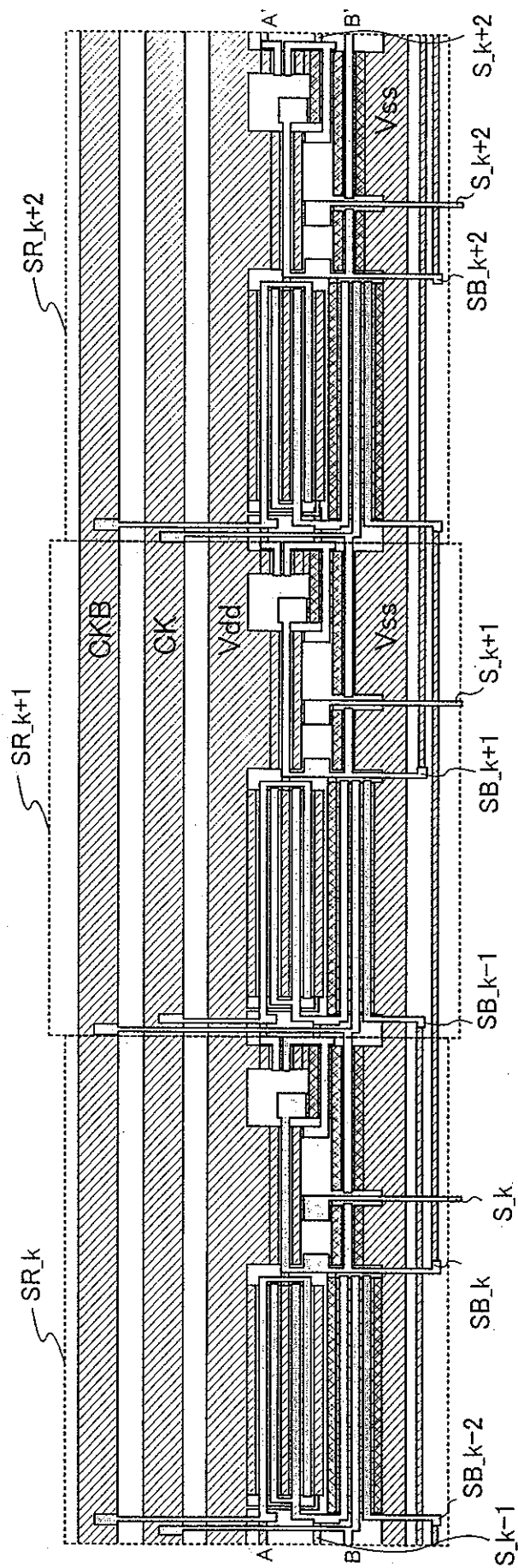




Fig. 18

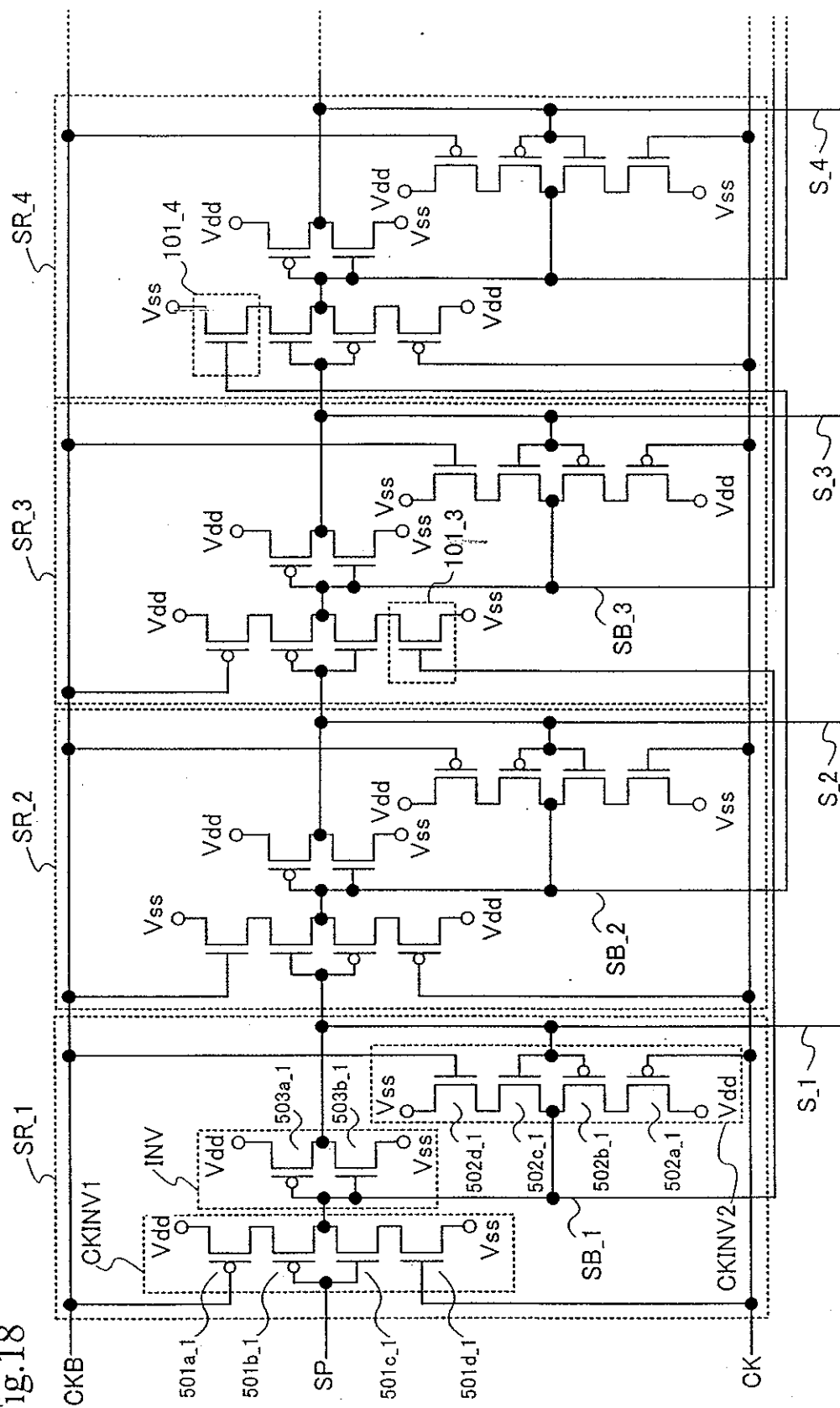


Fig. 19 is a schematic diagram of a semiconductor device, showing four stages (S1, S2, S3, S4) of a signal path. Each stage contains a differential pair of transistors (501a, 501b, 501c, 501d) and a load network (502a, 502b, 502c, 502d). The stages are connected in series, with the output of one stage feeding into the next. The diagram includes labels for various components and signals, such as CKIN1, CKIN2, CKB, CK, SP, SR1, SR2, SR3, SR4, SB1, SB2, SB3, SB4, and VDD/VSS.

Fig.20

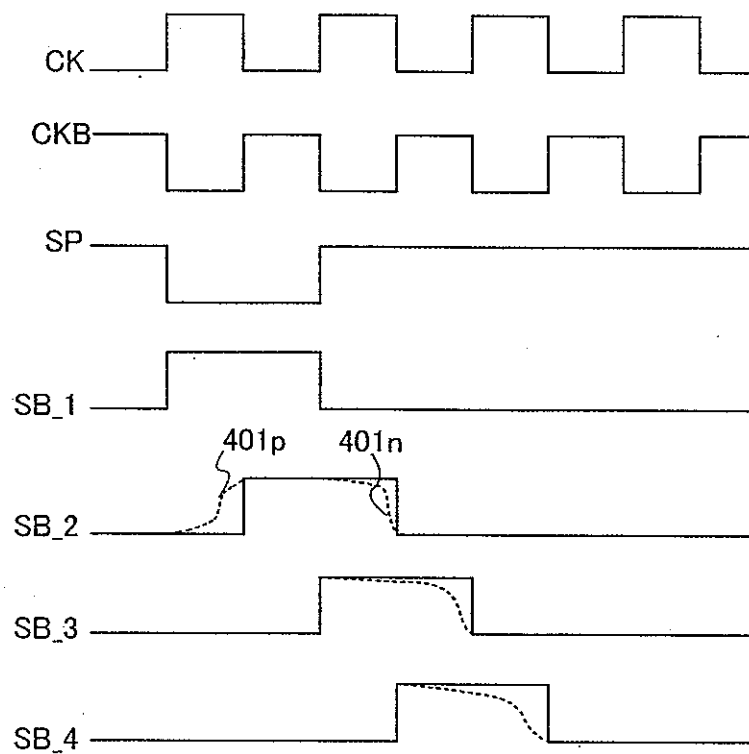


Fig. 21

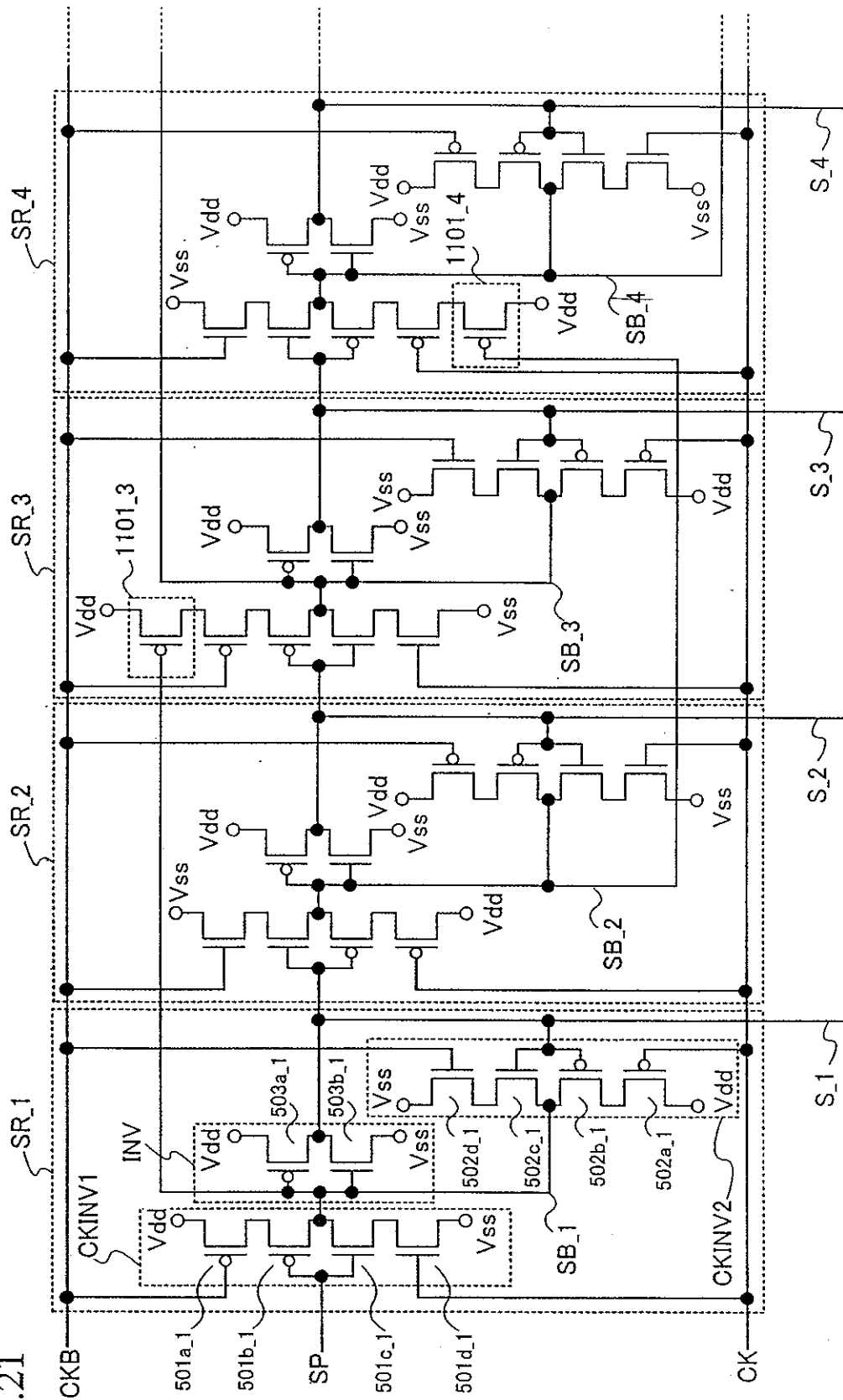


Fig.22

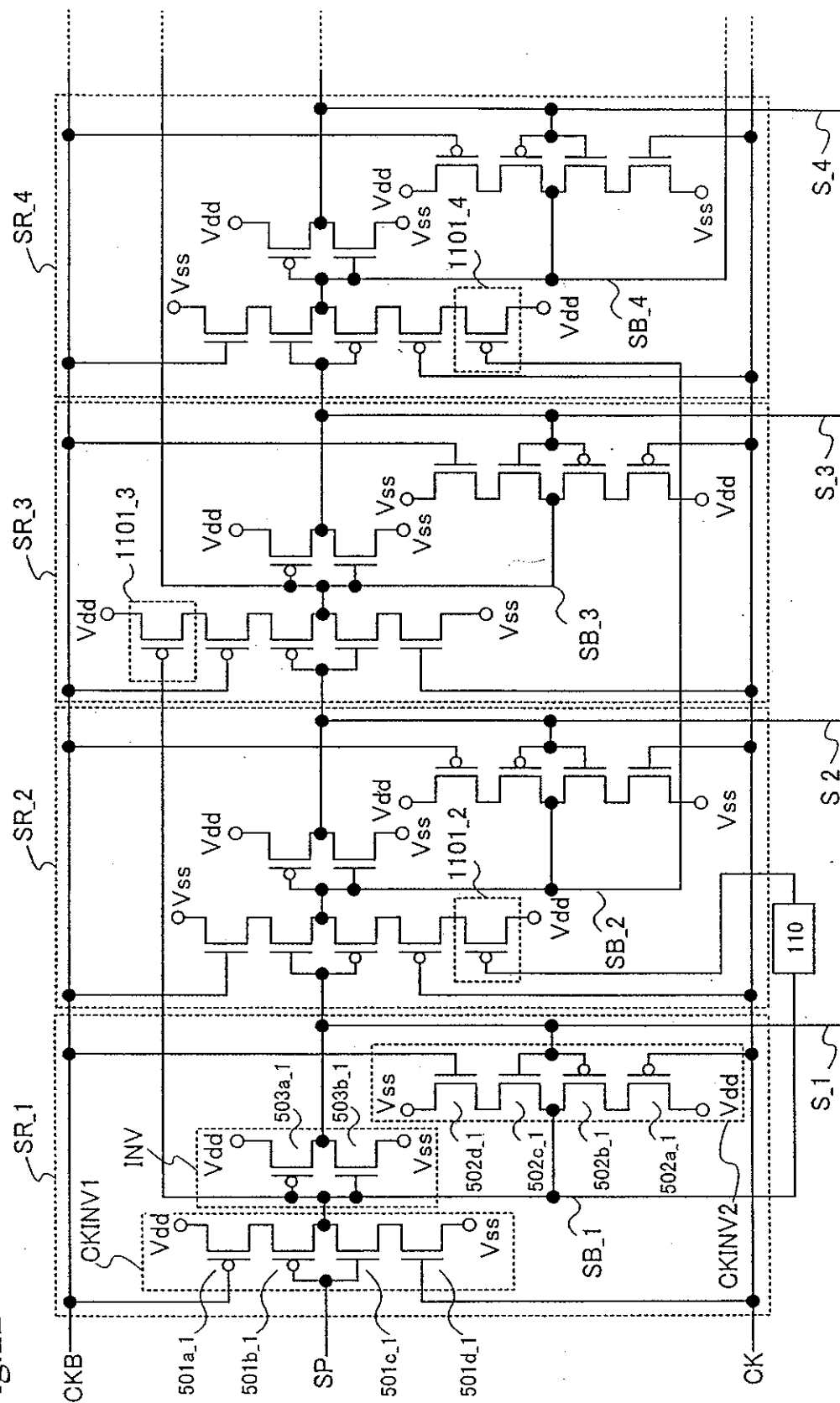


Fig.23

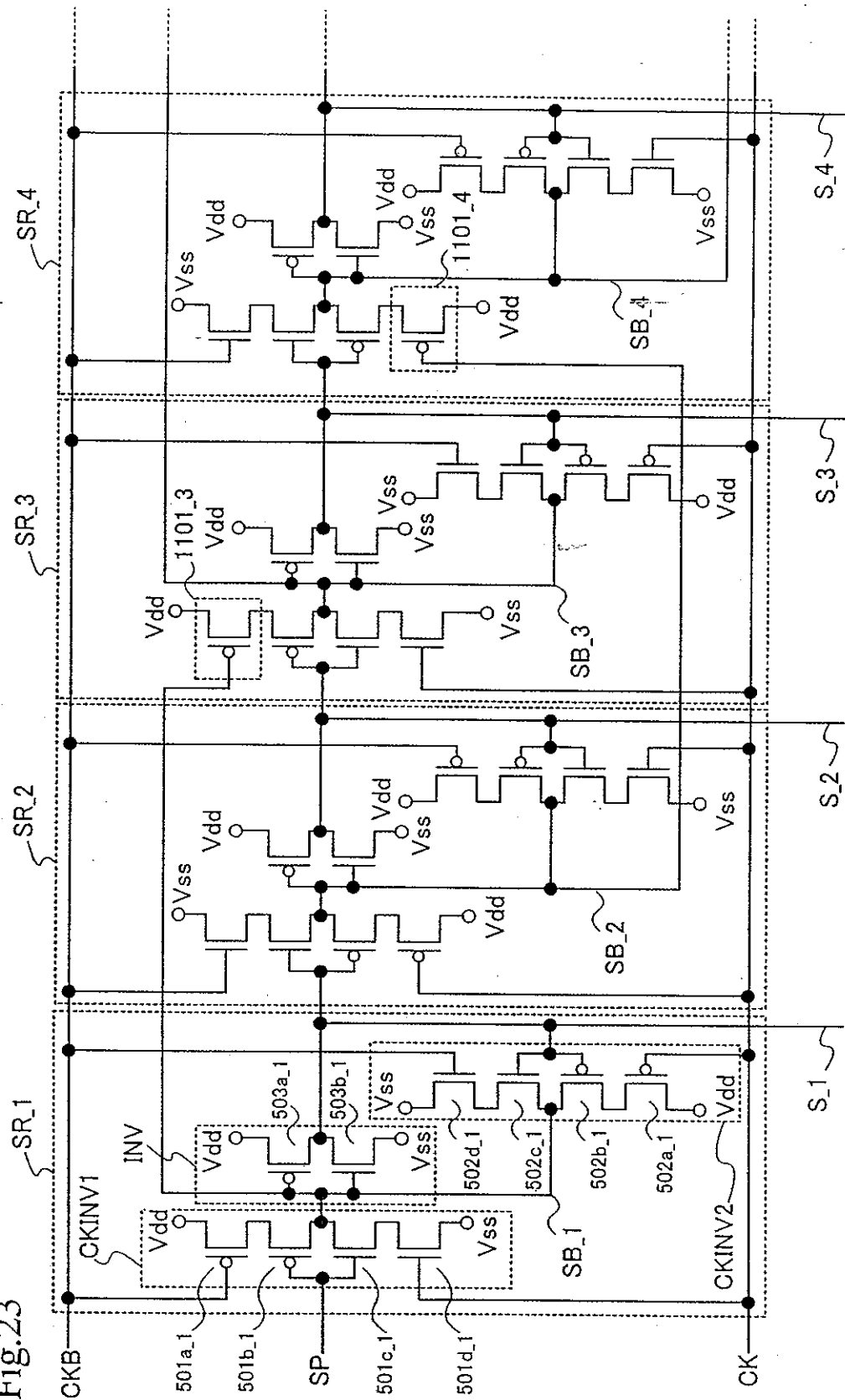


Fig. 24

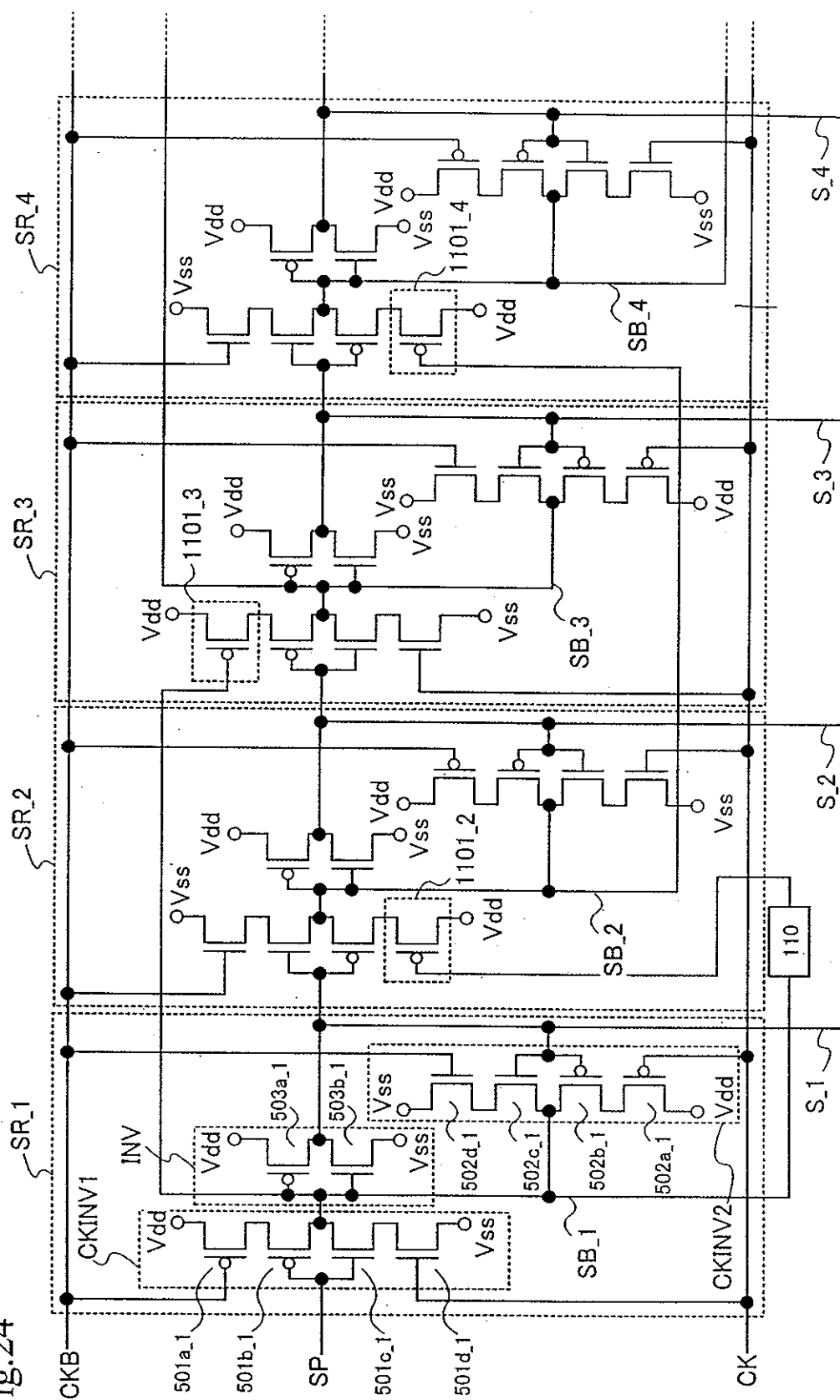


Fig. 25

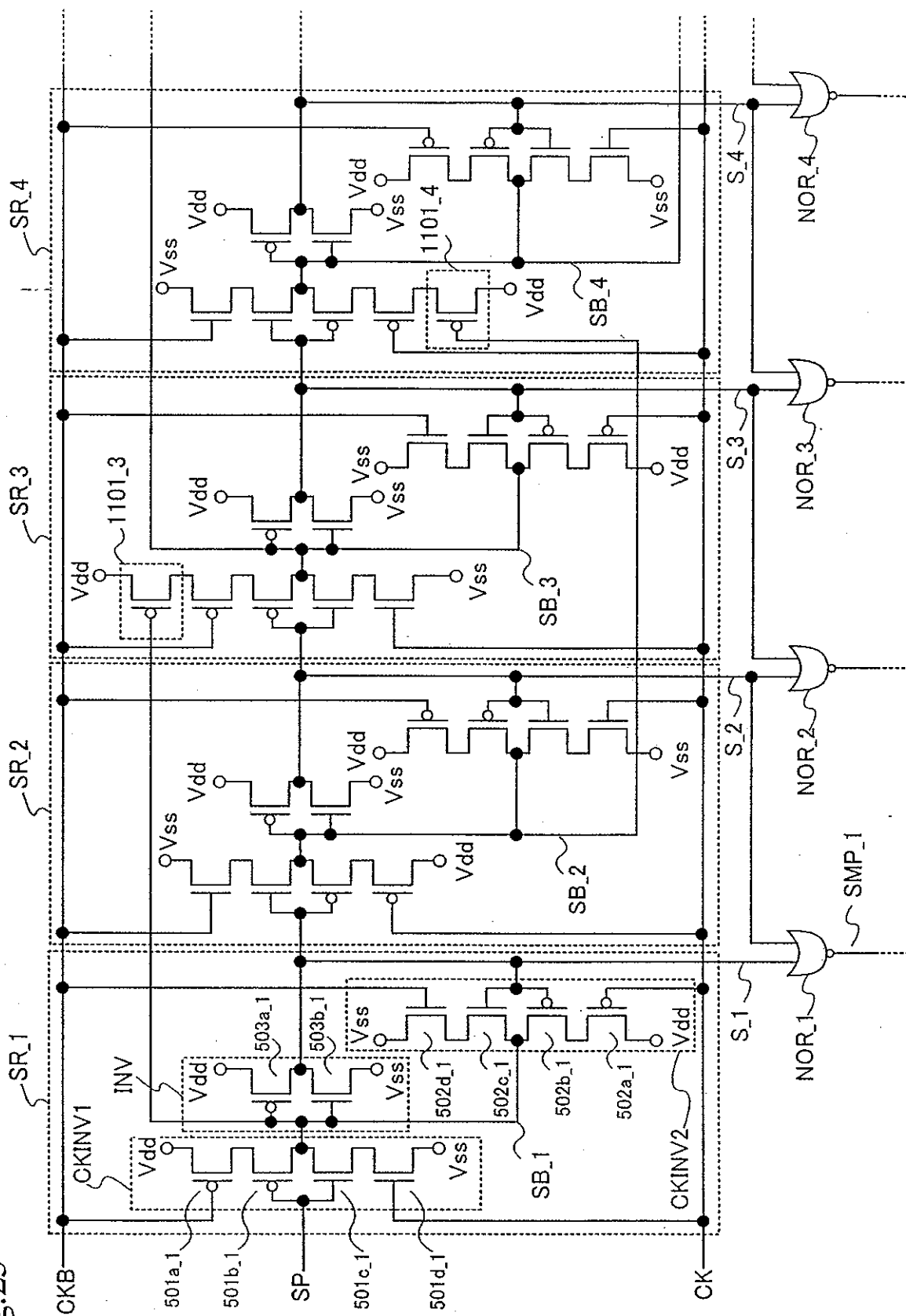


Fig.26A

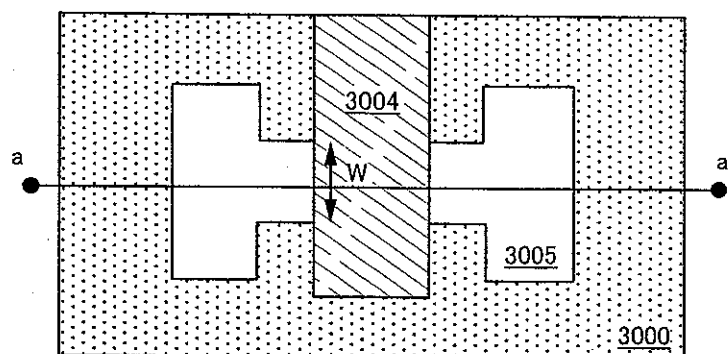


Fig.26B

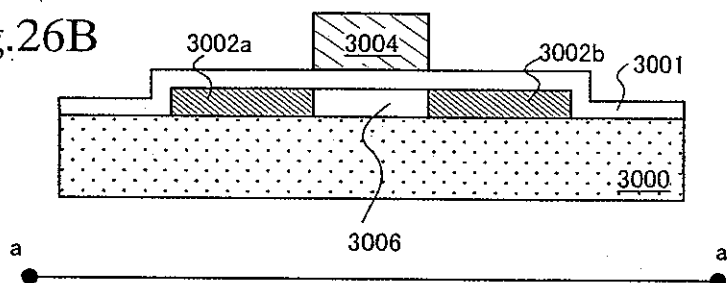


Fig.27

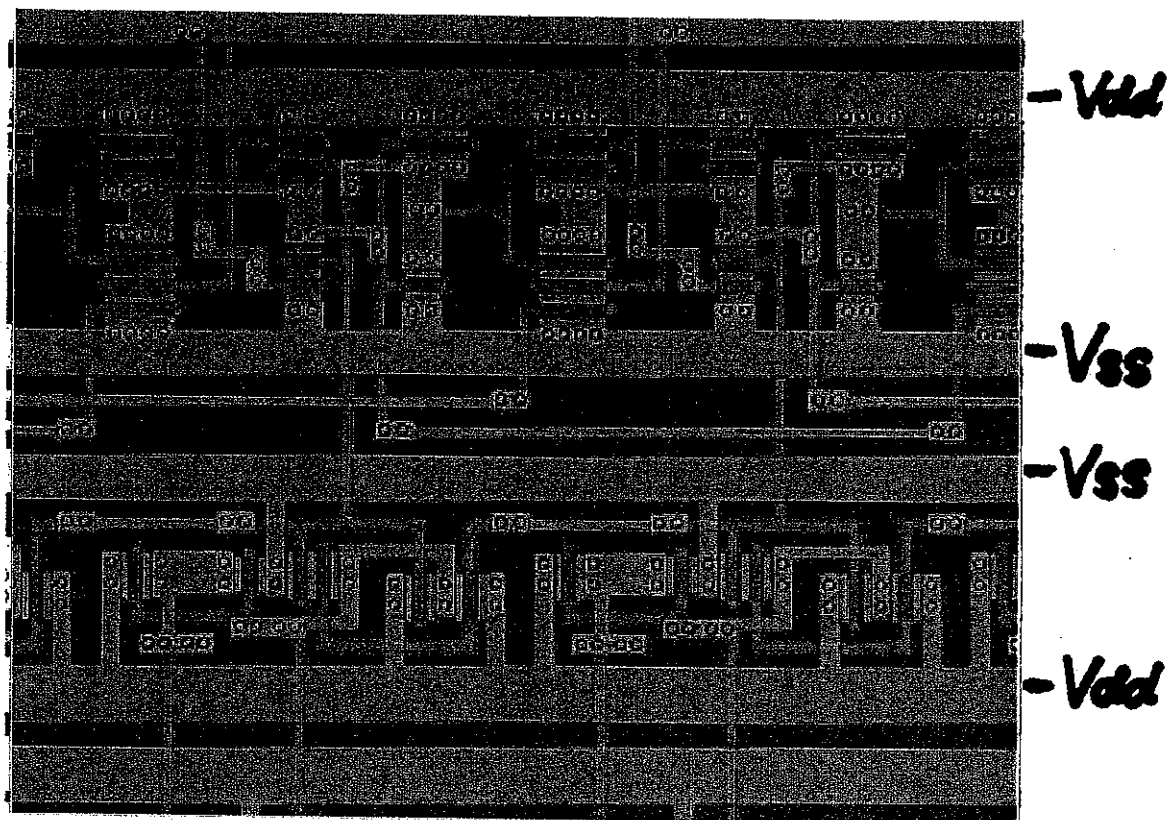


Fig. 28

