Connecting the emitter contacts of a semiconductor device

Description

The invention relates to a semiconductor device according to Claim 1 and to a method for fabricating a semiconductor device according to Claim 5.

Fig. 16 shows a conventional semiconductor device which will be used to demonstrate the problems of the prior art with which the invention is concerned. The semiconductor device comprises a (vertical) bipolar transistor 10, which, in a known way, has a base contact 12, an emitter contact 14 and a collector contact 16. The bipolar transistor 10 may be an npn transistor or a pnp transistor which, for example, forms part of a radio frequency circuit of the semiconductor device. In addition, a CMOS circuit, which in the simplest case comprises an MOS transistor 20 with a source contact 22, a gate contact 24 and a drain contact 26, may be provided on the same substrate 8 (for example a silicon wafer).

A characteristic feature of bipolar CMOS circuits of this type is that the emitter contact (known as the emitter stack) 14 is designed to be significantly "higher" above the process surface 8' of the substrate 8 than all the other contacts. The contact surface, remote from the process surface 8' of the substrate 8, of the emitter contact 14 is at a greater distance from the process surface 8' than contact surfaces of the other contacts 12, 16, 22, 24 and 26. This relative great height of the emitter contact 14 results from necessary process demands imposed on an optimized bipolar transistor.

By way of example, the overall height of the emitter contact 14 of a bipolar transistor corresponding to the Infineon B9C process above the process surface 8' is typically 550 nm. By contrast, by way of example, the height of the polysilicon gate contact 24 of an MOS transistor 20 arranged on the same substrate 8 is typically only 280 nm.

These very different heights of the contact surface of the emitter contact 14 compared to the other contacts lead to serious process technology problems with regard to connecting these contacts via contact holes 32 to a first patterned metal plane 34 (known as the metal-1 plane), and these problems are described below.

All the active components of the semiconductor device (i.e. the bipolar and CMOS transistors), after the FEOL (front end of line) process end, are typically covered with a dielectric 30, for example BPSG (Borophosphosilicate glass) to a total height of approximately 1400 nm. Fig. 1 shows a semiconductor device following the step of depositing this insulator layer 30 (BPSG layer). At this stage of the process, the semiconductor device according to the invention is not yet different from the prior art.

Then, the insulator layer 30 is polished back until it is planar with a specified target thickness by means of a chemical mechanical planarization step (CMP BPSG step). The semiconductor device obtained after this polishing step has ended is diagrammatically depicted in Fig. 2.

The high emitter contact 14 means that the planar polishing step (CMP BPSG step) is extremely critical. Whereas in the Infineon C9N process, which is a CMOS logic process belonging to the ninth generation using 0.25 μm technology, this planar polishing step is not a process technology requirement on account of the

relatively low height of the gate contact 24 (approximately 280 mm above the substrate surface), transferring the process specification for the C9N CMP BPSG step directly would lead to significant losses of production yield.

For example, in accordance with the C9N process, the insulator layer 30 (the BPSG layer) is polished back to a total height of 700 nm ± 150 nm in the CMP BPSG polishing step. Therefore, taken as an average over the entire wafer, there is a minimum BPSG layer thickness of 550 nm above the substrate surface, and consequently a BPSG layer 30 with a height of at least 270 nm remains above the gate contact 24. Position-dependent occupation densities of the active components may cause the BPSG layer thickness to locally drop below the typical value of 550 nm. Therefore, the layer heights of the insulator layer 30 achieved for a pure logic-based process in accordance with C9N are not critical, resulting in a relatively wide process window for the CMP BPSG step.

However, if a bipolar transistor 10 is provided as the active component of the semiconductor device (if appropriate in addition to a CMOS transistor 20), the process technology situation is somewhat different. Specifically, if the specification for the step of polishing the insulator layer 30 (CMP BPSG) is transferred direct from the CMOS logic process (Infineon C9N process: BPSG layer height 700 nm ± 150 nm) to the bipolar CMOS process (Infineon B9C process), the most unfavourable scenario, given an emitter contact height of 550 nm above the substrate 8, may result in a BPSG insulator layer 30 with a height of only a few nanometers. This very thin insulator layer 30 above the emitter contact 14 is not suitable for subsequent patterning of a contact hole 32. Consequently, the process window for the planarization

step (CMP BPSG) is greatly reduced with B9C process technology.

Furthermore, it is likely that future bipolar transistor generations, which comprise in particular silicon-germanium heterobipolar transistors, will have even higher emitter contacts (emitter stacks) compared to the other contacts (for example the gate contact polystack), which will intensify this problem still further.

A further problem of conventional semiconductor devices which is associated with the relatively high emitter contact 14 is based on the high process engineering demands on the step of patterning the contact holes 32 (CT), via which the contacts 12, 14, 16, 22, 24 and 26 are in each case connected in a standard way to the first patterned metal plane 34. For example, the etching step (CT etch step) for the contact holes 32, which is typically a plasma etching step, has to be highly selective with respect to the emitter contact 14 (polysilicon contact), in order to allow even the "deepest" contact surfaces (i.e. the surfaces located closest to the process surface 8' of the substrate 8) to be opened up reliably and without residues yet without the emitter contact 14 being attacked. For example, with the abovementioned specifications of the C9N process, source contacts 22 and drain contacts 26 of the MOS transistor 20 may be "buried" a maximum of 850 nm below the insulator layer 30 following the polishing step (CMP BPSG).

To enable these contacts 22 and 26 located close to the substrate to be opened up without leaving any residues by means of the plasma etching step, a relatively long etching time is required. This long etching time, in conjunction with a BPSG layer thickness of 700 nm ± 150 nm, means that, for a minimum thickness of 550 nm that after even a short etching time duration

the etching front of the contact hole 32 which is located above the emitter contact 14 will have reached the contact surface of the emitter contact 14. From this instant onwards, the contact surface of the emitter contact 14 is exposed to the plasma etch. Only if the plasma etching step etches the insulator 30 (e.g. BPSG) highly selectively (through the addition of suitable passivation compounds to the etching plasma) with respect to the contact material (e.g. polysilicon) can the etching process for opening up the deep-lying contact be continued without the emitter contact 14 being attacked. This process engineering requirement may lead to further significant yield losses.

In addition to the process engineering difficulties entailed by the production of the conventional semiconductor device described above (critical process window for the CMP BPSG and CT etch process steps), in known semiconductor devices of this type the contact surface area of the emitter contact 14 is disadvantageously restricted to the surface area of the contact hole 32. Bipolar applications, which require high emitter-collector current intensities, can only be realized to a limited extent on account of the less than optimum utilization of the cross section of the emitter contact 14.

The problems described above in connection with the fabrication of the known semiconductor device have hitherto been solved by "widening" the specification, derived from the C9N process, for the polishing step (CMP BPSG) carried out on the insulator layer 30. Whereas the C9N process required a specification of 700 nm ± 150 nm for the layer height of the insulator layer 30 following the planarization step, the bipolar CMOS process step (Infineon B9C process) only demanded a layer height of the insulator layer 30 of 750 nm ± 150 nm above the process surface 8'.

If the height of the emitter contact is reduced by 50 nm (i.e. to 500 nm), the process window for the step of etching the contact holes 32 is, as it were, restricted, since there is now a smaller "reserve" of polysilicon of the emitter contact 14 which can be attacked by the contact hole etch (CT etch). This reduces the process window for the plasma etching step for the contact holes 32.

In view of the abovementioned drawbacks of conventional semiconductor devices and their production processes, it is an object of the invention to provide a semiconductor device and a process for producing a semiconductor device in which the height of a contact (for example of the emitter contact 14) can be selected as desired without making the processing of the semiconductor device more difficult in the long term.

This object is achieved by a semiconductor device as described in Claim 1 and a method for fabricating a semiconductor device as described in Claim 5. Preferred embodiments form the subject matter of the dependent claims.

According to a first expression of the invention, a semiconductor device comprises

- a substrate, the process surface of which has a substrate-normal direction;
- at least a first contact and a second contact arranged on the substrate, a contact surface of the second contact being at a greater distance, in the substrate-normal direction, from the substrate than a contact surface of the first contact; and
- at least a first and a second patterned metal plane, in each of which at least one conductor, which is electrically connected to at least one of the contacts, is formed;

the second metal plane being at a greater distance, in the substrate-normal direction, from the substrate than the first metal plane,
the second contact being electrically connected to a conductor, located above it in the substrate-normal direction, of the second metal plane without a conductor of the first metal plane being connected in between, and
the first contact being electrically connected to a conductor, located above it in the substrate-normal direction, of the second metal plane via an interposition of a conductor, located above the first contact in the substrate-normal direction, of the first metal plane.

As has already been described above, it is customary for all the contacts of the active components of conventional semiconductor devices to be connected, typically via what are known as contact holes (CT), to conductors, located above them in the substrate-normal direction, of a first patterned metal plane. For example, if the active component of the semiconductor device is a bipolar transistor, respective conductors of the first patterned metal plane are connected to the base contact, the emitter contact and the collector contact of the transistor.

However, according to the invention, a contact whose contact surface is at a great distance from the process surface of the substrate is not connected to a conductor of the first metal plane. Instead, contact is only made with this contact in a subsequent process stage, for example through a contact hole leading to a second patterned metal plane, which is arranged above the first patterned metal plane, as seen in the substrate-normal direction. Consequently, the second contact, which has a considerable height above the process surface compared to the other contacts, can be

21 APR 2006

provided with any desired height, since there is no need to make

contact with this second contact together with the other contacts via the first patterned metal plane.

There is no conductor belonging to the first metal plane arranged above the second (high) contact, as seen in the substrate-normal direction. Instead, only a conductor of the second metal plane, which is connected to the contact surface of the second contact for example via a tungsten contact pin, is located above the second contact.

With this semiconductor device according to the invention, particular advantages result from the fact that further vertical connecting contacts (known as VIA connecting contacts) are usually provided in any case after processing in order to connect certain conductors belonging to the first metal plane to higher conductors belonging to the second metal plane. Therefore, contact can be made between the second contact and the second metal plane via the VIA-1 connecting contacts, and consequently there is no need for any additional lithography, cleaning, metallization and polishing steps in order to make contact with the second contact via the higher metal plane.

According to a preferred embodiment, the second contact is an emitter contact of a bipolar transistor, and the first contact is a base contact or collector contact of a bipolar transistor or a source contact, gate contact or drain contact of an MOS transistor. As has already been described in the introduction, the emitter contact of a bipolar transistor, compared to the other contacts of the active components of a semiconductor device, typically has the greatest height above the process surface of the substrate. It is therefore advantageous for the (relatively high) emitter contact not to be connected to a conductor of the first metal plane, but rather to be connected only to a conductor of the second metal plane, for example via a VIA-1 contact.

Therefore, there is no conductor belonging to the first metal plane located above the emitter contact.

The first contact is preferably connected to the conductor of the first metal plane via a contact hole which extends in the substrate-normal direction and is filled with an electrically conductive contact-hole filling material. The contact-hole filling material may, for example, be tungsten which is introduced into a previously plasma-etched contact hole using a MCVD process. What is known as a liner, for example a TiN liner, may be provided as a diffusion stop at all the interfaces (in particular between the contact-hole filling material and the metal plane or the contact material).

The second contact is preferably connected to the conductor of the second metal plane via a contact hole, which extends in the substrate-normal direction and is filled with an electrically conductive contact-hole filling material, without a conductor of the first metal plane being connected in between. As has already been explained above, the contact hole may be what is known as the VIA-1 connecting contact, which normally connects conductors of the second patterned metal plane to corresponding conductors of the first patterned metal plane. According to the invention, this VIA-1 connecting contact can be used to make contact with the second contact or a plurality of high contacts. No conductor of the first metal plane is arranged between the corresponding conductor of the second metal plane and the contact surface of the second contact, as seen in the substrate-normal direction.

According to a second expression of the invention, a method for fabricating a semiconductor device, in particular a semiconductor device in accordance with the first aspect of the invention, comprises the following steps:

- providing a substrate, the process surface of which has a substrate-normal direction;
- defining at least a first contact and a second contact on the substrate, a contact surface of the second contact being located at a greater distance, in the substrate-normal direction from the substrate than a contact surface of the first contact;
- electrically connecting the first contact to a conductor, located above it in the substrate-normal direction, of a first patterned metal plane; and
- electrically connecting the second contact to a conductor, located above it in the substrate-normal direction, of a second patterned metal plane without a conductor of the first metal plane being connected in between;

the second metal plane being at a greater distance, in the substrate-normal direction, from the substrate than the first metal plane,
characterized in that
at the same time as the step of electrically connecting the second contact to the conductor of the second metal plane, at least one conductor of the first metal plane is connected to a conductor of the second metal plane such that the first contact is electrically connected to said conductor, located above it in the substrate-normal direction, of the second metal plane via an interposition of the conductor, located above the first contact in the substrate-normal direction, of the first metal plane.

Accordingly, in a method for fabricating a semiconductor device in accordance with the invention, the second contact, which is further away from the process surface as seen in the substrate-normal direction, is not connected to a conductor of the first metal plane, but rather is connected only to a

conductor, located above it in the substrate-normal direction, of the second metal plane.

This simplifies the patterning of the electrical connections for the other contacts to form the first patterned metal plane to a considerable extent. This is because there is no need to take into account the (high) second contact or a multiplicity of such high second contacts when realizing the process engineering for electrically connecting the first contact to the first metal plane. Instead, the patterning and process parameters for making contact with the first contact

(or first contacts) can be optimized for this contact-making step. At the same time, the height of the second contact (i.e. the distance from the top of the second contact to the process surface, as seen in the direction normal to the substrate) can be selected as desired (provided that the BPSG layer thickness is adapted at the same time; its minimum height must be greater than or equal to the resulting contact height of the second contact), in order to ensure optimum patterning and component properties.

The second contact is preferably an emitter contact of a bipolar transistor, and the first contact is preferably a base contact or collector contact of a bipolar transistor or a source contact, gate contact or drain contact of an MOS transistor.

The step of electrically connecting the first contact preferably comprises the following steps:

- defining a contact hole, which ends at the first contact and extends in the substrate-normal direction, in an insulator;
- filling the contact hole with an electrically conductive contact-hole filling material; and
- defining the conductor, which lies above the first contact in the substrate-normal direction, of the first metal plane in such a manner that it is electrically connected to the contact-hole filling material.

By way of example, after the active components of the semiconductor device has been completed (FEOL process end), a dielectric insulator, such as BPSG (borophosphosilicate glass) is deposited on the semiconductor device by means of a CVD process, is polished back to a target height by means of a subsequent planarization step (CMP BPSG) and is patterned by means of conventional lithography and etching steps. The contact hole which is formed and

extends along the substrate-normal direction ends at the first contact with which contact is to be made or the first contacts with which contact is to be made. This contact hole can then be filled with an electrically conductive contact-hole filling material, preferably tungsten, by means of a MCVD metallization step. Then, it is preferable for a conductor of the first metal plane to be arranged on the tungsten contact pin, which has been planarized again, in such a manner that it is electrically conductively connected to the first contact.

The step of electrically connecting the second contact preferably comprises the following steps.

- defining a contact hole, which ends at the second contact and extends in the substrate-normal direction, in an insulator;
- filling the contact hole with an electrically conductive contact-hole filling material; and
- defining the conductor, which lies above the second contact in the substrate-normal direction, of the second metal plane. As noted above, this is done in such a manner that it is electrically connected to the contact-hole filling material without a conductor of the first metal plane being connected in between.

As noted above, at the same time as the step of electrically connecting the second contact to the conductor of the second metal plane, at least one conductor of the first metal plane is connected to a conductor of the second metal plane. Accordingly, the second contact is preferably electrically conductively connected to a conductor of the second metal plane via what is known as the VIA-1 connecting contact. The processing of these VIA-1 connecting contacts forms part of the standard processes carried out on semiconductor devices of this type, and consequently there is no need for any additional patterning steps to

make contact with the second contact compared to conventional processing processes.

The invention is described below by way of example with reference to accompanying drawings showing preferred embodiments, in which:

Figs. 1 to 14 show diagrammatic sectional views through a preferred embodiment of a semiconductor device in accordance with the first aspect of the invention at various patterning or processing stages during the fabrication method;

Fig. 15 shows a diagrammatic sectional view through a preferred embodiment of a semiconductor device in accordance with the second aspect of the invention; and

Fig. 16 shows a sectional view through a conventional semiconductor device.

Fig. 1 shows a sectional view through a preferred embodiment of a semiconductor device in accordance with the first aspect of the invention. The semiconductor device is at a process stage in which the active components - such as the bipolar transistor 10 and the MOS transistor 20 - have already been completed. The FEOL (front end of line) process end, in which in particular high-temperature steps may occur, has therefore already been reached.

As shown in Fig. 1, in the following process step the entire semiconductor device is covered with a dielectric insulator 30, which may, for example, be BPSG (borophosphosilicate glass), preferably by means of a CVD deposition step (CVD BPSG step). The insulator layer 30 is typically applied in a layer height of approx. 1400 nm. This layer covering is significantly

greater than the height of the emitter contact 14, which is typically 550 nm, and of the gate contact 24, which is typically 280 nm.

In a following process step, illustrated in Fig. 2, the insulator layer 30 is polished back by a polishing step to a target height of typically 700 nm ± 150 nm, for which purpose known CMP (chemical mechanical planarization) steps are used (CMP BPSG step).

As illustrated in Fig. 3, contact holes 32 are then defined in the insulator layer 30 by means of a lithography and subsequent etching step (CT etch step). These contact holes 32 extend in the direction normal to the substrate 8, i.e. they have a vertical orientation. Unlike in a conventional fabrication method, for example for a semiconductor device as illustrated in Fig. 16, a contact hole 32 which ends at a contact surface of the emitter contact 14 is not defined. In other words, a window leading to the contact surface of the emitter contact 14 is not etched into the insulator layer 30.

Therefore, during the subsequent metallization steps contact is not made with the emitter contact 14, which in this embodiment of the semiconductor device is the second (higher) contact. On account of the fact that contact is not made with the emitter contact 14 (the second contact) in this process stage, the patterning of the contact holes 33, i.e. the CMP BPSG polishing step and the CT etch plasma etching step, does not need to be adapted to make simultaneous contact with the first and second contacts, which is complex in terms of the process engineering.

As a result, the process window for the CMP BPSG polishing step, the result of which is illustrated in Fig. 2, and for the CT etch plasma etching step (cf. Fig. 3) is widened considerably compared to a method

for fabricating the semiconductor device shown in Fig. 16. The permissible height in the substrate-normal direction for the second contact 14 no longer has to be selected while taking account of the patterning of the contact holes 32. Instead, in accordance with the fabrication method according to the invention for a semiconductor device in accordance with the first aspect of the invention, the height of the emitter contact 14 can be selected freely or matched to the process requirements of an optimized bipolar transistor. Eliminating the topology-induced restrictions on the height of the emitter contact 14 makes it possible to avoid the need to develop new contact hole etching techniques for bipolar components belonging to future technology platforms.

Fig. 4 illustrates the preferred embodiment of the semiconductor device according to the invention in accordance with the first aspect of the invention after the contact hole metallization has concluded. First of all, it is preferable for what is known as a liner, which consists, for example, of TiN and is used in particular as a diffusion stop, to be sputtered. Then, for example, tungsten is deposited, filling the contact holes 32 as a contact-hole filling material, for example by means of a MCVD process.

The process steps illustrated in Figs. 4 to 9 correspond to steps used in a conventional method for fabricating a semiconductor device as illustrated, for example, in Fig. 16. Therefore, in a conventional way, the electrically conductive contact-hole filling material is polished back to a target height by means of a planarization step (step: CMP W). The target height is in this case selected in such a manner that the emitter contact 14 (the second contact) is not opened up (cf. Fig. 5) and there are no residues of the filling material or liner outside the defined contact holes.

Then, to form the first patterned metal plane 34, a metal, which may, for example, be AlCu, is sputtered onto the semiconductor device (cf. Fig. 6; step: sputter metal 1). The layer thickness of this first metal plane 34 can be selected as a function of the design requirements and is typically approximately 400 nm.

A subsequent lithography and etching step (step: etch metal 1) is used to pattern the first metal plane 34 in such a manner that electrical conductors or connection contacts are formed in the first metal plane 34 above the contact holes 32, which are filled, for example, with tungsten. As illustrated in Fig. 7, all the (first) contacts 12, 16, 22, 24 and 26 are connected via contact holes to corresponding conductors, located above them in the substrate-normal direction, of the first metal plane 34. Only above the second contact 13, which in the present embodiment is the emitter contact, is there no conductor of the first metal plane 34 arranged above the contact 14 in the substrate-normal direction.

This is followed, in a deposition step, by the application of a further dielectric or insulator (step: deposit ILD1 (interlayer dielectric 1)). Fig. 8 shows the semiconductor device after this deposition step has ended. Then, the dielectric which has previously been deposited is polished back to a target height by means of a further polishing step (step: CMP ILD1) (cf. Fig. 9).

Next, in the same way as for the step of patterning the insulator layer 30 explained with reference to Fig. 3, a lithography and etching step is used to introduce contact holes 38 into the dielectric 36 (ILD) (step: etch VIA1). Unlike in a conventional fabrication method, for example for a semiconductor device as shown in Fig. 16, however, not only the contact holes 38

which end at conductors of the first metal plane 34, but also a contact hole 38 which ends at the contact surface of the emitter contact 14 (of the second contact) are patterned.

A window leading to the emitter contact 14 is therefore preferably only opened up during the patterning of what are known as the VIA-1 connecting channels, which are standard means of connecting conductors of the first metal plane 34 to conductors of the second metal plane 40. Consequently, unlike in the prior art, contact is made with the emitter contact 14 preferably via a VIA1 contact hole connection to the second metallization plane.

Then, in a similar way to the metallization step described with reference to Fig. 4, the contact holes 38 are filled with an electrically conductive contact-filling material. Once again, first of all a liner (TiN) is sputtered on as a diffusion stop (step: sputter liner). Next, a suitable metal (for example tungsten) is deposited by means of a MCVD process (step MCVD W; cf. Fig. 11), and this metal is polished back to a target height by means of a further planar polishing step (step: CMP W; cf. Fig. 12). The second metal plane 40 is patterned in the same way as the patterning of the first metal plane 34 which was described with reference to Figs. 6 and 7.

The preferred embodiment of the semiconductor device in accordance with the first aspect of the invention after the method steps of the invention have ended is illustrated in Fig. 14. As has already been explained in detail above, this semiconductor device differs from a known semiconductor device illustrated in Fig. 16 in particular through the fact that the second contact 14 (in this embodiment the emitter contact) is not connected to a conductor of the first metal plane 34 by means of a filled contact hole 32, but rather is

directly connected to the second metallization plane 40, preferably via what is known as the VIA-1 connecting contact. There is no conductor belonging to the first metal plane 34 arranged between the contact surface of the second contact 14 and the conductor of the second metallization plane 40, which is arranged above the contact 14 in the substrate-normal direction.

Since the so-called VIA-1 connecting contact, which is a standard means of connecting conductors of the first metal plane to conductors of the second metal plane, must in any case be formed in a standard process, making contact with the second contact 14 via the second metal plane 40 does not entail additional process steps. Accordingly, the VIA-1 etching above the contact 14 is not stopped by a conductor of the first metal plane, but rather ends at the polysilicon of the emitter contact 14. Therefore, the liners which can be used as an etching stop are broken through into the first metal plane 34 or the polysilicon of the emitter contact 14 in a simultaneous, controlled manner.

Fig. 15 shows a semiconductor device in accordance with the second aspect of the invention after the fabrication method steps of the invention have ended. The semiconductor device has a substrate 80, which may be a silicon semiconductor substrate, with a process surface 80'. The active components which have been patterned in the FEOL process steps may, for example, correspond to those of the preferred embodiment of the semiconductor device in accordance with the first aspect of the invention which has been described above.

In the preferred embodiment illustrated in Fig. 15, there is a bipolar transistor 100 with a base contact 120 (first contact), an emitter contact 140, which forms the second (higher) contact, and a collector contact 160 (first contact). The bipolar transistor 100 may, for example, be part of a radio frequency circuit

of the semiconductor device. Furthermore, the embodiment of the semiconductor device illustrated in Fig. 15 has a CMOS circuit, which is represented in simplified form by a MOS transistor 200. The MOS transistor 200 comprises a source contact 220, a gate contact 240 consisting of polysilicon and a drain contact 260. The contacts 220, 240 and 260 are first contacts in the sense of the invention.

As has already been described in connection with Fig. 1, after the FEOL process end, the semiconductor device is covered with an insulator 300, which is, for example, BPSG (borophosphosilicate glass), for example by means of a CVD deposition process.

Unlike in the fabrication method in accordance with the first aspect of the invention and known fabrication methods, however, the subsequent planar polishing step (step: CMD BPSG) is carried out in such a manner that the insulator is polished back as far as the second contact (i.e. the emitter contact 140). The CMP process step is therefore stopped at the emitter contact 140. In a known manner, an end point detection system, which indicates the instant at which the polishing step reaches the second contact 140, may be used for this purpose. It is also possible to provide additional auxiliary structures which function as a polishing stop.

As has already been described in detail with reference to Figs. 3 to 5, contact holes 320 are then patterned in the insulator 300 by means of a lithography step and an etching step (step: CT etch). However, unlike in the case of a conventional semiconductor device as shown in Fig. 16, a contact hole 320 is not formed above the emitter contact 140. The contact holes 320 can be lined in the usual way with a liner (for example consisting of TiN) and filled with a suitable contact-hole filling material, for example tungsten. The metal layer which

has been applied, for example, using a MCVD process is polished back, in a subsequent planar polishing step (CMP W), to a target height which is such that the contact surface of the emitter contact 140 (of the second contact) is uncovered. This means that the step of polishing the contact-hole filling material of the contact holes 320 can also be used to open up (and eliminate liner residues from) the contact surface of the second contact 140.

This is followed by definition of the (first) patterned metal plane 340, the process steps of which are no different from a conventional standard process for defining metal planes of this type. It should be noted that a conductor of the metal plane 340 which is arranged above the second contact 140 in the substrate-normal direction directly adjoins this second contact, so that an electrically conductive connection is produced between the second contact 140 (the emitter contact) and the corresponding (second) conductor of the metal plane 340. In other words, the second contact 140, unlike the other contacts of the semiconductor device, is not connected to the associated second conductor of the metal plane 340 by a contact-hole pin 320. Instead, contact is made with the second contact 140 directly by means of conductors of the first metal plane 340 which adjoin it. A thin, in particular metallic interlayer may be present between the second contact and the second conductor of the metal plane 340, for example in order to reduce the contact resistance.

An advantage of this fabrication method and/or of the semiconductor device which is thereby obtained is that the height of the second contact 140 can be selected as desired in the substrate-normal direction and/or can be matched to the process requirements of an optimized bipolar transistor. There is no need for thickness measurement by means of STI. At the same time, the

uncertainty in the measurement of the layer thickness of the insulator 300 (the BPSG layer) following the CMP BPSG polishing step (which amounts to ± 150 nm) is reduced and the risk of over-polishing is minimized or eliminated. There is no need to make contact with the second contact by means of a contact hole 320 filled with contact-hole filling material (for example tungsten). The first metal plane 340 can be connected to the emitter contact 140 directly (without the need for contact hole pins 320).

The limitation of the contact surface area, i.e. the diameter of the contact holes 320, is eliminated, since the entire effective surface area of the second contact 140 can be used to produce a contact. This means that higher current intensities can be realized in the bipolar transistor 100 and/or optimally matched to the surface area of the emitter contact 140.

List of reference symbols

For the preferred embodiment in accordance with the first aspect of the invention and the prior art:

8	Substrate (e.g. silicon semiconductor substrate)
8'	Process surface of the substrate 8
10	Bipolar transistor
12	Base contact of the bipolar transistor
14	Emitter contact (emitter stack) of the bipolar transistor
16	Collector contact of the bipolar transistor
20	MOS transistor
22	Drain contact of the MOS transistor
24	Gate contact of the MOS transistor
26	Source contact of the MOS transistor
30	Insulator (e.g. BPSG)
32	Contact hole (CT) filled with contact-hole filling material (e.g. W)
34	Patterned first metal plane with conductors
36	Dielectric (insulator) ILD (e.g. TEOS)
38	Contact hole (VIA-1) filled with contact-hole filling material
40	Patterned second metal plane with conductors

For the preferred embodiment in accordance with the second aspect of the invention:

80	Substrate (e.g. silicon semiconductor substrate)
80'	Process surface of the substrate 80
100	Bipolar transistor
120	Base contact of the bipolar transistor
140	Emitter contact (emitter stack) of the bipolar transistor
160	Collector contact of the bipolar transistor
200	MOS transistor
220	Drain contact of the MOS transistor
240	Gate contact of the MOS transistor
260	Source contact of the MOS transistor
300	Insulator (e.g. BPSG)

320 Contact hole (CT) filled with contact-hole filling material (e.g. W)

340 Patterned first metal plane with conductors

Claims

1. Semiconductor device, having
- a substrate (8), the process surface (8') of which has a substrate-normal direction;
- at least a first contact (12, 16, 22, 24, 26) and a second contact (14) arranged on the substrate, a contact surface of the second contact (14) being at a greater distance, in the substrate-normal direction, from the substrate (8) than a contact surface of the first contact (12, 16, 22, 24, 26); and
- at least a first (34) and a second (40) patterned metal plane, in each of which at least one conductor, which is electrically connected to at least one of the contacts, is formed;

the second metal plane (40) being at a greater distance, in the substrate-normal direction, from the substrate (8) than the first metal plane (34),
the second contact (14) being electrically connected to a conductor, located above it in the substrate-normal direction, of the second metal plane (40) without a conductor of the first metal plane (34) being connected in between, and
the first contact (12, 16, 22, 24, 26) being electrically connected to a conductor, located above it in the substrate-normal direction, of the second metal plane (34) via an interposition of a conductor, located above the first contact in the substrate-normal direction, of the first metal plane (34).

2. Semiconductor device according to Claim 1, in which the second contact (14) is an emitter contact of a bipolar transistor (10), and the first contact is a base contact (12) or collector contact (16) of a bipolar transistor or is a source contact (22), gate contact (24) or drain contact (26) of an MOS transistor (20).

3. Semiconductor device according to Claim 1 or 2, in which the first contact (12, 16, 22, 24, 26) is connected to the conductor of the first metal plane (34) via a contact hole (32) which extends in the substrate-normal direction and is filled with an electrically conductive contact-hole filling material.

4. Semiconductor device according to one of the preceding claims, in which the second contact (14) is connected to the conductor of the second metal plane (40) via a contact hole (38), which extends in the substrate-normal direction and is filled with an electrically conductive contact-hole filling material, without a conductor of the first metal plane (34) being connected in between.

5. Method for fabricating a semiconductor device, comprising the steps of:

- providing a substrate (8), the process surface (8') of which has a substrate-normal direction;
- defining at least a first contact (12, 16, 22, 24, 26) and a second contact (14) on the substrate (8), a contact surface of the second contact (14) being located at a greater distance, in the substrate-normal direction from the substrate (8) than a contact surface of the first contact (12, 16, 22, 24, 26);
- electrically connecting the first contact (12, 16, 22, 24, 26) to a conductor, located above it in the substrate-normal direction, of a first patterned metal plane (34); and
- electrically connecting the second contact (14) to a conductor, located above it in the substrate-normal direction, of a second patterned metal plane (40) without a conductor of the first metal plane (34) being connected in between;

the second metal plane (40) being at a greater distance, in the substrate-normal direction, from the

substrate (8) than the first metal plane (34), characterized in that
at the same time as the step of electrically connecting the second contact (14) to the conductor of the second metal plane (40), at least one conductor of the first metal plane (34) is connected to a conductor of the second metal plane (40) such that the first contact (12, 16, 22, 24, 26) is electrically connected to said conductor, located above it in the substrate-normal direction, of the second metal plane (34) via an interposition of the conductor, located above the first contact in the substrate-normal direction, of the first metal plane (34).

6. Process according to Claim 5, in which the second contact (14) is an emitter contact of a bipolar transistor (10), and the first contact is a base contact (12) or collector contact (16) of a bipolar transistor or is a source contact (22), gate contact (24) or drain contact (26) of an MOS transistor (20).

7. Method according to Claim 5 or 6, in which the step of electrically connecting the first contact (12, 16, 22, 24, 26) comprises the following steps:

- defining a contact hole (32), which ends at the first contact (12, 16, 22, 24, 26) and extends in the substrate-normal direction, in an insulator (30);
- filling the contact hole (32) with an electrically conductive contact-hole filling material; and
- defining the conductor, which lies above the first contact (12, 16, 22, 24, 26) in the substrate-normal direction, of the first metal plane (34) in such a manner that it is electrically connected to the contact-hole filling material.

8. Method according to one of Claims 5 to 7, in which the step of electrically connecting the second contact (14) comprises the following steps:

- defining a contact hole (38), which ends at the second contact (14) and extends in the substrate-normal direction, in an insulator (36);
- filling the contact hole (38) with an electrically conductive contact-hole filling material; and
- defining the conductor, which lies above the second contact (14) in the substrate-normal direction, of the second metal plane (40) in such a manner that it is electrically connected to the contact-hole filling material without a conductor of the first metal plane (34) being connected in between.