

1070.742



PATENT SPECIFICATION

DRAWINGS ATTACHED

1070.742

Date of Application and filing Complete Specification: March 4, 1964.

No. 9277/64.

Application made in United States of America (No. 270,749) on April 4, 1963.

Application made in United States of America (No. 273,187) on April 15, 1963.

Complete Specification Published: June 1, 1967.

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Index at acceptance:—H1 K(1A1, 1CX, 2S1A, 2S2A, 2S3, 2S8, 2S13, 2S14, 2S18, 2S23, 2S27, 3G, 4C21, 4F1A, 4F11G, 4F18, 4F19, 4F22, 4F27, 5C5, 8M, 8V); C7 F(1V2, 2Z3, 2Z11, 4X); H1 C(38Y, 46Y, 47Y, 315, 317, 323, 384, 472, 742)

Int. CL:—H 02 I 7/34 // C 23 c, H 01 s

COMPLETE SPECIFICATION

Diffusable Substrates and Diffusion Processes

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organized according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to the preparation of substrates of semiconductor material generally and to diffusion processes in conjunction therewith, in particular as appertaining to techniques for surface protection and control of semiconductors, especially compound semiconductors, during diffusion. This invention has particular application to compound semiconductor diffusion substrates and the processing of such substrates to fabricate various compound semiconductor devices and networks.

Problems can arise in the processing of compound semiconductors due to deterioration of the material caused by volatilization of one of the constituents at certain temperatures accompanied by the release of this constituent from the semiconductor compound, resulting in a change of the physical or chemical properties of the material.

Many of the compound semiconductors, and particularly the Group III—V compound semiconductors, and more specifically gallium arsenide, indium arsenide and lead telluride, are compounds in which at least one of the elements is relatively volatile in the temperature range over which vapour-solid diffusion may be achieved and when the semiconductor is heated to effect diffusion therein, sublimation of the volatile element or elements causes deterioration at the surface of the semiconductor. This sublimation and the accompanying surface deterioration also occur at temperatures sufficient for thermal conversion of the

surface of the semiconductor to an oxide layer.

Previous workers have attempted to avoid the volatility problem resulting in deterioration of compound semiconductors by utilising sealed ampoules for vapour-solid diffusion wherein the impurity sources is maintained at a temperature appropriate to control its vapour pressure and the substrate is maintained at a temperature appropriate for diffusion. Also attempts have been made to achieve vapour-solid diffusion by maintaining an ampoule containing the substrate and impurity at a uniform, diffusion temperature. Such techniques have had only limited success due to the fact that surface deterioration still occurs and the control over the diffusant and surface concentrations of diffusants remains difficult.

According to the present invention, a method of preparing a substrate of a compound semiconductor material which would suffer deterioration caused by volatilization of a portion thereof, includes the step of depositing a layer of oxide material on the surface of at least a portion of the substrate surface, the oxide layer having a thickness sufficient to prevent volatilization of the underlying semiconductor material. The oxide layer may for example be pyrolytically deposited on or, alternatively, sputtered onto, the semiconductor. The thickness of the oxide layer, while being adequate to prevent deterioration of the underlying substrate, can be made such as to permit diffusion of conductivity-affecting impurities into the substrate through the oxide layer.

The invention also provides a method of diffusing conductivity-affecting impurities into a substrate of semiconductor material, which may be a compound semiconductor material, in which prior to diffusion, there is deposited on the surface of at least a portion of the substrate a protective layer of an oxide material, the conductivity-affecting impurities then being diffused into the semiconductor

[Price 4s. 6d.]



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Source

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material through the said portion of the oxide layer. Alternatively, a protective layer of oxide material containing a controlled concentration of conductivity-affecting impurities can be deposited on the surface of at least a portion of the substrate. The oxide layer provides greater controllability of not only surface concentration of impurities but also the diffusion profile. Another advantage of the oxide deposit is that it affords vapour-solid diffusion into a compound semiconductor in a sealed system, in a closed tube single-zone to two-zone diffusion system, or in an open tube diffusion system.

The oxide layer containing conductivity-affecting impurities may be formed by concurrently depositing an oxide material, e.g. an oxide of silicon, and conductivity-affecting impurities. Preferably, the oxide layer has a differential thickness over the substrate surface, being adequately thick in selected regions to prevent deterioration of the underlying semiconductor yet permit diffusion of conductivity-affecting impurities into the substrate, and being sufficiently thick in other regions to prevent both deterioration and diffusion.

An oxide of silicon material has been found particularly suitable for use in forming the protective layer in methods embodying the invention. In a particular embodiment, an oxide of silicon layer containing conductivity-affecting impurities may be formed over part of the portion of the semiconductor, a layer of an oxide of silicon being formed over the remaining parts of that portion. The oxide of silicon layer containing the conductivity-affecting impurities may also be overcoated with another oxide of silicon layer devoid of conductivity-affecting impurities. Thus, various compound semiconductor integrated circuit devices containing, for example, resistive and capacitive regions, ohmic interconnections, transistors and diodes, may be fabricated by depositing the oxides of silicon containing the appropriate impurities therein over the regions wherein the various devices will be fabricated. Likewise, various diodes, transistors, or other active devices can also be fabricated by the technique of this invention.

By way of example, the invention will be described in greater detail with reference to the accompanying drawings, in which:—

Fig. 1 depicts apparatus suitable for depositing an oxide of silicon-coating on the surface of a compound semiconductor,

Fig. 2 depicts apparatus suitable for reactive sputtering a silicon dioxide coating over a compound semiconductor wafer sufficiently thick to prevent surface deterioration during diffusion,

Fig. 3 illustrates a compound semiconductor wafer that has been partially coated with an oxide of silicon surface protecting film which has been exposed to an environment for diffusion of an im-

purity into said compound semiconductor wafer,

Fig. 4 illustrates the sealed tube process for diffusing the compound semiconductors, Fig. 5 depicts apparatus for open tube diffusion of impurities into a compound semiconductor through an oxide of silicon coating,

Figs. 6, 7, 8 and 9 depict a series of typical diffusion curves for a compound semiconductor with and without a protective silicon dioxide coating thereover,

Fig. 10 depicts a compound semiconductor wafer after diffusion in accordance with the invention,

Fig. 11 depicts a mesa transistor made in accordance with the invention,

Fig. 12 depicts diffusion of a planar p-n junction using a differential depth silicon oxide layer,

Fig. 13 illustrates the impurity distribution of zinc concentration vs. depth for different time functions,

Fig. 14 illustrates the junction capacitance vs. voltage values,

Figs. 15 a—e illustrate the various stages of fabrication for a planar compound semiconductor diode according to the invention, and

Figs. 16 a—c depict the various stages of fabrication for a mesa diode according to the invention.

Referring specifically to Fig. 1, a system is depicted suitable for depositing an oxide of silicon on a compound semiconductor substrate. In the vapour flow process system illustrated, a single-zone furnace 1 supports a deposition tube 2 therein. Tube 2 may be made of quartz or other suitable material. A boat or support 3 provided within tube 2 supports semiconductor substrates 4 which are to be coated with an oxide of silicon. A cap exhaust 6 is provided on one end of tube 2 and allows discharge of spent reactants and products thereof. At its other end, tube 2 has an inlet region 7. A container 8 is provided which holds a liquid 9 which may be tetraethoxysilane or any other suitable organic oxysilane. A carrier gas inlet 10, extending below the surface of liquid 9, furnishes a controllable amount of a carrier gas, such as oxygen, into container 8 to entrain liquid 9. An outlet pipe 11, couples the carrier gas into the reaction tube 2. Interposing outlet pipe 11 are an inlet 12 to provide oxygen entry for dilution of the carrier gas and an inlet valve 13 to provide pure nitrogen or other inert gas entry to the system.

The operation of the oxide of silicon vapour flow deposition apparatus illustrated in Fig. 1 is as follows. Liquid tetraethoxysilane — TEOS — is maintained at normal room temperature. Oxygen at a flow rate of one-half cubic foot per hour (at standard conditions) entering inlet 10 bubbles through and entrains TEOS, passing into outlet pipe 11. Oxygen

dilution is obtained by injecting one cubic foot per hour (at standard conditions) of oxygen into pipe 11 via inlet 12. Nitrogen flow (during initial heating) is shut-off and therefore reactants are introduced into the quartz reactor 2. Previously, a quartz boat 3 with the compound semiconductor slices 4 to be coated had been placed in the reaction zone where the slices are to be subjected to the reactant stream. With the reaction temperature being held at 500°C, 2,300 angstroms per hour of the oxide of silicon is formed on the slices. The spent process stream is exhausted via cap exhaust 6.

In Fig. 2 is depicted the preferred embodiment of depositing silicon dioxide by reactive sputtering on to the compound semiconductor wafers. The apparatus consists of a silicon cathode 50 having a tab 51. The cathode is positioned on an insulating base 52 such that tab 51 protrudes into an opening provided in insulating base 52. The insulating base is mounted by any suitable means in a fixed position. Immediately above cathode 50 is a sample holder 53 which contains on its under-surface a series of clips 54 for retaining a compound semiconductor substrate 55. Sample holder 53 is a circular plate mounted to a rotatable shaft 56 journaled in bearing and support housing 57. Shaft 56 mounts a gear sprocket 58 suitable to engage a chain drive (not illustrated). Support arm 59 mounts bearing housing support 57 to a suitable bracket (not illustrated) to adjustably maintain the compound semiconductor wafers at an adjustable fixed distance above cathode 50 and centered thereover. A high voltage supply 61 has its positive side attached to support arm 59 and is grounded. The negative side of the voltage supply 61 is attached to high voltage lead 62 containing a clip 63 which attaches to the tab 51 of the silicon cathode 50. High voltage lead 62 is shielded by a metallic sheath 64 which has a ground connection 66. Since the sputtering operation is performed in an oxygen atmosphere, the apparatus is suitably housed within a chamber (not illustrated) which permits a controlled environment.

Typical operating conditions for reactively sputtering approximately 1,000 angstroms per hour of silicon dioxide on to the compound semiconductor wafers is achieved under the following conditions. A gas pressure of 40 microns of oxygen is maintained as the environment for sputtering. The silicon cathode 50 is a less than 0.01 ohm — cm (arsenic doped) highly crystalline disc about 4 inches in diameter. The distance between the top surface of the silicon cathode and the bottom surface of the semiconductor slice holder is about 1.25 inches. When an impurity-containing film is desired, an impurity cathode 68 is placed on the silicon cathode 50. A negative voltage of about 1500 volts d.c. is applied to the silicon cathode and develops a current of about 40 milliamps. The slice holder 53 is rotated at

approximately 50 r.p.m. The compound semiconductor slices under the applied voltage reach a temperature of about 200°C in approximately 20 minutes and remain relatively constant thereafter. During the first 30 minutes of sputtering, the slice is shielded to prevent deposition of the oxide thus permitting cleaning of the cathode prior to actual sputtering of the silicon dioxide film on to the compound semiconductor wafer. The dielectric constant of silicon dioxide films deposited in accordance with the above technique has been measured to be 3.54 as compared to fused silica of 3.78.

Fig. 3 depicts a compound semiconductor wafer 80 having an oxide of silicon layer 81 (the oxide of silicon being deposited as reactively sputtered SiO_2 or other deposition techniques) which covers only a portion of the wafer 80. Under diffusion of an impurity thereinto, wafer 80, as depicted at the left portion, has suffered deterioration and has a non-uniform diffusion interface 82 under the area of the wafer not having the surface protection of layer 81, whereas, under the surface protection of layer 81 deterioration has not occurred, and wafer 80 has a uniform flat diffusion interface 83. Hence, it will be appreciated that the layer 81 afforded surface protection during diffusion, preventing occurrence of an erratic diffusion interface attributable to loss of the volatile constituent from the compound semiconductor surface.

A description of open tube and closed tube diffusion of impurities into compound semiconductor wafers follows with specific reference to the apparatus in Figs. 4 and 5 and the diffusion impurity characteristic depicted in Figs. 6—9.

The closed or sealed tube diffusion apparatus (Fig. 4) consists of a quartz ampoule or tube 100 having a restriction 102 therein. A seal 103 is made after insertion of the substrate 104 with oxide of silicon layer 105 thereon and after insertion of impurity carrier material 106. Ampoule 100 has a break-off sealing tip 107 which is coupled to an evacuation system to decrease the pressure within tube 100 to about 10^{-8} Torr, and then the ampoule 100 is sealed. Ampoule 100 is at this stage ready to be inserted in a furnace to provide diffusion of the impurity contained in carrier material 106 into wafer 104. The furnace provides a uniform temperature throughout ampoule 100 at any desired diffusion temperature. The oxide of silicon layer 105 provides deterioration-preventing surface protection of the wafer allowing a uniform diffusion interface similar to that depicted as interface 83 in Fig. 3, notwithstanding diffusion temperatures maintained just below the melting point of the compound semiconductor wafers.

The open tube diffusion apparatus (Fig. 5) consists of a quartz reaction tube 120 fitted with an exhaust cap 121 and an inlet cap 122. A diffusion furnace 125 (schematically illus-

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 SiO_2

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100

105

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115

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125

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trated) surrounds a portion of tube 120 to provide a diffusion region therein. A vapour pressure control furnace 126 (schematically illustrated) surrounds another portion of tube 120 to provide an impurity vapour control zone therein. Within the diffusion region of the tube 120, a quartz boat 123 is provided to hold wafers 124 during diffusion. An impurity boat 127 is positioned within the vapour control zone of tube 120 to hold an impurity source 128. To obtain a controlled flow of impurity vapour into the diffusion zone of tube 120, an inert or forming gas ambient is provided. The source of gas 129 is coupled by a valve 130 and pipe 131 to flow meter 132. Pipe 133 provides a flow path from meter 132 to introduce gas from source 129 into reactor tube 120.

Figs. 6—9 depict zinc impurity concentrations at various depths in gallium arsenide wafers that were exposed to zinc vapours in a closed tube diffusion process at a temperature of 1000°C for various periods of time, some with and others without the surface protection afforded by a sputtered silicon dioxide layer 6500 Å thick, the layer being achieved by the process heretofore described with reference to Fig. 2. In Fig. 6, curves A and B represent

the zinc concentrations achieved by 2 and 4 hour periods of diffusion, respectively, in an ambient of about 0.1 atmosphere of zinc. In Fig. 7, curves C and D, respectively, represent the zinc concentrations achieved in silicon dioxide protected and unprotected gallium arsenide wafers after 18 hours of diffusion in an ambient of about 0.01 atmosphere of zinc. Curves E and F of Fig. 8 and curves G and H of Fig. 9 illustrate a further comparison of zinc concentrations achieved under various conditions of diffusion in gallium arsenide. The curves F and H relate to wafers which were not protected with silicon dioxide.

Table I appearing hereinafter details the various characteristics of the crystal and protective layer thereover used in the closed or sealed tube diffusion of zinc into gallium arsenide among others. Some examples include the compound semiconductor unprotected with the sputtered silicon dioxide film or other oxide of silicon layer. The examples are identified with the curves A—H of Figs. 6—9. Table II appearing immediately following Table I gives the diffusion conditions and results achieved by diffusion for the examples set forth in Table I, example numbers in both tables corresponding to one another.

TABLE I

Example		Crystal Data			Protective Film	
No.	Figs. 6—9 Curve	Material	Impurity *Conc. Carriers/cc	**Cond. Type	Type	Thickness Å
1	A	GaAs	1×10^{17}	N	SiO ₂	6500
2	B	GaAs	1×10^{17}	N	SiO ₂	6500
3	C	GaAs	1×10^{17}	N	SiO ₂	6500
4	D	GaAs	1×10^{17}	N	None	—
5	E	GaAs	1×10^{17}	N	SiO ₂	6500
6	F	GaAs	1×10^{17}	N	None	—
7	G	GaAs	1×10^{17}	N	SiO ₂	6500
8	H	GaAs	1×10^{17}	N	None	—
9	—	GaAs	1×10^{17}	N	SiO ₂	6500
10	—	GaAs	1×10^{17}	N	None	—
11	—	InAs	1×10^{17}	N	SiO ₂	4000
12	—	PbTe	—	N	SiO ₂	4500
13	—	PbTe	—	N	SiO ₂	4500

*Concentration

**Conductivity

TABLE II

Example No.	Diffusant		Diffusion		Results of Diffusion		
	Source	Zinc Pressure in Atm	Temp °C	Time Hours	Surface Appearance	Junction Depth X_j Microns	Surface Concentration (C_0) Atom/cc
1	Zn	0.1	1000	2	No Decadence	40	3×10^{19}
2	Zn	0.1	1000	4	No Decadence	54	3×10^{19}
3	1%Zn ⁽¹⁾	0.01	1000	18	No Decadence	10	3×10^{18}
4	1%Zn ⁽¹⁾	0.01	1000	18	Decadence	47	1.5×10^{19}
5	0.1%Zn ⁽¹⁾	0.001	1000	18	No Decadence	3.5	5×10^{17}
6	0.1%Zn ⁽¹⁾	0.001	1000	18	Decadence	14	2.5×10^{17}
7	0.01%Zn ⁽¹⁾	0.0001	1000	18	No Decadence	0	10^{17}
8	0.01%Zn ⁽¹⁾	0.0001	1000	18	Decadence	11	10^{18}
9	Zn	0.1	1000	18	No Decadence	—	3×10^{19}
10	Zn	0.1	1000	18	Decadence	—	—
11	Zn	—	800	1	No Decadence	5.1	—
12	None	—	800	1	No Decadence ⁽²⁾	—	—
13	Fe 50Mg	—	800	1	No Decadence ⁽²⁾	(3)	—

⁽¹⁾ Percent zinc refers to atomic % of zinc in a gallium-zinc alloy.

⁽²⁾ Unprotected regions suffered severe decadence.

⁽³⁾ A diffused layer or region was achieved.

The data presented in Table III, hereinafter, provides details of the open tube diffusion process with both vapour flow oxide of silicon (TEOS deposit) and sputtered silicon dioxide processes to obtain the protective layer. The carrier gas used in the open tube diffusion was Forming Gas (5–10% H_2 in N_2) at a flow rate of 500 cc per min. In all the examples given, gallium arsenide was the

compound semiconductor undergoing diffusion. As the impurity source, about 10 grams of zinc having an exposed molten surface area of about 10 sq. cm was used to maintain a constant zinc vapour pressure in the diffusion tube. In the examples given, diffusion was performed for two hours at the various diffusion conditions specified.

TABLE III

Example No.	N-Type Impurity Atom/cc	Protective Layer		Diffusion Conditions		Diffusion	Diffused
		Thickness Å	Type	Impurity Zone Temp °C	Diffusion Zone Temp °C	Depth Microinch	Surface Condition
1	5×10^{15}	500	SiO _x *	650	900	63	Good
2	5×10^{15}	500	SiO _x	700	700	40	Good
3	5×10^{15}	500	SiO _x	700	800	205	Good
4	5×10^{15}	500	SiO _x	800	800	250	Good
5	5×10^{15}	500	SiO _x	800	900	348	Good
6	5×10^{15}	500	SiO _x	800	1000	316***	Bad
7	5×10^{15}	500	SiO _x	900	900	316	Good
8	5×10^{15}	500	SiO _x	900	1000	378***	Bad
9	5×10^{16}	1500	SiO ₂ **	800	800	40	Good
10	5×10^{16}	1500	SiO ₂	800	900	47	Good
11	5×10^{16}	1500	SiO ₂	800	1000	111***	Bad
12	5×10^{16}	1500	SiO ₂	900	800	16	Good
13	5×10^{16}	1500	SiO ₂	900	900	32	Good
14	5×10^{16}	1500	SiO ₂	900	1000	111***	Bad
15	5×10^{16}	500	SiO _x	650	900	158	Good
16	5×10^{16}	500	SiO _x	700	800	205	Good
17	5×10^{16}	500	SiO _x	700	900	284	Bad
18	5×10^{16}	500	SiO _x	800	800	221	Good
19	5×10^{16}	500	SiO _x	800	900	300	Good
20	1×10^{17}	1100	SiO _x	700	700	40	Good
21	1×10^{17}	1100	SiO _x	700	800	40	Good
22	1×10^{17}	1100	SiO _x	700	900	95	Good
23	1×10^{17}	1100	SiO _x	700	1000	253***	Bad
24	1×10^{17}	1100	SiO _x	800	900	95	Good
25	1×10^{17}	1100	SiO _x	800	1000	190***	Bad
26	1×10^{17}	1100	SiO _x	700	700	40	Good
27	1×10^{17}	500	SiO _x	800	900	206	Good
28	1×10^{17}	500	SiO _x	900	900	158	Good

*The notation SiO_x refers to an oxide of silicon which may or may not be SiO₂.

**The notation SiO₂ refers to a reactively sputtered silicon dioxide layer.

***Surface pitting prevented accurate depth measurement.



Referring to Fig. 10, a typical compound semiconductor wafer appertaining to the invention is illustrated. The wafer 150 has an oxide of silicon protective layer 151 thereover. Typically after diffusion according to the invention, wafer 150 has a p-n junction 152 therein. The wafer 150 is used to form a semiconductor device. Fig. 11 depicts such a device as a mesa transistor generally designated by the reference numeral 180 and being made from a wafer similarly treated as wafer 150. As illustrated in Fig. 11, a gallium arsenide wafer 160 has an n-type conductivity region 161 with an ohmic contact 162 serving as the collector. The p-type region 163 was diffused therein, in accordance with the invention. An ohmic contact 164 attached to region 163 serves as the transistor base. An alloy contact 166 having a regrowth region 167 forms the

emitter of the transistor.

For purposes of evaluation, the transistors made according to the illustration in Fig. 11 had an ohmic collector contact of platinum connected to the GaAs wafer by an alloy of 99% gold and 1% selenium (by weight). The base contact was ohmic and made by an alloy of 96% gold and 4% zinc (by weight). The alloy emitter was made using an alloy of 62 wt.% gold and 38 wt.% tin; a gold wire was used for the emitter lead. In Table IV following, hereinafter, is recorded the betas and breakdown voltages with collector-to-base open (BV_{CBO}) for the mesa transistors fabricated. The example numbers in Table IV are correlated to the example numbers of the material in Table III from which the transistor was fabricated.

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TABLE IV

Example No.	Table III Example	BV_{CBO} Volts	β
1	4	40	5
2	4	40	4
3	4	40	1
4	5	40	5
5	5	40	4
6	5	40	1
7	17	21	3
8	17	21	2
9	19	20	4
10	19	20	3
11	19	20	2

The technique of making planar diffusions into compound semiconductors utilising the invention is presented hereafter with reference to Fig. 12. A compound semiconductor substrate 190 is coated with an oxide of silicon layer 191, which may be reactively sputtered silicon dioxide hereinbefore mentioned; sufficiently thick to prevent diffusion therethrough. A region 192 in layer 191 is provided which is sufficiently thin to permit diffusion therethrough. As illustrated in Fig. 12, a diffused region 193 is present and forms a planar junction. It will be appreciated that other planar devices may be made by diffusion techniques employing various regions of diffusion mask

and surface protection diffusion windows or openings in the oxide of silicon sufficiently thin for diffusion, yet sufficiently thick to prevent surface degradation. Several devices have been made using the differential depth oxide of silicon technique (one region of the oxide of silicon masking diffusion and another region permitting diffusion yet both regions preventing surface deterioration).

In making planar or other selectively diffused compound semiconductor devices, the oxide of silicon layer must be of differential depth so that for given diffusion conditions, a junction will be diffused into the substrate in some areas and not in other areas. It will be

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appreciated that for given diffusion rates the thickness of the oxide of silicon layer to prevent diffusion and deterioration of the compound semiconductor device may vary from less than 10,000 angstroms to more than 20,000 angstroms, whereas the oxide of silicon layer to permit diffusion and prevent deterioration of the compound semiconductor may vary from less than 500 angstroms to more than 10,000 angstroms. It will be understood that masking afforded by regions of the oxide of silicon layer is achieved since the time required for the impurities to diffuse through the layer is greater than the time diffusion is conducted. Hence, by using differential depth oxide of silicon layers for diffusion, both masking against diffusion and forming diffused region may be achieved concurrently in the compound semiconductor without decadence thereof.

Examples of gallium arsenide having differential depth silicon dioxide layers (formed by reactive sputtering under the conditions heretofore given) are presented as follows.

EXAMPLE I

A gallium arsenide wafer having 1×10^{17} atoms of tin per cubic centimetre had deposited thereon a differential depth layer of silicon dioxide, 5,000 angstroms over the region to be diffused and 25,000 angstroms over the region to be masked. Diffusion was performed in the sealed ampoule process (heretofore described) using 1% (atomic) zinc in a gallium zinc alloy as the diffusant source. After diffusion at 1000°C for 30 minutes, a p-n planar junction was formed 2 microns below the gallium arsenide surface. The 25,000 angstrom silicon dioxide layer completely masked the gallium arsenide thereunder from the diffusant.

EXAMPLE II

A second gallium arsenide wafer having 1×10^{17} atoms of tin per cubic centimetre had deposited thereover a differential depth layer of silicon dioxide, 1,000 angstroms over the region to be diffused and 13,000 angstroms over the region to be masked. Diffusion was performed in the sealed ampoule process (heretofore described) using 30 wt. percent manganese in a manganese-gallium alloy as the diffusant source. After diffusion at 1000°C for one hour, a planar p-n junction was formed 1.58 microns below the gallium arsenide surface. The 13,000 angstrom silicon dioxide layer completely masked the gallium arsenide thereunder from the diffusant.

From the foregoing, it will be appreciated that the invention provides a highly desirable diffusion process for various compound semiconductors. The oxide of silicon surface protection layer afforded by the invention permits excellent control of the various diffusion processes which may be employed without the potential danger of the compound semi-

conductor undergoing deterioration, particularly surface deterioration.

Furthermore, the invention provides not only protection of the compound semiconductor surface to avoid surface deterioration or decomposition but permits selective distribution of impurities into the compound semiconductor surface by including the desired impurity within the silicon oxide film.

Again referring to Fig. 2, silicon oxide films which contain conductivity-affecting impurities may be formed on the semiconductor substrate by the simultaneous sputtering of silicon and the desired impurity. For this purpose an impurity cathode 68 shown in phantom lines may be positioned on top of the silicon cathode 50. During the sputtering process a silicon oxide deposit or layer will be formed which has not only the desired surface protecting qualities, but also contains a small amount of impurity which may diffuse from the film into the semiconductor when the substrate is exposed to normal diffusion temperatures.

It will be appreciated that the impurity concentration in the silicon dioxide layer may be varied by varying the amount of exposed surface area of the silicon cathode 50 compared to the impurity cathode 68. The operation of the apparatus for sputtering silicon dioxide films containing zinc as an impurity on to a compound semiconductor substrate and in particular gallium arsenide was performed using a silicon cathode 3 inches in diameter and a zinc cathode 1/2 inch in diameter. The sputtering operation was conducted at 1800 volts d.c. with 60 milliamps of current and an oxygen pressure of 40 microns. The cathode to anode spacing was 1 inch, measured from sample holder 53 with respect to the silicon cathode 50.

In using the zinc and silicon cathodes under the reactive sputtering conditions set forth above, the zinc cathode has a disintegration rate of about 1/3 of a milligram per hour whereas the silicon cathode had a disintegration rate of about 4 milligrams per hour. These rates were essentially constant throughout the sputtering process.

It will be appreciated that there are various other techniques for controlling the amount of impurity incorporated into the silicon dioxide film, such as casting the silicon with a known, uniform amount of impurity therein or by diffusing impurities into the silicon cathode at a desired concentration level. Another relatively simple technique for depositing the silicon dioxide layer doped with a uniform, controlled concentration of impurities is to introduce a vapour or gaseous compound or elemental vapour stream of impurities into the oxygen stream as the ambient environment for the reactive sputtering. In this manner the impurity will be deposited concurrently with the silicon dioxide.

Inclusion of the impurity within the silicon oxide film permits even more versatile and simpler diffusion techniques. Referring again to Fig. 4, the impurity carrier material 106 may be eliminated from the closed tube diffusion process since the impurity is included within the silicon oxide layer 105. Therefore the size of the diffusion ampoule 100 may be significantly reduced.

The open tube diffusion apparatus (Fig. 5) may also be simplified. Where the wafers 124 have been coated with an impurity-containing film prior to diffusion, the impurity source 128 and the impurity boat 127 may be eliminated. Since diffusion of the impurity from the film into the wafer 124 is independent of the surrounding atmosphere, the vapour pressure control furnace 126 may also be eliminated.

Devices have been successfully fabricated from semiconductor substrates prepared by utilising the apparatus and process illustrated by Fig. 5 with the above modification.

In general in the examples presented in Table V following hereinafter, the sputtered film thicknesses ranged from 6700 to 7500 angstroms, and all diffusions out of the film were at 900°C in a flowing hydrogen or forming gas environment. Further, in Table V for purposes of illustration, gallium arsenide was the compound semiconductor utilised. It had n-type conductivity with a tin concentration of 10^{17} atoms/cc., having a resistivity of 0.015 to 0.02 ohm-cm. The silicon cathode was 0.01 ohm-cm arsenic doped. The impurity cathode was a zinc disc with a surface area of 1.82 square centimetre.

TABLE V

Example	Open Tube Diffusion		Crystal Data After Diffusion		Reverse Diode Break-down	Junction Depth (Mils)	N Power ⁽²⁾ of Junction Capacitance C_j , Equation
	Time ⁽¹⁾ (Hrs)	Atmosphere ($\frac{1}{2}$ l/min)	Sheet Resistance (Ω /sq)	Bulk Resistivity (Ω -cm)			
1 ⁽³⁾	3	Form. Gas	0.095—0.110	0.03	10V	0.075—0.10	
2 ⁽⁴⁾	3	Form. Gas	—	—	12V	0.095	
3	1	H ₂	44.3—56.0	0.04	15V	0.125	
4	1	H ₂	58.6—68.0	0.03	12	0.095	
5	1	H ₂	46.0—55.0	0.05	10V	0.125	
6	1	H ₂	58.6—68.0	0.02	12V	0.095	0.40—0.41
7	3	H ₂	—	—	—	0.088	
8	3	H ₂	—	—	—	0.080	
9 ⁽⁶⁾	2@900°C; cooled to 400°C over 2½ hr period	H ₂	55.0—65.0	0.03	15V	0.125	
10	24	H ₂	54.6—67.9	0.06	15—20V	0.182	0.40
11 ⁽⁹⁾	32	H ₂	56.1	0.036—0.042	15V	0.222	0.36—0.37
12	32	H ₂	53.3—58.4	0.037—0.044	15V	0.220	
13	1	H ₂	33.5—32.25	0.034—0.037	—	0.125	

TABLE V—cont.

Example	Open Tube Diffusion		Crystal Data After Diffusion		Reverse Diode Break-down	Junction Depth (Mils)	N Power ⁽²⁾ of Junction Capacitance C_j , Equation
	Time ⁽¹⁾ (Hrs)	Atmosphere ($\frac{1}{2}$ l/min)	Sheet Resistance (Ω/sq)	Bulk Resistivity ($\Omega\text{-cm}$)			
14	1/2	H ₂	37.0—39.0	0.005—0.006	—	0.120	
15	1/4	H ₂	42.5—49.1	0.014—0.02	—	0.1	
16	5 min.	H ₂	90.0—97.0	0.02—0.03	—	—	

(1) Samples except as otherwise noted were maintained at 900°C for period specified.

(2) Junction capacitance equation is $C_j = A [V - V_d]^{-n}$ where A is a constant, V is the applied bias voltage V_d is the barrier potential and n is a power between 0.5 and 0.33.

(3) For one sample slice of this crystal, processed concurrently with the example slice reported herein, the over-all variation of junction depth was determined by measuring junction depths in four quadrants of sample. In the first quadrant four readings were 0.098 mils; in the second quadrant four readings were 0.088 mils; in the third quadrant six readings ranged from 0.098 to 0.12 mils; and in the fourth quadrant two readings were 0.088 mils; the readings indicating insignificant variations within the accuracy of the measuring technique.

(4) A transistor made from this crystal had a beta of $2\frac{1}{2}$.

(5) A transistor made from this crystal had a beta of $1\frac{1}{2}$.

(6) Both mesa diodes and lasers were made from this crystal as later described.

The distribution of zinc impurity as a function of time of diffusion out of the silicon dioxide film is illustrated in Fig. 13. The abscissa represents depth from the surface of the semiconductor wafer and the ordinate represents the zinc concentration in relative proportions. For example, after approximately 15 minutes of diffusion, curve A would be illustrative of the impurity concentration distribution, whereas after a varying number of hours up to about 40, curves B, C, D and E, respectively, would be typical of the impurity concentration distribution in the semiconductor wafer.

Considering the curves in Fig. 13 in conjunction with Table V, it will be noted that sheet resistance, except for very short diffusions, remains essentially constant regardless of depth. Thus, it would be established that only a given quantity of impurity (zinc) is available for diffusion. The behaviour could be described by a Gaussian distribution except for curve A which exhibits the concentration dependent diffusion coefficient of zinc. The effect of these

combined factors is that short periods of diffusion (15 minutes to 3 hours) produce junction depths approximately the same. Longer diffusion approximates the Gaussian distribution. Diffusion times of 15 minutes and under produce degenerate P type layers (tunnel diodes have been made thereby).

Further substantiating the distribution, with reference to Fig. 14, the junction capacitance for the various crystals in Table V was determined. The value of n should be 0.5 for an abrupt junction and 0.33 for a graded junction. Curves BB—FF in Fig. 14 illustrate the change in distribution of zinc impurities from abrupt to graded with increased diffusion time.

Laser devices were made from a slice of the crystal next to the slice in example 11 by the usual sealed ampoule diffusion (with no surface protection for the wafer). The ampoule was evacuated and sealed with elemental zinc and a wafer about 1 inch diameter and 20 mils thick. The diffusion was at 915°C for $2\frac{1}{2}$ minutes. The junction depth was about 0.3 mil and was irregular. The diffused crystal

5 slice of example 11 having a 0.222 mil junction was made into laser devices. In each case the crystal slices were cut into 20 × 20 mil wafers and fabricated. The characteristics of current threshold and current density for the laser devices are compared in Table VI hereinafter. These devices were made according to the usual laser fabrication process of cutting on the 110 plane and making ohmic contacts

on opposed sides of the junction. Lasers 10 numbers 1 to 7 were made from the gallium arsenide diffusion substrates of the invention which contained impurities in the silicon dioxide coating, whereas lasers 8 to 6 were made by diffusing elemental zinc into a gallium 15 arsenide wafer in a closed tube system with no surface protection.

TABLE VI

Laser Number	Current Threshold Amp	Current Density Amp/cm ²
1	54	20,930
2	38	14,728
3	30	11,638
4	40	15,503
5	54	20,930
6	160	62,015
7	100	38,759
8	350	135,659
9	220	85,271
10	140	54,263
11	370	143,410
12	290	112,403
13	250	96,899
14	200	77,519
15	280	108,529
16	230	89,147

Note: Current values were obtained at 78°K.

Referring to Figs. 15 a—e, a compound semiconductor planar diode construction is depicted. A compound semiconductor wafer 200 with a conductivity-affecting impurity containing silicon dioxide layer 201 (Fig. 15a) was processed by KMER-mask technique to form a reduced layer 203 on wafer 200 (Fig. 15b). Next a pure silicon dioxide layer 204 was deposited over the unprotected wafer 200 and the silicon dioxide layer 203 (Fig. 15c). The wafer 200 then was diffused in the apparatus depicted in Fig. 5 (as modified above) under suitable temperature and inert or reducing flowing ambient to form diffused region 206 of opposite-type conductivity than

wafer 200 (Fig. 15d). A hole was then made in silicon dioxide layers 203 and 204, and an ohmic contact 207 was formed therein by evaporation techniques (Fig. 15e). An ohmic base contact 208 was then formed on wafer 200 to complete the device. The devices, made as above, were operated successfully as diodes. 40

Referring to Figs. 16 a—c, the process of making a mesa diode according to the invention will be described. A compound semiconductor wafer 250 having a silicon dioxide layer 251 deposited thereover is provided (Fig. 16a). The layer 251 contains a uniformly distributed controlled concentration of impurities therein which, after diffusion, will impart



opposite-type conductivity to a region of wafer 250. The diffusion region 252 (Fig. 16b) is achieved by subjecting wafer 250 having layer 251 thereover to a diffusion environment such as provided by the apparatus depicted in Fig. 5 (as modified above) at a temperature appropriate for diffusion.

After diffusion, the mesa diode is fabricated by the usual mesa forming techniques. A suitable ohmic contact 253 is made to the diffused region 252, and a suitable ohmic contact 254 is made to the wafer 250 to complete the device (Fig. 16c).

The mesa diodes made from the crystal of example 11 in Table V, according to the above process, had 20 x 20 mil mesas with evaporated gold-zinc contacts on the P-layer (mesa surface) and gold-antimony on the n-region (wafer base).

Moreover, although the invention has been disclosed with respect to Group III-V and Group II-IV compound semiconductors, it will be readily apparent to those skilled in the art that other compound semiconductors having two or more elements could be processed in accordance with the invention.

WHAT WE CLAIM IS:—

1. A method of preparing a substrate of a compound semiconductor material which would suffer deterioration caused by volatilization of a portion thereof, including the step of depositing a layer of oxide material on the surface of at least a portion of the substrate surface, the oxide layer having a thickness sufficient to prevent volatilization of the underlying semiconductor material.

2. A method as claimed in claim 1, wherein said oxide layer is pyrolytically deposited on the semiconductor.

3. A method as claimed in claim 1, wherein said oxide layer is sputtered onto said semiconductor.

4. A method of diffusing conductivity-affecting impurities into a substrate of semiconductor material, including the steps of depositing on the surface of at least a portion of the substrate prior to diffusion a protective layer of an oxide material, and diffusing conductivity-affecting impurities into the semiconductor through the said portion of the oxide layer.

5. A method of diffusing conductivity-affecting impurities into a substrate of semiconductor material, including the steps of depositing on a surface of at least a portion of the substrate prior to diffusion a protective layer of oxide material containing a controlled concentration of conductivity-affecting impurities.

6. A method according to claim 4 or claim 5, in which the oxide material is an oxide of silicon.

7. A method according to claim 5, in which the said oxide layer is an oxide of silicon layer

not less than about 6500 Angstrom units thick.

8. A method as claimed in claim 5 or claim 7, including the step of applying another oxide layer devoid of conductivity-affecting impurities overlying the oxide layer containing the conductivity-affecting impurities and the remainder of the said surface portion of the semiconductor.

9. The method as claimed in claim 8, including the step of diffusing the conductivity-affecting impurities from the portion of the layer containing the conductivity-affecting impurities into the semiconductor to form a diffused zone therein.

10. The method as claimed in any one of claims 4-10, in which the or each oxide layer is formed by reactive sputtering.

11. The method as claimed in claim 5 or claim 7, including the step of concurrently depositing an oxide of silicon and conductivity-affecting impurities to form an oxide of silicon layer containing conductivity-affecting impurities.

12. The method as claimed in claim 11, wherein the oxide of silicon and the said impurities are concurrently deposited by reactive sputtering.

13. The method as claimed in any one of claims 5, 7, 11 and 12, and including the further step of effecting diffusion of the conductivity-affecting impurities from the oxide layer into the semiconductor.

14. The method as claimed in claim 13, in which the diffusion step produces at least one p-n junction in the semiconductor.

15. The method as claimed in claim 14, wherein the diffusion step produces a planar junction.

16. The method as claimed in claim 5 or in any one of claims 7-12, in which the oxide layer has a differential thickness, being sufficient to permit diffusion of conductivity-affecting impurities in selected regions and prevent such diffusion in other regions.

17. The method as claimed in claim 16, in which the semiconductor is of one conductivity type, in which the conductivity-affecting impurities are of a type appropriate to form p-n junctions in the semiconductor, and in which the regions of the oxide layer that permit diffusion through it are appropriate to formation of planar p-n junctions in the semiconductor.

18. The method as claimed in claim 5 or claim 7, in which an oxide of silicon layer containing conductivity-affecting impurities is formed over part of the portion of the semiconductor and a layer of an oxide of silicon is formed over the remaining parts of that portion.

19. The method as claimed in claim 18, in which the semiconductor is of one conductivity-type, in which the conductivity-affecting impurities are appropriate to formation of p-n junctions in the semiconductor,



opposite-type conductivity to a region of wafer 250. The diffusion region 252 (Fig. 16b) is achieved by subjecting wafer 250 having layer 251 thereover to a diffusion environment such as provided by the apparatus depicted in Fig. 5 (as modified above) at a temperature appropriate for diffusion.

After diffusion, the mesa diode is fabricated by the usual mesa forming techniques. A suitable ohmic contact 253 is made to the diffused region 252, and a suitable ohmic contact 254 is made to the wafer 250 to complete the device (Fig. 16c).

The mesa diodes made from the crystal of example 11 in Table V, according to the above process, had 20 × 20 mil mesas with evaporated gold-zinc contacts on the P-layer (mesa surface) and gold-antimony on the n-region (wafer base).

Moreover, although the invention has been disclosed with respect to Group III—V and Group II—IV compound semiconductors, it will be readily apparent to those skilled in the art that other compound semiconductors having two or more elements could be processed in accordance with the invention.

WHAT WE CLAIM IS:—

1. A method of preparing a substrate of a compound semiconductor material which would suffer deterioration caused by volatilization of a portion thereof, including the step of depositing a layer of oxide material on the surface of at least a portion of the substrate surface, the oxide layer having a thickness sufficient to prevent volatilization of the underlying semiconductor material.

2. A method as claimed in claim 1, wherein said oxide layer is pyrolytically deposited on the semiconductor.

3. A method as claimed in claim 1, wherein said oxide layer is sputtered onto said semiconductor.

4. A method of diffusing conductivity-affecting impurities into a substrate of semiconductor material, including the steps of depositing on the surface of at least a portion of the substrate prior to diffusion a protective layer of an oxide material, and diffusing conductivity-affecting impurities into the semiconductor through the said portion of the oxide layer.

5. A method of diffusing conductivity-affecting impurities into a substrate of semiconductor material, including the steps of depositing on a surface of at least a portion of the substrate prior to diffusion a protective layer of oxide material containing a controlled concentration of conductivity-affecting impurities.

6. A method according to claim 4 or claim 5, in which the oxide material is an oxide of silicon.

7. A method according to claim 5, in which the said oxide layer is an oxide of silicon layer

not less than about 6500 Angstrom units thick.

8. A method as claimed in claim 5 or claim 7, including the step of applying another oxide layer devoid of conductivity-affecting impurities overlying the oxide layer containing the conductivity-affecting impurities and the remainder of the said surface portion of the semi-conductor.

9. The method as claimed in claim 8, including the step of diffusing the conductivity-affecting impurities from the portion of the layer containing the conductivity-affecting impurities into the semiconductor to form a diffused zone therein.

10. The method as claimed in any one of claims 4—10, in which the or each oxide layer is formed by reactive sputtering.

11. The method as claimed in claim 5 or claim 7, including the step of concurrently depositing an oxide of silicon and conductivity-affecting impurities to form an oxide of silicon layer containing conductivity-affecting impurities.

12. The method as claimed in claim 11, wherein the oxide of silicon and the said impurities are concurrently deposited by reactive sputtering.

13. The method as claimed in any one of claims 5, 7, 11 and 12, and including the further step of effecting diffusion of the conductivity-affecting impurities from the oxide layer into the semiconductor.

14. The method as claimed in claim 13, in which the diffusion step produces at least one p—n junction in the semiconductor.

15. The method as claimed in claim 14, wherein the diffusion step produces a planar junction.

16. The method as claimed in claim 5 or in any one of claims 7—12, in which the oxide layer has a differential thickness, being sufficient to permit diffusion of conductivity-affecting impurities in selected regions and prevent such diffusion in other regions.

17. The method as claimed in claim 16, in which the semiconductor is of one conductivity type, in which the conductivity-affecting impurities are of a type appropriate to form p—n junctions in the semiconductor, and in which the regions of the oxide layer that permit diffusion through it are appropriate to formation of planar p—n junctions in the semiconductor.

18. The method as claimed in claim 5 or claim 7, in which an oxide of silicon layer containing conductivity-affecting impurities is formed over part of the portion of the semiconductor and a layer of an oxide of silicon is formed over the remaining parts of that portion.

19. The method as claimed in claim 18, in which the semiconductor is of one conductivity-type, in which the conductivity-affecting impurities are appropriate to formation of p—n junctions in the semiconductor,



and in which the regions of the oxide layer containing conductivity-affecting impurities are appropriate to the formation of planar p-n junctions in the semiconductor.

5 20. The method as claimed in any one of claims 4—19, in which the oxide layer is a silicon dioxide layer.

10 21. The method as claimed in claim 14, wherein the said semiconductor is gallium arsenide and one of the said diffused impurities that forms the junction is zinc.

22. The method as claimed in any one of claims 4—20, in which the semiconductor is a compound semiconductor.

15 23. The method as claimed in any one of claims 1—3, or as claimed in claim 22, wherein the said semiconductor is a Group III—V compound semiconductor.

20 24. The method as claimed in claim 23, in which the compound semiconductor is gallium arsenide, indium arsenide, indium antimonide or lead telluride.

25. The method as claimed in claim 1 or claim 4, in which the oxide layer is formed by passing a vapour of an organoxysilane and a carrier gas including oxygen over the substrate material and depositing therefrom an oxide of silicon layer onto the substrate.

26. A semiconductor body made by the method as claimed in any one of claims 1—3 or claim 25.

27. A Group III—V compound semiconductor body when tested by the method as claimed in any one of claims 4—21.

28. A semiconductor body made by the method described herein with reference to Figs. 1—5 or to any one of Figs. 12, 15 and 16 of the accompanying drawings.

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Leamington Spa: Printed for Her Majesty's Stationery Office, by the Courier Press.
—1967. Published by The Patent Office, 25 Southampton Buildings, London, W.C.2,
from which copies may be obtained.

