

## PHASE LOCKED LOOP

## Abstract

PLL apparatus (16) for generating an oscillatory signal (S5) phase locked to a component (S2) of a further signal (S1) comprises a variable oscillator (26) for generating the oscillatory signal (S5) and a source (12) of the further signal (S1). A phase detector (22,30) responsive to the oscillatory signal (S5) and to the component of the further signal (S2), provides a phase error signal (S9) which is coupled to the variable oscillator (26) via a limiter (50). Circuit means (44) are provided for controlling the limiting level of the limiter. The dual limiting substantially improves the loop noise tolerance and reduces the loop sensitivity to occasional phase reversals of the component of the further signal. Additional enhancements to loop stability and noise immunity are provided by an unlock detector (808,812,814) which detects and totalizes phase rotations in a selected area of a phase plane and by a phase wrap detector (804) which maintains a lock indication during phase angle.

FIGURE 1