

RECEIVER, MEMORY AND TESTING METHOD

ABSTRACT

Embodiments of the disclosure provide a receiver, a memory, and a testing method. The receiver includes: a signal receiving module, including a first MOS transistor and a second MOS transistor, where a gate of the first MOS transistor is configured to receive a reference signal and a gate of the second MOS transistor is configured to receive a data signal, and the signal receiving module is configured to output a comparison signal, the comparison signal being configured to represent a magnitude relationship between a voltage value of the reference signal and a voltage value of the data signal; and an adjusting module, including a third MOS transistor, where a source of the third MOS transistor is connected to a source of the first MOS transistor, a drain of the third MOS transistor is connected to a drain of the first MOS transistor, and a gate of the third MOS transistor is configured to receive an adjusting signal. The embodiments of the disclosure facilitate enlarging the range of an effective recognition window of the data signal.

[Fig. 1]