

**METHOD OF INTEGRATING SUBSTRATE CONTACT ON SOI WAFERS
WITH STI PROCESS**

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FIELD OF THE INVENTION

The present invention relates to silicon-on-insulator (SOI) semiconductor devices and a method for forming a structure for contacting a portion of the substrate underlying the silicon on insulator region of the substrate. The present invention also includes semiconductor devices formed according to this process.

BACKGROUND OF THE INVENTION

Semiconductor devices including a silicon on insulator substrate structure include a wafer that has a buried layer of oxide that isolates the top layer of silicon, where the active devices are formed, from the substrate. Hence the term silicon on insulator (SOI). Because the portion of the substrate underlying the oxide layer typically is not electrically connected to any other structure, in other

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words the underlying substrate is floating, static charges can build up in the substrate during normal chip operation. Such static build ups can cause a back channel of the SOI devices to turn on, which can disturb normal operation of the chips. Impact of build up of static charges can include an increase of standby current of the chips, chip thermal runaway, and even malfunction of the logic and SRAM circuits.

To solve this problem, contact has been made to the portion of the substrate underlying the insulator portion of the silicon-on-insulator substrate structure so as to ground it. At the present time, substrate contact typically is created by wire bonding to the back side of a chip at the packaging level. However, such methods can require extra steps and materials. For example, wire bonding to the back of a chip is expensive because it has to be performed on individual chips one by one. Wire bonding may also require alteration of standard packaging methods.

SUMMARY OF THE INVENTION

The present invention provides a method for forming contacts to a substrate region underlying the insulator

portion of a silicon on insulator substrate that may be carried during normal processing operations for forming the chip.

In accordance with these and other objects and advantages, aspects of the present invention provide a method for forming a substrate contact and a substrate that includes a silicon on insulator region. The method includes forming a shallow isolation trench in the silicon on insulator substrate region. The shallow isolation trench is filled. Photoresist is deposited on the substrate. The method also includes forming a contact trench in the substrate through the filled shallow isolation trench and silicon on insulator substrate region extending down at least to the top of a silicon substrate underlying the silicon on insulator region. The contact trench is filled, wherein the material filling the contact trench forms a contact to the silicon substrate.

According to other aspects, the present invention also provides a semiconductor device structure. The device structure includes a substrate including a silicon on insulator substrate region. A shallow trench isolation region is arranged in the substrate. The device also

includes a contact trench extends through the shallow trench in the isolation region to a silicon portion of the substrate underlying the silicon on insulator region. The contact trench forms a contact to an underlying silicon portion of the substrate.

Still other objects and advantages of the present invention will become readily apparent by those skilled in the art from the following detailed description, wherein it is shown and described only the preferred embodiments of the invention, simply by way of illustration of the best mode contemplated of carrying out the invention. As will be realized, the invention is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned objects and advantages of the present invention will be more clearly understood when considered in conjunction with the accompanying drawings, in

which:

Fig. 1 represents a cross-sectional view of an embodiment of a semiconductor device according to the present invention;

Figs. 2-10 represent cross-sectional views an embodiment of a semiconductor device at various stages of an embodiment of a process for forming a semiconductor device according to the present invention, wherein Fig. 10 represents a final form of the embodiment;

Fig. 11 represents an overhead view of another embodiment of a structure according to the present invention;

Fig. 12 represents a cross-sectional view of the embodiment illustrated in Fig. 11, taken along the line 12-12; and

Fig. 13 represents a cross-sectional view of an embodiment of the present invention that includes an island of wells.

DETAILED DESCRIPTION OF THE INVENTION

As described above, the present invention provides a contact to a substrate portion underlying a silicon on insulator substrate structure and a method for forming the contact. The present invention provides a relatively easily manufacturable and cost effective method for making the substrate contact. Among the advantages of the present invention is that the process may be integrated with current processes typically utilized for forming shallow trench isolation regions. The present invention may be integrated with current manufacturing processes without impacting the yield of the processes. Among other functions, a contact according to the present invention may act as a via for a substrate contact.

Fig. 1 illustrates an embodiment of a structure according to the present invention. The embodiment illustrated in Fig. 1 includes two devices 31 and 33 and a substrate contact 35. Oxide region 37 underlies device 33. Substrate 39 includes n+ region 23.

According to the methods of the present invention, a substrate including a silicon on insulator region is

provided. As stated above, the process of the present invention may be integrated with the process of forming a shallow trench isolation region in the substrate.

Accordingly, Fig. 2 illustrates a substrate 1 that includes the underlying substrate 3.

On top of the substrate 3 the insulator region 5 has been formed. In the case of a silicon substrate, the insulator portion of the silicon on insulator structure is an oxidized portion of the silicon substrate. A layer of silicon 7 overlies the oxide or insulator portion of the substrate 5.

In the embodiment illustrated in Fig. 2, the silicon layer 7 has been patterned as part of the process for forming the shallow trench isolation region. Nitride layer 9 overlies silicon layer 7. Both nitride layer 9 and silicon layer 7 are deposited as blanket layers and patterned together. The nitride may be used as CMP stop layer. The broken lines in Fig. 2 illustrate the etched-away portions of the silicon layer.

After etching of the shallow trench to form the structure illustrated in Fig. 2, a material may be deposited

in the regions etched to create the structure illustrated in Fig. 2 as well as on other exposed portions of the top surface of the substrate. Typically, the material deposited in the shallow isolation trench and other portions of the substrate is an electrically insulating material. One example of such an electrically insulating material is tetraethylorthosilicate (TEOS).

After depositing the electrically insulating material, which forms the fill of the shallow isolation trench, a trench may be etched through the shallow isolation trench fill as well as the underlying insulator of the silicon on insulator substrate structure. One method for forming the contact trench is to deposit a layer of photoresist 17 on the electrically insulating material 15 filling the shallow isolation trench and covering portions of the substrate. As illustrated in Fig. 4, the photoresist may be exposed and developed, resulting in formation of a mask with an opening 19 for etching the contact trench.

The pattern formed in the photoresist for etching the contact trench depends upon the form that it is desired that the contact trench have. According to one embodiment, a ring is patterned in the photoresist around the chip in the

field area of the chip, as illustrated in Figs. 11 and 12, as represented by 20. Alternatively, the contact structure may have other configurations. For example, contact may be made inside the chip represented by 22, as also illustrated in Fig. 11. However, the ring configuration may also shield the chip from contamination after dicing.

After patterning the photoresist, the contact trench may be etched. The photoresist may be utilized as a mask to etch the contact trench while masking the shallow isolation trenches to form a conductive contact. Any suitable process may be utilized for etching the contact trench. According to one embodiment, reactive ion etching (RIE) is utilized to form the contact trench. By etching the contact trench after deposition of the electrically insulating in the shallow isolation trench, an oxide RIE process can be utilized as opposed to utilizing a silicon RIE and then an oxide RIE.

Fig. 5 illustrates an embodiment of a contact trench that has been etched through the electrical insulator filling the shallow isolation trench as well as through the buried oxide layer of the silicon on insulator substrate region. Fig. 5 illustrates the structure after etching of

the trench and stripping of the photoresist. As can be seen in Fig. 5, at least a portion of the underlying substrate 3 is exposed by etching of the contact trench.

According to some embodiments, the contact trench may at least partially extend into the underlying substrate region 3. The dimensions of the contact trench may be determined by a desired operational characteristics of the trench. For example, the contact trench may be formed sufficiently wide so as to act as a guard structure to prevent diffusion of dopants through the insulator region of the silicon on insulator region of the substrate. According to one embodiment, the contact trench in the form of a ring has a width of about 0.5 μm .

Where the contact trench is etched as a ring in the substrate, the contact trench may act as a guard ring. The contact structure may extend to the surface of a layer overlying a substrate, to the top of the substrate, or into the substrate.

In some embodiments, in order to enhance substrate contact, at least one dopant may be implanted into the silicon substrate exposed by etching of the contact trench.

According to one embodiment, boron may be implanted into the exposed silicon substrate. Other dopants that may be utilized include arsenic, phosphorus, and/or indium. The dopant dosage may be heavy. For example, the dopant dosage could be about $1 \times 10^{15} \text{ cm}^{-2}$.

The contact trench may then be filled with a desired material. So that the filled contact trench forms an electrical contact to the underlying substrate, the material filling the contact trench may be electrically conducting material. Alternatively, a material that may be treated to become electrically conducting may be utilized to fill the contact trench. The contact trench may be formed and filled with undoped polycrystalline silicon simultaneously with forming and filling trenches forming the shallow isolation regions between devices.

According to one embodiment, undoped polycrystalline silicon may be deposited in the contact trench. As stated above, the present invention may fit in with existing processes. Along these lines, according to standard practices for forming the shallow isolation trench, undoped polycrystalline silicon may be deposited for the purposes of planarizing the shallow isolation trench. Therefore, by

filling the contact trench with undoped polycrystalline silicon, no new steps are introduced by filling the contact trench with undoped polycrystalline silicon.

If the contact trench is in a form of a ring about a portion of the substrate, after depositing the undoped polycrystalline silicon, a ring of polycrystalline silicon may exist about an area of the substrate. This ring or other filled trench structure may be utilized to make a substrate contact.

Fig. 6 illustrates an example of a structure according to the present invention wherein the contact trench has been filled with polycrystalline silicon. The undoped polycrystalline silicon has also been deposited on other surfaces of the substrate.

After this point in the process illustrated in Figs. 2-10, the steps carried out may be basically identical to process steps normally carried out in the shallow trench isolation processing. After depositing the polycrystalline silicon 21, the structure may be planarized. This includes planarizing the electrically insulating material forming the shallow trench isolation region as well as the undoped

polycrystalline silicon. The undoped polycrystalline silicon and electrically insulating material filling the shallow isolation trench may be planarized utilizing chemical mechanical polishing (CMP). Fig. 7 illustrates the structure after planarization of the polycrystalline silicon 21 and the electrically insulating material 15 filling the shallow isolation trench.

The polycrystalline silicon filling the contact trench may be treated as any active silicon area. Accordingly, the undoped polycrystalline silicon filling the contact trench may be subject to a p+ diffusion implant. The polycrystalline silicon filling the contact trench may also be silicided.

After planarization of the polycrystalline silicon and electrically insulating material filling the shallow isolation trench, the structure may be subjected to a reactive ion etch. Fig. 8 illustrates the resulting structure. The purpose of step(s) resulting in the structure represented in Fig. 8 is to etch the oxide 15 down in the area(s) not covered by polycrystalline silicon so it becomes planar with the oxide 21 below the poly. The polycrystalline silicon acts like a mask during this etch.

Fig. 9 shows the polycrystalline silicon mask being etched away/recessed so it is slightly below oxide TEOS 15 level. At this point all oxide 21 is sufficiently planar so that a CMP step can be used to further planarized it down to nitride level as shown in Fig. 10.

After doping of the filled contact trench with dopant, such as arsenic and phosphorus for the contact to an n-type substrate and boron and indium for contact to a p-type substrate, and also silicidation, the substrate contact may be landed to connect and ground the substrate. Doping and silicidation processes typically are part of normal processing for a chip. According to one embodiment, the middle contact (MC) is landed to the polycrystalline silicon filling the contact trench to connect and ground the substrate.

The contact of the present invention may be landed by depositing at least one electrically conducting material on at least one portion of the filled contact trench. The at least one electrically conducting material may include at least one metal and/or alloy. Other material(s) that can be used to fill the contact may include tungsten, in which case the substrate contact etch step can be done after all device

formation, such as NFET and PFET, and insulating material has been deposited and planarized for middle contact insulator but before middle contact etch.

Because of the simplicity of the process of the present invention, it can provide very good ohmic contact to the substrate without any potential yield degradation to the chip. According to some applications, it may be desirable to locally bias the substrate in order to modify and enhance the performance of the SOI device on top of the substrate. According to such embodiments, an island of wells may be required in the substrate to isolate them from each other. The present invention may be easily combined with such structures because the structure of the present invention requires minimal area and can be integrated easily into any part of the circuit in the chip.

Fig. 13 illustrates an example of an embodiment of the present invention that includes an island of wells. The embodiment illustrated in Fig. 13 includes two devices 23 and 25, each having an associated substrate contact 27 and 29. An n well is associated with device 27 and an n well and a p well are associated with contact 29.

As stated above, the present invention also includes a semiconductor device. The semiconductor device includes a substrate including a silicon on insulator substrate region. The semiconductor device structure also includes at least one shallow trench isolation region on the substrate. A contact trench extends through at least a portion of a shallow trench isolation region to a silicon portion of the substrate underlying the silicon on insulator region. The contact trench forms a contact to the underlying silicon portion of the substrate.

The foregoing description of the invention illustrates and describes the present invention. Additionally, the disclosure shows and describes only the preferred embodiments of the invention, but as aforementioned, it is to be understood that the invention is capable of use in various other combinations, modifications, and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein, commensurate with the above teachings, and/or the skill or knowledge of the relevant art. The embodiments described hereinabove are further intended to explain best modes known of practicing the invention and to enable others skilled in the art to utilize the invention in such, or other, embodiments and

with the various modifications required by the particular applications or uses of the invention. Accordingly, the description is not intended to limit the invention to the form disclosed herein. Also, it is intended that the appended claims be construed to include alternative embodiments.



CLAIMS

We claim:

1. A method for forming a substrate contact in a substrate that includes a silicon on insulator region, the method comprising the steps of:

forming a shallow isolation trench in the silicon on insulator substrate;

filling the shallow isolation trench;

depositing photoresist on the substrate;

forming a contact trench in the substrate through the filled shallow isolation trench and silicon on insulator substrate region, extending at least to a top of a silicon substrate underlying the silicon on insulator region; and

filling the contact trench, wherein the material filling the contact trench forms a contact to the silicon substrate.

2. The method according to claim 1, wherein the shallow isolation trench is filled with an electrically insulating material.

3. The method according to claim 2, wherein the



electrically insulating material is tetraethylorthosilicate oxide.

4. The method according to claim 1, wherein forming the contact trench comprising the steps of:

depositing a layer of photoresist on the substrate after filling the shallow isolation trench;

patterning the photoresist; and

etching the contact trench utilizing the photoresist as a mask.

5. The method according to claim 1, wherein the contact trench extends around the substrate in a field area of the substrate.

6. The method according to claim 1, wherein the contact trench is formed utilizing reactive ion etching.

7. The method according to claim 1, wherein the contact trench is formed sufficiently wide to act as a guard structure to prevent diffusion of dopants through the insulator region of the silicon on insulator region of the substrate.



8. The method according to claim 1, further comprising the step of:

implanting at least one dopants into the silicon substrate exposed by etching of the contact trench.

9. The method according to claim 8, wherein the at least one dopant includes boron, phosphorus, arsenic, or indium.

10. The method according to claim 1, further comprising the step of:

planarizing material filling the shallow isolation trench.

11. The method according to claim 10, further comprising the steps of:

depositing undoped polycrystalline silicon over the substrate; and

planarizing the undoped polycrystalline silicon and material filling the shallow isolation trench.

12. The method according to claim 1, wherein the contact trench is filled with undoped polycrystalline silicon.



13. The method according to claim 1, further comprising the step of:

carrying out a p⁺ diffusion implant on the material filling the contact trench for contact to a p-type substrate and n⁺ diffusion for contact to a well on an n-type substrate.

14. The method according to claim 1, further comprising the step of:

siliciding the material filling the contact trench.

15. The method according to claim 1, further comprising the step of:

forming a contact of an electrically conducting material to the filled contact trench.

16. The method according to claim 15, wherein the contact includes at least one metal.

17. The method according to claim 1, further comprising the step of:

biasing the substrate.

18. The method according to claim 17, further



comprising the steps of:

forming a plurality of wells in the substrate; and
isolating the wells from each other.

19. A semiconductor device structure, comprising:
a substrate including a silicon-on-insulator substrate
region;

at least one shallow trench isolation region on the
substrate; and

a contact trench extending through the shallow trench
isolation region to a silicon portion of the substrate
underlying the silicon on insulator region and forming a
contact to the underlying silicon portion of the substrate.

20. The semiconductor device according to claim 19,
wherein the shallow trench isolation region is filled with
an electrically insulating material.

21. The semiconductor device according to claim 20,
wherein the electrically insulating material is
tetraethylorthosilicate oxide.

22. The semiconductor device according to claim 19,
wherein the contact trench extends around the substrate in a



field area of the substrate.

23. The semiconductor device according to claim 19, wherein the contact trench is sufficiently wide to act as a guard structure to prevent diffusion of dopants through the insulator region of the silicon on insulator region of the substrate.

24. The semiconductor device according to claim 19, wherein at least one dopant is implanted into the silicon substrate underlying the contact trench.

25. The semiconductor device according to claim 24, wherein the at least one dopant includes boron, phosphorus, arsenic, indium, or antimony.

26. The semiconductor device according to claim 19, wherein the contact trench is filled with polycrystalline silicon.

27. The semiconductor device according to claim 19, wherein the polycrystalline silicon is p+ doped or n+ doped.

28. The semiconductor device according to claim 27,



24.

wherein the material filling the contact trench as silicided.

29. The semiconductor device according to claim 19, further comprising:

a contact of an electrically conducting material electrically connected to the contact trench.

30. The semiconductor device according to claim 29, wherein the contact includes at least one metal.

31. The semiconductor device according to claim 19, wherein the substrate is biased.

32. The semiconductor device according to claim 31, further comprising:

a plurality of isolated wells in the substrate.