INTEGRATED CIRCUIT PACKAGE AND METHOD OF MAKING SAME

ABSTRACT

A chip package includes a first die with an active surface having at least one die pad positioned thereon; a first adhesive layer having a first surface coupled to the active surface of the first die and a second surface opposite the first surface; and a first dielectric layer having a top surface. A first portion of the top surface of the first dielectric layer is coupled to the second surface of the first adhesive layer. A second portion of the top surface of the first dielectric layer, distinct from the first portion, is substantially free of adhesive.

Figure 1