

RESISTANCE VARIABLE MEMORY CELL STRUCTURES AND METHODS

Technical Field

[0001] The present disclosure relates generally to semiconductor memory devices, methods, and systems, and more particularly, to resistance variable memory cell structures and methods.

Background

[0002] Memory devices are typically provided as internal, semiconductor, integrated circuits in computers or other electronic devices. There are many different types of memory, including random-access memory (RAM), read only memory (ROM), dynamic random access memory (DRAM), synchronous dynamic random access memory (SDRAM), flash memory, and resistance variable memory, such as phase change random access memory (PCRAM), resistive random access memory (RRAM), and conductive bridge random access memory (CBRAM), among others.

[0003] The phase change material of a PCRAM device may exist in an amorphous, higher resistance state, or a crystalline, lower resistance state. The resistance state of the PCRAM cell may be altered by applying sources of energy to the cell, such as current pulses or pulses of light, among other sources of energy. For example, the resistance state of the PCRAM cell may be altered by heating the cell with a programming current. This results in the PCRAM cell being programmed to a particular resistance state, which may correspond to a data state. PCRAM devices may also be configured to provide multi-level storage. That is, the memory device may have a plurality of discrete and identifiable states which allow for multi-bit storage in a single memory cell.

[0004] An RRAM device includes a variable resistive material, such as a transition metal oxide, that has varying resistance depending on voltages applied thereto. When a voltage equal to or greater than a set voltage is applied to the variable resistive material, the resistance of the variable resistive material decreases (e.g., ON state). When a voltage equal to or greater than a reset voltage is applied to the variable resistive material, the resistance of the variable resistive material increases (e.g., OFF state). High volume manufacturability

and reliability remain issues for resistance variable memory devices such as PCRAM and RRAM devices.

Brief Description of the Drawings

[0005] Figures 1A-1G illustrate process steps associated with forming a resistance variable memory cell structure in accordance with embodiments of the present disclosure.

[0006] Figure 1H illustrates a top view of the memory cell structure illustrated in Figure 1G.

Detailed Description

[0007] Resistance variable memory cell structures and methods are described herein. A number of methods of forming a resistance variable memory cell structure include forming a memory cell structure having a via formed over a first electrode, forming a resistance variable memory cell material on the first electrode and a wall of the via, forming a first dielectric material on the resistance variable memory cell material, removing a portion of the first dielectric material such that a portion of the resistance variable memory cell material is exposed, and forming a second electrode on a first exposed portion of the resistance variable memory cell material and third electrode on a second exposed portion of the resistance variable memory cell material. One or more methods include forming a spacer material on at least a portion of the second electrode, the third electrode, and the first dielectric material, and forming a first and a second resistance variable memory cell structure by removing at least a portion of the spacer material between the second and third electrodes, at least a portion of the first dielectric material within the via, and at least a portion of the resistance variable memory cell material formed on the first electrode.

[0008] Embodiments of the present disclosure provide various benefits such as providing a pitch doubled array having a reduced footprint as compared to previous resistance variable memory cell structures. Embodiments also provide a memory cell structure yielding a low switching current as compared to previous resistance variable memory cell structures, among other benefits. For instance, the pitch doubled vertical orientation of one or more embodiments

provide a manufacturable alternative to previous memory cell approaches such as the planar bridge cell structure.

[0009] As will be appreciated, elements shown in the various embodiments herein can be added, exchanged, and/or eliminated so as to provide a number of additional embodiments of the present disclosure. In addition, as will be appreciated, the proportion and the relative scale of the elements provided in the figures are intended to illustrate the embodiments of the present disclosure and should not be taken in a limiting sense.

[0010] Figures 1A-1F illustrate process steps associated with forming the resistance variable memory cell structure shown in Figure 1G in accordance with embodiments of the present disclosure. The memory cell structure shown in Figures 1A-1G includes a base semiconductor structure that includes a substrate 102 including a conductive contact 106 formed in a dielectric material 104. The substrate 102 can be a silicon substrate, silicon on insulator (SOI) substrate, or silicon on sapphire (SOS) substrate, among others. The dielectric material 104 can be a nitride or oxide such as silicon dioxide (SiO_2), among other dielectric materials. The conductive contact 106 can be made of tungsten (W) or other suitable conductive material and can be formed in the dielectric layer 104 via a masking and etching process, for instance.

[0011] The structure includes a via 116 formed over a bottom electrode (BE) 108. In this example, the via 116 is formed through a dielectric material 114 to expose the top surface of the bottom electrode 108 and can be referred to as a contact hole 116. In one or more embodiments, the via 116 has a diameter of not greater than 20 nanometers (nm). However, embodiments are not limited to a particular diameter of via 116, which can be formed by masking and etching, among other suitable processes. Although the examples described in Figures 1A-1F relate to an annular shaped via, embodiments are not so limited. For instance, the via 116 can be various different shapes and can various different aspect ratios associated therewith.

[0012] The bottom electrode 108 is formed in a dielectric material 112, such as silicon dioxide, and can be made of various conductive materials or composite structures including tungsten, TiN (titanium nitride), TaN (tantalum nitride), iridium, platinum, ruthenium, and/or copper, for example. As described further herein, the bottom electrode 108 can serve as a common bottom electrode

for two distinct resistance variable memory cells (e.g., PCRAM cells, CBRAM cells, or RRAM cells, among others). The bottom electrode 108 is formed on conductive contact 104. Although not shown in Figures 1A-1G, the contact 106 can be coupled to an access device (e.g., an access transistor) corresponding to a particular memory cell.

[0013] Figure 1B illustrates a resistance variable material 118 formed on the structure illustrated in Figure 1A. As such, the material 118 is formed over the bottom electrode 108, the walls of the via 116, and the exposed portions of the dielectric material 114. The material 118 can be formed (e.g., deposited) using techniques such as atomic layer deposition (ALD) or chemical vapor deposition (CVD), among other methods, as will be appreciated by one of ordinary skill in the art. The material 118 is deposited to a thickness of not more than about 5nm, in some embodiments. In various embodiments, the thickness of material 118 is 1-5nm.

[0014] In embodiments in which the resistance variable memory cell structure is a phase change memory cell structure, the material 118 can be referred to as a phase change material 118. In such embodiments, the phase change material 118 can be a phase change chalcogenide alloy such as a Germanium-Antimony-Tellurium (GST) material (e.g., a Ge-Sb-Te material such as $\text{Ge}_2\text{Sb}_2\text{Te}_5$, $\text{Ge}_1\text{Sb}_2\text{Te}_4$, $\text{Ge}_1\text{Sb}_4\text{Te}_7$, etc.). The hyphenated chemical composition notation, as used herein, indicates the elements included in a particular mixture or compound, and is intended to represent all stoichiometries involving the indicated elements. Other phase change materials can include alloys of: Ge-Te, In-Se, Sb-Te, Ga-Sb, In-Sb, As-Te, Al-Te, Ge-Sb-Te, Te-Ge-As, In-Sb-Te, Te-Sn-Se, Ge-Se-Ga, Bi-Se-Sb, Ga-Se-Te, Sn-Sb-Te, In-Sb-Ge, Te-Ge-Sb-S, Te-Ge-Sn-O, Te-Ge-Sn-Au, Pd-Te-Ge-Sn, In-Se-Ti-Co, Ge-Sb-Te-Pd, Ge-Sb-Te-Co, Sb-Te-Bi-Se, Ag-In-Sb-Te, Ge-Sb-Se-Te, Ge-Sn-Sb-Te, Ge-Te-Sn-Ni, Ge-Te-Sn-Pd, and Ge-Te-Sn-Pt, among various other phase change materials.

[0015] In embodiments in which the resistance variable memory cell structure is a resistive random access memory cell structure, the material 118 can be a transition metal oxide (M_xO_y) material with the metal (M) being nickel, niobium, titanium, zirconium, hafnium, cobalt, iron, copper, or chrome, for

instance. In such embodiments, the material 118 can also be a chalcogenide material or perovskite material, for example.

[0016] In embodiments in which the resistance variable memory cell structure is a conductive bridging random access memory cell structure, the material 118 can be an electrolyte material such as a chalcogenide material, for instance. The chalcogenide material can be germanium-sulfide, germanium-selenide, tungsten oxide, or copper sulfide, among other electrolyte materials.

[0017] Figure 1C illustrates a dielectric material 120 formed on the structure shown in Figure 1B. The dielectric material 120 can be a low temperature oxide or nitride material deposited at a temperature of below about 450°C, for example. The dielectric material 118 is formed on the resistance variable material 118 and fills the via 116.

[0018] Figure 1D illustrates the structure shown in Figure 1C subsequent to removal of a portion of the dielectric material 120 and a portion of the resistance variable material 118. As an example, the removed portions of materials 118 and 120 can be removed via chemical mechanical planarization (CMP). In the embodiment illustrated in Figure 1D, the structure is planarized to the surface of the dielectric material 114. As such, an exposed planarized upper surface of the resistance variable material 118 located within the via 116 has an annular shape. That is, the upper surface of the material 118 has an arcuate shape around the planarized upper surface of the dielectric 120 formed in the via 116.

[0019] Figure 1E illustrates the structure shown in Figure 1D subsequent to formation of a first top electrode (TE) 122-1 and a second top electrode 122-2. The top electrodes 122-1/122-2 are formed on exposed portions of the resistance variable material 118. In this example, the top electrodes 122-1/122-2 are formed such that an edge portion of each of the top electrodes overlaps the planarized surface of the dielectric material 120 within the via 116. The top electrodes 122-1/122-2 are also formed such that they also overlap the dielectric material 114; however, embodiments are not limited to top electrodes that overlap the dielectric material 114. The top electrodes 122-1/122-2 can be made of various conductive materials or composite structures including tungsten, TiN (titanium nitride), TaN (tantalum nitride), iridium, platinum, ruthenium, and/or copper, for example. In one or more embodiments, the bottom electrode 108 and

top electrodes 122-1/122-2 can be asymmetric. For instance, the bottom electrode 108 can be made of a different material than one or both of the top electrodes 122-1 and 122-2.

[0020] Figure 1F illustrates the structure shown in Figure 1E subsequent to a spacer material 124 formed thereon. The spacer material 124 can be an oxide material such as silicon dioxide or other suitable dielectric material.

[0021] Figure 1G illustrates the structure shown in Figure 1F subsequent to removal of at least a portion of the spacer material 124 between the electrodes 122-1 and 122-2, at least a portion of the dielectric material 120 within the via 116, and at least a portion of the resistance variable material 118 formed on the bottom electrode 108. Figure 1H illustrates a top view of the memory cell structure illustrated in Figure 1G. In this example, the structure has been patterned and a dry etch process used to form an opening 125 and also create two distinct resistance variable memory cell structures (e.g., PCRAM, CBRAM, or RRAM structures), which share a common bottom electrode 108.

[0022] For instance, a first memory cell structure includes the vertically oriented resistance variable material 118-1 located between bottom electrode 108 and top electrode 122-1 and a second memory cell structure includes the vertically oriented resistance variable material 118-2 located between bottom electrode 108 and top electrode 122-2. As illustrated in Figure 1G, the spacer material 124-1 is formed on the dielectric material 120-1 and on the edges of the top electrode 122-1 and the spacer material 124-2 is formed on the dielectric material 120-2 and on the edges of the top electrode 122-2.

[0023] The resistance variable materials 118-1 and 118-2 each have an arcuate top surface in contact with a respective top electrode 1122-1 and 122-2 and a non-arcuate bottom surface in contact with the bottom electrode 108. The non-arcuate portions of the material 118-1 and 118-2 correspond to the portions located beneath the respective dielectric material 120-1 and 120-2 remaining in via 116 subsequent to the etch process. As such, the arcuate portions of the material 118-1 and 118-2 refer to the regions located between the dielectric material 114 and the respective dielectric material 120-1 and 120-2.

Accordingly, in various embodiments, the arcuate portions of the first and second vertically oriented resistance variable materials 118-1 and 118-2 are

located a distance of not more than 20nm from each other (e.g., in embodiments in which the diameter of the via 116 is not greater than 20nm).

[0024] Forming memory cell structures according to embodiments described herein can provide two memory cells for a single contact hole (e.g., via 116), which can increase memory density by providing pitch doubling as compared to previous approaches that may provide a single memory cell for a particular contact hole. The vertical orientation of the resistance variable cell material (e.g., 118-1 and 118-2) can also provide increased memory density as compared to previous approaches such as a planar bridge cell approach, for example.

[0025] Additionally, embodiments described herein can provide a reduced cross sectional area of the resistance variable material as compared to previous approaches, which can provide a low switching current. Forming resistance variable memory cell structures in accordance with one or more embodiments of the present disclosure can also avoid etch damage of the memory cell structures.

[0026] In various embodiments, the processing associated with Figures 1F-1H can be optional. For instance, the structure shown in Figure 1E can represent two resistance variable memory cells that can be operated independently. As such, the spacer material 124 formation and etch to the bottom electrode 108 is optional, in one or more embodiments.

[0027] One of ordinary skill in the art will appreciate that an array of resistance variable memory cells including memory cell structures such as those illustrated in Figures 1E and 1G would include additional memory components. For instance, a PCRAM and/or RRAM array could include access devices (e.g., access transistors) formed on substrate 102. The bottom electrode 108 can be coupled to an access device (e.g., to a source or drain region via contact plug 106) and the top electrodes 122-1 and 122-2 can be coupled to one or more bit lines (e.g., via contact plugs), for example.

[0028] Resistance variable memory cell structures and methods are described herein. A number of methods of forming a resistance variable memory cell structure include forming a memory cell structure having a via formed over a first electrode, forming a resistance variable memory cell material on the first electrode and a wall of the via, forming a first dielectric material on

the resistance variable memory cell material, removing a portion of the first dielectric material such that a portion of the resistance variable memory cell material is exposed, forming a second electrode on a first exposed portion of the resistance variable memory cell material and third electrode on a second exposed portion of the resistance variable memory cell material, forming a spacer material on at least a portion of the second electrode, the third electrode, and the first dielectric material, and forming a first and a second resistance variable memory cell structure by removing at least a portion of the spacer material between the second and third electrodes, at least a portion of the first dielectric material within the via, and at least a portion of the resistance variable memory cell material formed on the first electrode.

[0029] Although specific embodiments have been illustrated and described herein, those of ordinary skill in the art will appreciate that an arrangement calculated to achieve the same results can be substituted for the specific embodiments shown. This disclosure is intended to cover adaptations or variations of various embodiments of the present disclosure. It is to be understood that the above description has been made in an illustrative fashion, and not a restrictive one. Combination of the above embodiments, and other embodiments not specifically described herein will be apparent to those of skill in the art upon reviewing the above description. The scope of the various embodiments of the present disclosure includes other applications in which the above structures and methods are used. Therefore, the scope of various embodiments of the present disclosure should be determined with reference to the appended claims, along with the full range of equivalents to which such claims are entitled.

[0030] In the foregoing Detailed Description, various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the disclosed embodiments of the present disclosure have to use more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

What is claimed is:

1. A method of forming a memory cell, comprising:
forming a resistance variable memory cell material on a first electrode and a wall of a via;
forming a first dielectric material on the resistance variable memory cell material;
removing a portion of the first dielectric material such that a portion of the resistance variable memory cell material is exposed; and
forming a second electrode on a first exposed portion of the resistance variable memory cell material and third electrode on a second exposed portion of the resistance variable memory cell material.
2. The method of claim 1, wherein the method includes forming a spacer material on at least a portion of the second electrode, the third electrode, and the first dielectric material.
3. The method of claim 2, wherein the method includes removing at least a portion of the spacer material between the second and third electrodes, at least a portion of the first dielectric material within the via, and at least a portion of the resistance variable memory cell material formed on the first electrode to form a first and a second resistance variable memory cell structure.
4. The method of claim 3, wherein forming the first and the second resistance variable memory cell structures includes forming a first arcuate resistance variable region corresponding to the first resistance variable memory cell structure and a second arcuate resistance variable region corresponding to the second resistance variable memory cell structure.
5. The method of any one of claims 1-4, including forming the resistance variable memory cell material such that it has a thickness of no greater than 5 nanometers.

6. The method of any one of claims 1-4, wherein forming the resistance variable memory cell material includes depositing the resistance variable memory cell material using atomic layer deposition.
7. The method of any one of claims 1-4, wherein forming the resistance variable memory cell material includes depositing the resistance variable memory cell material using chemical vapor deposition.
8. The method of any one of claims 1-4, including forming the first electrode of a material that is different than at least one of the second and the third electrode.
9. The method of any one of claims 1-4, including forming the via through a second dielectric material to the first electrode prior to forming the resistance variable memory cell material on the first electrode and the wall of the via.
10. The method of claim 9, wherein removing the portion of the first dielectric material includes planarizing an upper surface of the semiconductor structure down to the second dielectric material.
11. The method of any one of claims 1-4, including forming the second electrode and the third electrode such that a portion of each overlaps the first dielectric material formed in the via.
12. A method of forming a memory cell, comprising:
 - forming a memory cell structure having a via formed over a first electrode;
 - forming a phase change material on the first electrode and on the walls of the via such that a gap remains between the walls of the via;
 - forming a first dielectric material on the phase change material;
 - removing a portion of the first dielectric material such that a portion of the phase change material is exposed and such that the first dielectric material remains only in the gap;

forming a second electrode on a first exposed portion of the phase change material and third electrode on a second exposed portion of the phase change material;

forming a spacer material on at least a portion of the second electrode, the third electrode, and the first dielectric material located in the gap; and

removing at least a portion of the spacer material between the second and third electrodes, at least a portion of the first dielectric material within the via, and at least a portion of the phase change material formed on the first electrode such that a first and a second phase change memory cell structure is formed.

13. The method of claim 12, wherein removing the at least a portion of the spacer material between the second and third electrodes, the at least a portion of the first dielectric material within the via, and the at least a portion of the phase change material forms an arcuate phase change region corresponding to the first phase change memory cell structure and an arcuate phase change region corresponding to the second phase change memory cell structure, with the first electrode being common to the first and the second phase change memory cell structures.

14. The method of claim 12, wherein forming the first dielectric material includes depositing a low temperature oxide material.

15. The method of any one of claims 12-14, including forming the second and third electrodes such that they overlap the dielectric material located in the gap.

16. The method of any one of claims 12-14, including performing a dry etch to remove the at least a portion of the spacer material between the second and third electrodes, the at least a portion of the first dielectric material within the via, and the at least a portion of the phase change material formed on the first electrode.

17. A resistance variable memory cell structure, comprising:

a first electrode common to a first and a second resistance variable memory cell;

a first vertically oriented resistance variable material having an arcuate top surface in contact with a second electrode and a non-arcuate bottom surface in contact with the first electrode; and

a second vertically oriented resistance variable material having an arcuate top surface in contact with a third electrode and a non-arcuate bottom surface in contact with the first electrode.

18. The resistance variable memory cell structure of claim 17, wherein an arcuate portion of the first and the second vertically oriented resistance variable material is located between a first dielectric material and a second dielectric material.

19. The resistance variable memory cell structure of claim 18, wherein the arcuate portion of the first vertically oriented resistance variable material is located a distance of not more than 20 nanometers from the arcuate portion of the second vertically oriented resistance variable material.

20. The resistance variable memory cell structure of claim 18, wherein the second electrode overlaps a portion of the first and the second dielectric material.

21. The resistance variable memory cell structure of claim 18, wherein a spacer material is formed on the first dielectric material and on an edge of the second electrode and an edge of the third electrode.

22. The resistance variable memory cell structure of any one of claims 17-21, wherein the first electrode is made of a material different than at least one of the second and the third electrodes.

23. The resistance variable memory cell structure of any one of claims 17-21, wherein the resistance variable material has a thickness of not greater than 5 nanometers.

24. The resistance variable memory cell structure of claim 17, wherein the second electrode is the top electrode of a first phase change memory cell, the third electrode is the top electrode of a second phase change memory cell, and the first electrode is a bottom electrode common to the first and second phase change memory cells.

25. The resistance variable memory cell structure of any one of claims 17-21, wherein the arcuate top surface of the first and the second vertically oriented resistance variable material is a planarized surface.

26. The resistance variable memory cell structure of any one of claims 17-21, wherein the first electrode is formed on a conductive contact.

27. An array of resistance variable memory cells having at least a first and a second resistance variable memory cell structure formed according to a method, comprising:

- forming a memory cell structure having a via formed over a first electrode;

- forming a resistance variable memory cell material on the first electrode and a wall of the via;

- forming a first dielectric material on the resistance variable memory cell material;

- removing a portion of the first dielectric material such that a portion of the resistance variable memory cell material is exposed;

- forming a second electrode on a first exposed portion of the resistance variable memory cell material and third electrode on a second exposed portion of the resistance variable memory cell material;

- forming a spacer material on at least a portion of the second electrode, the third electrode, and the first dielectric material; and

- forming the first and the second resistance variable memory cell structure by removing at least a portion of the spacer material between the second and third electrodes, at least a portion of the first dielectric material within the via, and at least a portion of the resistance variable memory cell material formed on the first electrode.