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(54) Title: NANOSHEET TRANSISTOR WITH SELF-ALIGNED DIELECTRIC PILLAR

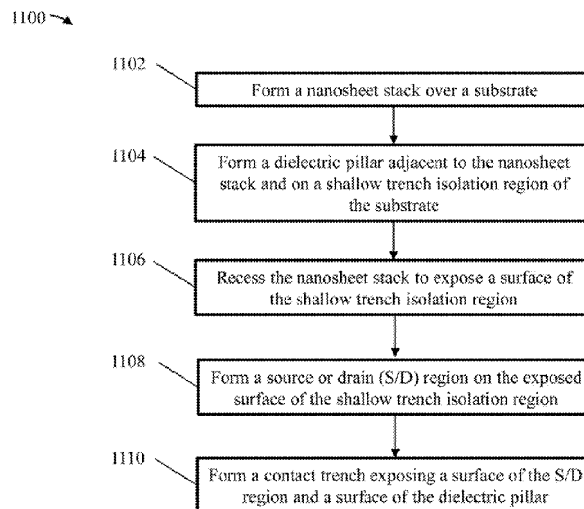


Fig. 11

(57) Abstract: A semiconductor structure and a method for forming a semiconductor structure having a self-aligned dielectric pillar for reducing trench silicide-to-gate parasitic capacitance are provided. A nanosheet stack (206) is formed over a substrate (204). A dielectric pillar (402) is positioned adjacent to the nanosheet stack (206) and on a shallow trench isolation region (212) of the substrate (204). The nanosheet stack (206) is recessed to expose a surface of the shallow trench isolation region (212) and a source or drain (S/D) region (602) is formed on the exposed surface of the shallow trench isolation region (212). A contact trench (802) is formed that exposes a surface of the S/D region (602) and a surface of the dielectric pillar (402).

[Continued on next page]

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