

SEMICONDUCTOR DEVICE AND OPERATING METHOD OF SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

5 **[0001]** This application claims priority to Korean Patent Application No. 10-2023-0018626 filed on February 13, 2023, which is incorporated herein by reference in its entirety.

BACKGROUND

10 **1. Technical Field**

[0002] Embodiments of the present disclosure relate to an integrated circuit technology, and, more particularly, to a semiconductor device and an operating method of the semiconductor device.

15 **2. Related Art**

[0003] As electronic devices are reduced in size, with low power consumption and high performance, a semiconductor device capable of storing information is required for various electronic devices, such as computers and portable communication devices. The semiconductor
20 device may be basically divided into a volatile memory device and a nonvolatile memory device. The volatile memory device has a fast data processing speed, but has a disadvantage in that the volatile memory device needs to be continuously supplied with power in order to maintain data that has been stored in the volatile memory device.

The nonvolatile memory device does not need to be continuously supplied with power in order to maintain data that has been stored in the nonvolatile memory device, but has a disadvantage in that the nonvolatile memory device has a slow data processing speed.

5 **[0004]** In order to deploy more memory cells in the same area of a nonvolatile memory device, a technology for forming a plurality of memory cells by cutting one hole is being developed.

[0005] Furthermore, research on the development of a technology for storing multi-bit data in two memory cells is being carried out.

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SUMMARY

[0006] In an embodiment of the present disclosure, a semiconductor device may include a page buffer comprising first to fifth latches, wherein the first to third latches and the fifth latch are configured to
15 store 4-bit original data, among 5-bit original data, respectively, and the fourth latch is configured to store data identical with the data that has been stored in the second latch and a control circuit configured to determine a program inhibition pattern based on data that have been stored in two of the first to fifth latches and control the page buffer so
20 that data that has been stored in at least one of the first to fifth latches is inverted based on the program inhibition pattern.

In an embodiment of the present disclosure, an operating method of a semiconductor device may include receiving 4-bit original data, among 5-bit original data, encoding the 4-bit original data into 5-bit

conversion data, programming 3-bit conversion data, among the 5-bit conversion data, into a first memory cell, receiving remaining 1-bit original data, among the 5-bit original data and programming remaining 2-bit conversion data among the 5-bit conversion data and
5 the remaining 1-bit original data, into a second memory cell.

In an embodiment of the present disclosure, an operating method of a semiconductor device may include receiving 4-bit original data, among 5-bit original data, converting the 4-bit original data into 5-bit conversion data including 2-bit conversion data and remaining 3-bit
10 conversion data, determining whether the remaining 3-bit conversion data have been encoded based on the 2-bit conversion data and determining whether the 2-bit conversion data have been encoded based on 2-bit data, among the remaining 3-bit conversion data.

BRIEF DESCRIPTION OF THE DRAWINGS

15 **[0007]** FIG. 1 is a diagram for schematically describing a semiconductor device according to an embodiment of the present disclosure.

[0008] FIG. 2 is a diagram for schematically describing input and output of data by a semiconductor device according to an embodiment of the present disclosure.

20 **[0009]** FIG. 3 is a diagram for describing reading of data from a memory cell by a semiconductor device according to an embodiment of the present disclosure.

[0010] FIG. 4A, FIG. 4B and FIG. 4C are a diagram for describing an encoding operation of a semiconductor device according to an

embodiment of the present disclosure.

[0011] FIG. 5 is a diagram for describing an operation of a page buffer with respect to an encoding operation of a semiconductor device according to an embodiment of the present disclosure.

5 [0012] FIG. 6 is a diagram for schematically describing input and output of data by a semiconductor device according to another embodiment of the present disclosure.

[0013] FIG. 7A, FIG. 7B and FIG. 7C are a diagram for describing an encoding operation of a semiconductor device according to another
10 embodiment of the present disclosure.

[0014] FIG. 8 is a diagram for describing an operation of a page buffer with respect to an encoding operation of a semiconductor device according to another embodiment of the present disclosure.

[0015] FIGS. 9 and 10 are flowcharts for describing an operating
15 method of a semiconductor device according to another embodiment of the present disclosure.

[0016] FIG. 11 is a block diagram of a semiconductor device according to an embodiment of the present disclosure.

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DETAILED DESCRIPTION

[0017] Hereinafter, embodiments according to the technical spirit of the present disclosure are described with reference to the accompanying drawings.

[0018] Embodiments of the present disclosure may provide a

semiconductor device capable of reducing the number of latches that is necessary for an encoding operation and an operating method of the semiconductor device.

[0019] It is possible to improve an area margin of the semiconductor device by reducing the number of latches of a page buffer, which is necessary for an encoding operation.

[0020] FIG. 1 is a diagram for schematically describing a semiconductor device 100 according to an embodiment of the present disclosure.

[0021] Referring to FIG. 1, the semiconductor device 100 may be configured to store multi-bit data in a pair of memory cells 41 and 42 by distributing the multi-bit data and outputting the multi-bit data. For example, the semiconductor device 100 may receive multi-bit data having 5 bits from a host 200, and may store the multi-bit data having 5 bits in the pair of memory cells 41 and 42 by distributing the multi-bit data having 5 bits. Furthermore, the semiconductor device 100 may restore, to multi-bit data having 5 bits, data that have been distributed and stored in the pair of memory cells 41 and 42, and may transmit the restored data to the host 200.

[0022] The semiconductor device 100 may include a data input and output circuit 10, an encoder 20, a data transfer circuit 30, the pair of memory cells 41 and 42, and a decoder 50. As illustrated in FIG. 1, the semiconductor device 100 may perform an operation of storing received multi-bit data in the pair of memory cells 41 and 42 by distributing the multi-bit data, restoring data that has been stored in

the pair of memory cells 41 and 42, and outputting the restored data.

[0023] The data input and output circuit 10 may receive multi-bit data (e.g., 5-bit data) from the host 200.

[0024] The encoder 20 may distribute 5-bit data so that the 5-bit data
5 is stored in the pair of memory cells 41 and 42, and may encode the distributed data if necessary.

[0025] The data transfer circuit 30 may transfer distributed data to the pair of memory cells 41 and 42 so that the distributed data is stored in the pair of memory cells 41 and 42, respectively. Furthermore, the
10 data transfer circuit 30 may transfer, to the decoder 50, data that has been stored in the pair of memory cells 41 and 42. In an embodiment, the data transfer circuit 30 may include a row decoder (X_DEC) and a page buffer (PB) capable of selecting the pair of memory cells 41 and 42 and sensing the pair of memory cells 41 and 42 that have been
15 selected.

[0026] The pair of memory cells 41 and 42 may include a first memory cell 41 and a second memory cell 42. In an embodiment, each of the first and second memory cells 41 and 42 may include a multi-level cell (MLC). The pair of memory cells 41 and 42 may be memory cells that
20 have been formed by cutting one memory cell. The first memory cell 41 may include an odd plug cell. The second memory cell 42 may include an even plug cell.

[0027] The decoder 50 may restore, to 5-bit data, the data that have been transferred by the data transfer circuit 30 (e.g., data that have

been distributed and stored).

[0028] The data that has been restored by the decoder 50 may be output to the host 200 through the data input and output circuit 10.

[0029] FIG. 2 is a diagram for schematically describing input and output of data by a semiconductor device according to an embodiment of the present disclosure. FIG. 2 is a diagram for schematically describing an operation of distributing multi-bit data in order to store the multi-bit data in a pair of memory cells and encoding the distributed data and an operation of restoring, to multi-bit data, data that has been stored in the pair of memory cells. FIG. 2 merely describes multi-bit data having 5 bits as an example, and does not limit multi-bit data to 5-bit data.

[0030] Referring to FIG. 2, multi-bit data having 5 bits may include data having first to fifth bits QSB, PSB, MSB, CSB, and LSB (i.e., 5-bit data). Each of the first and second memory cells (e.g., odd plug cell and even plug cell) may be a multi-level cell (MLC), and may store cell data including first to third bits MSB, CSB, and LSB. In an embodiment, each of the first and second memory cells (i.e., the odd plug cell and the even plug cell) may have six different cell distributions corresponding to a combination of the cell data including the first to third bits MSB, CSB, and LSB.

[0031] In some embodiments, 5-bit data may be encoded into 6-bit data through an encoding operation. In an embodiment, the 6-bit data may include data including first to sixth bits QSB, CSB_1, PSB, MSB, CSB_0, and LSB. More specifically, the data including the first bit QSB

of the 6-bit data may correspond to the data including the first bit QSB of the 5-bit data. The data including the second and fifth bits CSB_1 and CSB_0 of the 6-bit data may correspond to the data including the fourth bit CSB of the 5-bit data. The data including the third bit PSB of the 6-bit data may correspond to the data including the second bit PSB of the 5-bit data. The data including the fourth bit MSB of the 6-bit data may correspond to the data including the third bit MSB of the 5-bit data. The data including the sixth bit LSB of the 6-bit data may correspond to the data including the fifth bit LSB of the 5-bit data.

10 **[0032]** The first memory cell (i.e., the odd plug cell) may store the data including the first to third bits QSB, CSB_1, and PSB, among the 6-bit data, as the cell data including the first to third bits MSB, CSB, and LSB. In an embodiment, the first memory cell (i.e., the odd plug cell) may store the data including the first bit QSB, among the 6-bit data, as the cell data including the first bit MSB. The first memory cell (i.e., the odd plug cell) may store the data including the second bit CSB_1, among the 6-bit data, as the cell data including the second bit CSB. The first memory cell (i.e., the odd plug cell) may store the data including the third bit PSB, among the 6-bit data, as the cell data including the third bit LSB.

20 **[0033]** The second memory cell (i.e., the even plug cell) may store the data including the fourth to sixth bits MSB, CSB_0, and LSB, among the 6-bit data, as the cell data including the first to third bits MSB, CSB, and LSB. In an embodiment, the second memory cell (i.e., the even

plug cell) may store the data including the fourth bit MSB, among the 6-bit data, as the cell data including the first bit MSB. The second memory cell (i.e., the even plug cell) may store the data including the fifth bit CSB_0, among the 6-bit data, as the cell data including the second bit CSB. The second memory cell (i.e., the even plug cell) may store the data including the sixth bit LSB, among the 6-bit data, as the cell data including the third bit LSB.

[0034] The data including the first to third bits MSB, CSB, and LSB of the first and second memory cells (i.e., the odd plug cell and the even plug cell) may be restored to the data including the first to fifth bits QSB, PSB, MSB, CSM, and LSB through a decoding operation.

[0035] For example, the cell data including the first to third bits MSB, CSB, and LSB that have been stored in the first memory cell (i.e., the odd plug cell) may correspond to the first to third bits QSB, CSB_1, and PSB of the 6-bit data, respectively. Furthermore, the cell data including the first to third bits MSB, CSB, and LSB that have been stored in the second memory cell (i.e., the even plug cell) may correspond to the fourth to sixth bits MSB, CSB_0, and LSB of the 6-bit data, respectively. The 6-bit data may be decoded into the 5-bit data through a decoding operation.

[0036] FIG. 3 is a diagram for describing reading of data from a memory cell by a semiconductor device according to an embodiment of the present disclosure.

[0037] As in the description of FIG. 2, the semiconductor device

according to an embodiment of the present disclosure may encode 5-bit data into 6-bit data, may store data including 3 bits (e.g., QSB, CSB_1, and PSB), among the data including the 6 bits (i.e., QSB, CSB_1, PSB, MSB, CSB_0, and LSB), in the first memory cell (i.e., the odd plug cell), and may store the data including the remaining 3 bits (e.g., MSB, CSB_0, and LSB) in the second memory cell (i.e., the even plug cell). In an embodiment, at least one of the cell data including the first to third bits MSB, CSB, and LSB that are stored in each of the first and second memory cells (i.e., the odd plug cell and the even plug cell) may be encoded data. Furthermore, at least one of the cell data including the first to third bits MSB, CSB, and LSB that are stored in each of the first and second memory cells (i.e., the odd plug cell and the even plug cell) may include information in relation to whether encoded data is included in the cell data including the first to third bits MSB, CSB, and LSB that have been stored in each memory cell (i.e., the odd plug cell or the even plug cell).

[0038] Referring to FIG. 3, a combination of the data including the second and fifth bits CSB_1 and CSB_0, among the 6-bit data, which have been stored in the second bits CSB of the first and second memory cells (i.e., the odd plug cell and the even plug cell), respectively, may include the data including the fourth bit CSB, among the 5-bit data. Furthermore, a combination of the data including the second and fifth bits CSB_1 and CSB_0, among the 6-bit data, which have been stored as the second bits CSB in the first and second memory cells (i.e., the

odd plug cell and the even plug cell), respectively, may include, as coding data, information (Coding O or Coding X) in relation to whether the cell data including the first to third bits MSB, CSB, and LSB that have been stored in each of the first and second memory cells (i.e., the odd plug cell and the even plug cell) have been encoded.

[0039] For example, if the second and fifth bits CSB_1 and CSB_0 of the 6-bit data, which have been stored as the second bits CSB in the first and second memory cells (i.e., the odd plug cell and the even plug cell), respectively, have different data distributions, that is, different data values, the level of coding data may be a low (0) level. When the level of the coding data is a low level, this may mean that at least one of the first to third bits MSB, CSB, and LSB of the cell data, which have been stored in each of the first and second memory cells (i.e., the odd plug cell and the even plug cell), includes encoded data.

[0040] If the second and fifth bits CSB_1 and CSB_0 of the 6-bit data, which have been stored as the second bits CSB in the first and second memory cells (i.e., the odd plug cell and the even plug cell), respectively, have the same data distribution, that is, the same data value, the level of coding data may be a high (1) level. When the level of the coding data is a high level, this may mean that the first to third bits MSB, CSB, and LSB of the cell data, which have been stored in each of the first and second memory cells (i.e., the odd plug cell and the even plug cell), do not include encoded data.

[0041] If the level of the data including the second bit CSB_1 of the 6-

bit data, which has been stored as the second bit CSB in the first memory cell (i.e., the odd plug cell), is a low level and the level of the data including the fifth bit CSB_0 of the 6-bit data, which has been stored as the second bit CSB in the second memory cell (i.e., the even plug cell), is a high level, or if the level of the data including the second bit CSB_1 of the 6-bit data, which has been stored as the second bit CSB in the first memory cell (i.e., the odd plug cell), is a low level and the level of the data including the fifth bit CSB_0 of the 6-bit data, which has been stored as the second bit CSB in the second memory cell (i.e., the even plug cell), is a low level, the data including the fourth bit CSB of the 5-bit data may be data having a low level.

[0042] If the level of the data including the second bit CSB_1 of the 6-bit data, which has been stored as the second bit CSB in the first memory cell (i.e., the odd plug cell), is a high level and the level of the data including the fifth bit CSB_0 of the 6-bit data, which has been stored as the second bit CSB in the second memory cell (i.e., the even plug cell), is a low level, or if the level of the data including the second bit CSB_1 of the 6-bit data, which has been stored as the second bit CSB in the first memory cell (i.e., the odd plug cell), is a high level and the level of the data including the fifth bit CSB_0 of the 6-bit data, which has been stored as the second bit CSB in the second memory cell (i.e., the even plug cell), is a high level, the data including the fourth bit CSB of the 5-bit data may be data having a high level.

[0043] As described above, the semiconductor device according to an

embodiment of the present disclosure may perform an encoding operation and a decoding operation on data including specific bits CSB, among original data (i.e., the 5-bit data), and coding data, based on a combination of the data including the bits CSB_1 and CSB_0 that have
5 been stored as the specific bits CSB in the first and second memory cells (i.e., the odd plug cell and the even plug cell), respectively.

[0044] FIG. 4A, FIG. 4B and FIG. 4C are a diagram for describing an encoding operation of a semiconductor device according to an embodiment of the present disclosure.

10 **[0045]** FIG. 4A, FIG. 4B and FIG. 4C illustrate an encoding operation of the semiconductor device according to an embodiment of the present disclosure, for storing the data including the 5 bits QSB, PSB, MSB, CSB, and LSB (i.e., the 5-bit data) in the first and second memory cells (i.e., the odd plug cell and the even plug cell) by distributing the data.

15 **[0046]** Referring to FIG. 4A, the data including the 5 bits QSB, PSB, MSB, CSB, and LSB may include 32 different data patterns.

[0047] Referring to FIG. 4B, the data including the 6 bits QSB, CSB_1, PSB, MSB, CSB_0, and LSB may overlappingly include data including a specific bit CSB, among the data including the 5 bits QSB, PSB, MSB, CSB, and LSB. In an embodiment, the data including the second and
20 fifth bits CSB_1 and CSB_0, among the data including the 6 bits (i.e., QSB, CSB_1, PSB, MSB, CSB_0, and LSB) (i.e., the 6-bit data), may have the same data values as the data including the fourth bit CSB, among the data including the 5 bits QSB, PSB, MSB, CSB, and LSB.

Therefore, the first bit QSB of the 6-bit data may correspond to the first bit QSB of the 5-bit data. The second and fifth bits CSB_1 and CSB_0 of the 6-bit data may correspond to the fourth bit CSB of the 5-bit data. The third bit PSB of the 6-bit data may correspond to the second bit PSB of the 5-bit data. The fourth bit MSB of the 6-bit data may correspond to the third bit MSB of the 5-bit data. The sixth bit LSB of the 6-bit data may correspond to the fifth bit LSB of the 5-bit data.

[0048] The first memory cell (i.e., the odd plug cell) may store the data including the 3 bits (i.e., QSB, CSB_1, and PSB), among the data including the 6 bits (i.e., QSB, CSB_1, PSB, MSB, CSB_0, and LSB). The second memory cell (i.e., the even plug cell) may store the data including the 3 bits (i.e., MSB, CSB_0, and LSB), among the data including the 6 bits (i.e., QSB, CSB_1, PSB, MSB, CSB_0, and LSB). In an embodiment, each of the first and second memory cells (i.e., the odd plug cell and the even plug cell) might not have a cell distribution of a data pattern (0, 0, 1) or (0, 0, 0). The data pattern for the cell distribution, which is not stored by each of the first and second memory cells (i.e., the odd plug cell and the even plug cell), may be named a program inhibition data pattern (0, 0, 1) or (0, 0, 0).

[0049] In some embodiments, the program inhibition data pattern (0, 0, 1) or (0, 0, 0) according to a cell distribution, which is not stored by the first memory cell (i.e., the odd plug cell), may be encoded into a data pattern of a cell distribution, which may be stored by the first memory cell (i.e., the odd plug cell), and may be stored in the first

memory cell (i.e., the odd plug cell). Furthermore, the program inhibition data pattern (0, 0, 1) or (0, 0, 0) according to a cell distribution, which is not stored by the second memory cell (i.e., the even plug cell), may be encoded into a data pattern of a cell distribution, which may be stored by the second memory cell (i.e., the even plug cell), and may be stored in the second memory cell (i.e., the even plug cell).

[0050] Referring to FIG. 4C, the program inhibition data patterns (0, 0, 1) and (0, 0, 0) that is not stored in the first memory cell (i.e., the odd plug cell) may be encoded into (1, 0, 1) and (1, 0, 0), respectively. The program inhibition patterns (0, 0, 1) and (0, 0, 0) that are not stored in the second memory cell (i.e., the even plug cell) may be encoded into (1, 0, 1) or (1, 1, 1) and (1, 0, 0) or (1, 1, 0), respectively. In an embodiment, if encoded data is to be stored in the first memory cell (i.e., the odd plug cell), the bits MSB and CSB_0, among the 3 bits MSB, CSB_0, and LSB to be stored in the second memory cell (i.e., the even plug cell), may be inverted. If encoded data is to be stored in the second memory cell (i.e., the even plug cell), the bits QSB and CSB_1, among the 3 bits QSB, CSB_1, and PSB to be stored in the first memory cell (i.e., the odd plug cell), may be inverted.

[0051] As a result, the semiconductor device according to an embodiment of the present disclosure can encode, into 32 different patterns, the data including the 3 bits QSB, CSB_1, and PSB to be stored in the first memory cell (i.e., the odd plug cell) and the data

including the 3 bits MSB, CSB_0, and LSB to be stored in the second memory cell (i.e., the even plug cell) without including the program inhibition data pattern (0, 0, 1) or (0, 0, 0) in each of the 3 bits QSB, CSB_1, and PSB and the 3 bits MSB, CSB_0, and LSB, as shown in FIG.

5 4C.

[0052] FIG. 5 is a diagram for describing an operation of a page buffer with respect to an encoding operation of the semiconductor device according to an embodiment of the present disclosure.

[0053] Referring to FIG. 5, a page buffer PB may include first to sixth
10 latches Latch1, Latch2, Latch3, Latch4, Latch5, and Latch6. The first to sixth latches Latch1, Latch2, Latch3, Latch4, Latch5, and Latch6 may store the data including the 6 bits QSB, CSB_1, PSB, MSB, CSB_0, and LSB, respectively. In an embodiment, the bits LSB, CSB_0, and MSB that are stored in the first to third latches Latch1, Latch2, and Latch3,
15 respectively, may be programmed into the second memory cell (i.e., the even plug cell). The bits PSB, CSB_1, and QSB that are stored in the fourth to sixth latches Latch4, Latch5, and Latch6, respectively, may be programmed into the first memory cell (i.e., the odd plug cell).

[0054] In some embodiments, when the 5-bit data is received as shown
20 in FIG. 4A, the page buffer PB may store the 6-bit data by overlapping the 5-bit data and a specific bit CSB, among the 5-bit data, as shown in FIG. 4B. In an embodiment, the first latch Latch1 may store the bit LSB, among the 5-bit data. The second latch Latch2 may store the bit CSB, among the 5-bit data, as a bit CSB_0. The third latch Latch3 may

store the bit MSB, among the 5-bit data. The fourth latch Latch4 may store the bit PSB, among the 5-bit data. The fifth latch Latch5 may store the bit CSB, among the 5-bit data, as a bit CSB_1. The sixth latch Latch6 may store the bit QSB, among the 5-bit data.

5 **[0055]** The data including each of the bits QSB, CSB_1, PSB, MSB, CSB_0, and LSB that have been stored in the page buffer PB may be encoded as in FIG. 4C. The value of each of the bits that have been stored in the first to sixth latches Latch1 to Latch6 of the page buffer PB may be inverted or maintained by a control circuit (110 in FIG. 11).
10 Therefore, the data including the bits QSB, CSB_1, PSB, MSB, CSB_0, and LSB that have been stored in the page buffer PB may be encoded as shown in FIG. 4C by the control circuit.

15 **[0056]** As shown in FIG. 4C, the page buffer PB that has stored the encoded data including the 6 bits may program data including 3 bits, among the 6 bits, in each of the first and second memory cells (i.e., the odd plug cell and the even plug cell). For example, the data including the 3 bits that have been stored in the first to third latches Latch1 to Latch3 may be programmed into the second memory cell (i.e., the even plug cell). The data including the 3 bits that have been stored in the
20 fourth to sixth latches Latch4 to Latch6 may be programmed into the first memory cell (i.e., the odd plug cell).

[0057] FIG. 6 is a diagram for schematically describing input and output of data by a semiconductor device according to another embodiment of the present disclosure.

[0058] Referring to FIG. 6, 5-bit original data may include data including first to fifth bits QSB, PSB, MSB, CSB, and LSB. In an embodiment, each of the first and second memory cells (i.e., the odd plug cell and the even plug cell) may have six different cell distributions corresponding to a combination of the data including 3 bits MSB, CSB, and LSB.

[0059] In some embodiments, the 5-bit original data may be encoded into 5-bit conversion data through an encoding operation. In an embodiment, the 5-bit conversion data may include the data including first to fifth bits QSB, CSB_1, MSB, CSB_0, and LSB. More specifically, the first bit QSB of the 5-bit conversion data may correspond to the first bit QSB of the 5-bit original data. The second and fourth bits CSB_1 and CSB_0 of the 5-bit conversion data may correspond to the fourth bit CSB of the 5-bit original data. The third bit MSB of the 5-bit conversion data may correspond to the third bit MSB of the 5-bit original data. The fifth bit LSB of the 5-bit conversion data may correspond to the fifth bit LSB of the 5-bit original data.

[0060] The second memory cell (i.e., the even plug cell) may store the fourth to sixth bits MSB, CSB_0, and LSB, among the 5-bit conversion data, as the first to third bits MSB, CSB, and LSB of cell data, respectively.

[0061] The first memory cell (i.e., the odd plug cell) may store the first and second bits QSB and CSB_1, among the 5-bit conversion data, and the second bit PSB, among the 5-bit original data, as the first to third

bits MSB, CSB, and LSB of the cell data, respectively.

[0062] The cell data including the first to third bits MSB, CSB, and LSB of each of the first and second memory cells (i.e., the odd plug cell and the even plug cell) may be restored to the 5-bit original data including the first to fifth bits QSB, PSB, MSB, CSB, and LSB through a decoding operation.

[0063] In some embodiments, the first and third bits MSB and LSB of the cell data that have been stored in the first memory cell (i.e., the odd plug cell) may correspond to the first and second bits QSB and PSB of the 5-bit original data, respectively. The first and third bits MSB and LSB of the cell data that have been stored in the second memory cell (i.e., the even plug cell) may correspond to the third and fifth bits MSB and LSB of the 5-bit original data, respectively. A combination of the cell data including the second bit CSB that has been stored in the first memory cell (i.e., the odd plug cell) and the cell data including the second bit CSB that has been stored in the second memory cell (i.e., the even plug cell) may correspond to the fourth bit CSB of the 5-bit original data. More specifically, based on a combination of the data including the second bits CSB that have been stored in the first and second memory cells (i.e., the odd plug cell and the even plug cell), a value of the data including the fourth bit CSB of the 5-bit original data may be determined, and the data including the first and fifth bits QSB and LSB of the 5-bit original data may be inverted or maintained.

[0064] FIG. 7A, FIG. 7B and FIG. 7C are a diagram for describing an

encoding operation of a semiconductor device according to another embodiment of the present disclosure.

[0065] FIG. 7A, FIG. 7B and FIG. 7C illustrate an encoding operation of the semiconductor device according to another embodiment of the present disclosure, for converting 5-bit original data into 5-bit conversion data. In some embodiments, the 5-bit original data may include first to fifth bits QSB, PSB, MSB, CSB, and LSB. The 5-bit conversion data may include first to fifth bits QSB, CSB_1, MSB, CSB_0, and LSB.

10 **[0066]** The first memory cell (i.e., the odd plug cell) may store the data including the first and second bits QSB and CSB_1, among the 5-bit conversion data QSB, CSB_1, MSB, CSB_0, and LSB on which encoding has been completed, and the second bit PSB of the 5-bit original data. The second memory cell (i.e., the even plug cell) may store the data
15 including the third to fifth bits (i.e., MSB, CSB_0, and LSB), among the 5-bit conversion data QSB, CSB_1, MSB, CSB_0, and LSB on which encoding has been completed. In an embodiment, each of the bits MSB, CSB, and LSB of each of the first and second memory cells (i.e., the odd plug cell and the even plug cell) might not have a cell
20 distribution of the data patterns (0, 0, 1) and (0, 0, 0). In an embodiment, the data pattern for the cell distribution that is now stored by each of the first and second memory cells (i.e., the odd plug cell and the even plug cell) may be named a program inhibition data pattern (0, 0, 1) or (0, 0, 0).

[0067] Referring to FIG. 7A, the 5-bit original data QSB, PSB, MSB, CSB, and LSB may include 32 different data patterns.

[0068] Referring to FIG. 7B, the first bit QSB of the 5-bit conversion data may correspond to the first bit QSB of the 5-bit original data. The
5 second bit CSB_1 of the 5-bit conversion data may correspond to the fourth bit CSB of the 5-bit original data. The third bit MSB of the 5-bit conversion data may correspond to the third bit MSB of the 5-bit original data. The fourth bit CSB_0 of the 5-bit conversion data may correspond to the fourth bit CSB of the 5-bit original data. The fifth bit
10 LSB of the 5-bit conversion data may correspond to the fifth bit LSB of the 5-bit original data. As a result, the first bits QSB, third bits MSB, and fifth bits LSB of the 5-bit conversion data and those of the 5-bit original data illustrated in FIG. 7B may have the same data. The second and fourth bits CSB_1 and CSB_0 of the 5-bit conversion data
15 may have the same data as the fourth bit CSB of the 5-bit original data.

[0069] Each of the first and second memory cells (i.e., the odd plug cell and the even plug cell) might not have a cell distribution of the data patterns (0, 0, 1) and (0, 0, 0). In an embodiment, each of the data patterns (0, 0, 1) and (0, 0, 0) may correspond to the bits MSB, CSB,
20 and LSB of cell data. That is, in each of the first and second memory cells (i.e., the odd plug cell and the even plug cell), a data pattern when both the levels of the bits MSB and CSB, among the bits MSB, CSB, and LSB of the cell data to be programmed, have a low (0) level may be a program inhibition data pattern.

[0070] Accordingly, a data pattern when both the levels of the first and second bits QSB and CSB_1 of the 5-bit conversion data have a low (0) level or when both the levels of the third and fourth bits MSB and CSB_0 of the 5-bit conversion data have a low (0) level may be a program inhibition data pattern for the first and second memory cells (i.e., the odd plug cell and the even plug cell).

[0071] Referring to FIG. 7C, when the levels of the first and second bits QSB and CSB_1 to be stored in the first memory cell (i.e., the odd plug cell) as the cell data, among the 5-bit conversion data, are (0, 0), the data including the first bit QSB and the third bit MSB, among the 5-bit conversion data, may be encoded (e.g., the data may be inverted), and the fourth bit CSB_0 of the 5-bit conversion data may be inverted. When the levels of the third and fourth bits MSB and CSB_0 of the 5-bit conversion data to be stored in the second memory cell (i.e., the even plug cell) as the cell data are (0, 0), the data including the third bit MSB and the first bit QSB, among the 5-bit conversion data, may be encoded (e.g., the data may be inverted), and the second bit CSB_1 of the 5-bit conversion data may be inverted.

[0072] Results of an encoding operation of the semiconductor device according to another embodiment of the present disclosure, which have been illustrated in FIG. 7C, may be the same as results except the third bit PSB, among the 6-bit conversion data QSB, CSB_1, PSB, MSB, CSB_0, and LSB in FIG. 4C.

[0073] In an encoding operation of the semiconductor device according

to another embodiment of the present disclosure, 5-bit conversion data may be generated by performing the encoding operation on the 4 bits QSB, MSB, CSB, and LSB except a specific bit PSB, among the 5-bit original data QSB, PSB, MSB, CSB, and LSB. The 3 bits MSB, CSB_0, and LSB, among the 5-bit conversion data QSB, CSB_1, MSB, CSB_0, and LSB on which the encoding operation has been completed, may be programmed into one of the pair of memory cells. Thereafter, the remaining 2 bits QSB and CSB_1, among the 5-bit conversion data QSB, CSB_1, MSB, CSB_0, and LSB, and the specific bit PSB of the 5-bit original data may be programmed into the other of the pair of memory cells.

[0074] FIG. 8 is a diagram for describing an operation of a page buffer with respect to an encoding operation of a semiconductor device according to another embodiment of the present disclosure.

[0075] Referring to FIG. 8, a page buffer PB may include first to fifth latches Latch1, Latch2, Latch3, Latch4, and Latch5. The first to fifth latches Latch1, Latch2, Latch3, Latch4, and Latch5 may store the bits of 5-bit conversion data QSB, CSB_1, MSB, CSB_0, and LSB, respectively. In an embodiment, LSB, CSB_0, and MSB that are stored in the first to third latches Latch1, Latch2, and Latch3 may be stored as the cell data, and may be programmed into the second memory cell (i.e., the even plug cell). Thereafter, the bit PSB, among the 5-bit original data, may be stored in the third latch Latch3. The bit PSB that has been stored in the third latch Latch3 and the bits CSB_1 and QSB

that have been stored in the fourth and fifth latches Latch4 and Latch5 may be programmed into the first memory cell (i.e., the odd plug cell) as the cell data.

[0076] In an embodiment, when the 5-bit original data is received as shown in FIG. 7A, the page buffer PB may store the data including the remaining 4 bits LSB, CSB, MSB, and QSB except the bit PSB, among the 5-bit original data, as shown in FIG. 7B. In an embodiment, the first latch Latch1 may store the data including the bit LSB, among the 5-bit original data. The second latch Latch2 may store the data including the bit CSB, among the 5-bit original data, as the data including the bit CSB_0. The third latch Latch3 may store the data including the bit MSB, among the 5-bit original data. The fourth latch Latch4 may store the data including the bit CSB, among the 5-bit original data, as the data including the bit CSB_1. The fifth latch Latch5 may store the data including the bit QSB, among the 5-bit original data.

[0077] The data including each of the bits QSB, CSB_1, MSB, CSB_0, and LSB that have been stored in the page buffer PB may be encoded as shown in FIG. 7C. The values of the data that have been stored in the first to fifth latches Latch1 to Latch5 of the page buffer PB may be controlled to be inverted and maintained. Therefore, the data including each of the bits QSB, CSB_1, MSB, CSB_0, and LSB that have been stored in the page buffer PB may be encoded through the control circuit as shown in FIG. 7C. In an embodiment, the control circuit may

encode the data including the bits CSB_0 and MSB that have been stored in the second and third latches Latch2 and Latch3, based on the bits CSB_1 and QSB that have been stored in the fourth and fifth latches Latch4 and Latch_5 of the page buffer PB. In an embodiment, the control circuit may encode the data including the bits CSB_1 and QSB that have been stored in the fourth and fifth latches Latch4 and Latch5, based on the bits CSB_0 and MSB that have been stored in the second and third latches Latch2 and Latch3 of the page buffer PB. After the encoding operation is completed, the bits LSB, CSB_0, and MSB that have been stored in the first to third latches Latch1, Latch2, and Latch3 may be programmed into the second memory cell (i.e., the even plug cell) as the cell data. After the second memory cell (i.e., the even plug cell) is programmed, the third latch Latch3 may store the bit PSB of the 5-bit original data. The bits PSB, CSB_1, and QSB that have been stored in the third to fifth latches Latch3, Latch4, and Latch5 may be programmed into the first memory cell (i.e., the odd plug cell) as the cell data.

[0078] When FIGS. 5 and 8 are compared, the semiconductor device according to another embodiment of the present disclosure can perform the same encoding operation while reducing the number of latches that are included in the page buffer.

[0079] FIGS. 9 and 10 are flowcharts for describing an operating method of the semiconductor device according to another embodiment of the present disclosure.

[0080] FIG. 9 illustrates a program method of the semiconductor device according to another embodiment of the present disclosure.

[0081] As shown in FIG. 9, the program method of the semiconductor device according to another embodiment of the present disclosure may include a first data reception operation S10, an encoding operation S20, a first program operation S30, a second data reception operation S40, and a second program operation S50.

[0082] The first data reception operation S10 may include an operation of receiving 4-bit original data, among 5-bit original data. In an embodiment, the 5-bit original data may include bits QSB, PSB, MSB, CSB, and LSB. The 4-bit original data may include bits QSB, MSB, CSB, and LSB except the bit PSB.

[0083] The encoding operation S20 may include an operation of encoding the 4-bit original data into 5-bit conversion data. The 5-bit conversion data may include bits QSB, CSB_1, MSB, CSB_0, and LSB. The bits QSB, MSB, and LSB of the 5-bit conversion data may correspond to the bits QSB, MSB, and LSB of the 4-bit original data, respectively. The bits CSB_1 and CSB_0 of the 5-bit conversion data may correspond to the bit CSB of the 4-bit original data. If the bits QSB and CSB_1, among the 5-bit conversion data, correspond to a program inhibition data pattern, an encoding operation of inverting the bits QSB, MSB, and CSB_0, among the 5-bit conversion data, may be performed. If the bits MSB and CSB_0, among the 5-bit conversion data, correspond to a program inhibition data pattern, an encoding

operation of inverting the bits QSB, MSB, and CSB_1, among the 5-bit conversion data, may be performed. A method of encoding the 5-bit conversion data will be described in detail with reference to FIG. 10.

[0084] The first program operation S30 may include an operation of programming the data including the 3 bits MSB, CSB_0, and LSB on which the encoding has been completed, among the 5-bit conversion data, into the second memory cell (i.e., the even plug cell) as cell data.

[0085] The second data reception operation S40 may include an operation of receiving the remaining 1-bit original data, among the 5-bit original data. In an embodiment, the remaining 1-bit original data may include the bit PSB that has not been received in the first data reception operation S10, among the 5-bit original data.

[0086] The second program operation S50 may include an operation of programming, into the first memory cell (i.e., the odd plug cell), the conversion data including the 2 bits that have not been used in the first program operation S30, among the 5-bit conversion data, and the remaining 1-bit original data that has been received in the second data reception operation S40, as the cell data. In an embodiment, the conversion data including the 2 bits may include the bits QSB and CSB_1, and the remaining 1-bit original data may include the bit PSB.

[0087] FIG. 10 illustrates an encoding method of the semiconductor device according to another embodiment of the present disclosure.

[0088] Referring to FIG. 10, the encoding method of the semiconductor device according to another embodiment of the present disclosure may

include a data reception operation S101, a 5-bit conversion data generation operation S201, a first encoding-required determination operation S301, a first encoding operation S311, a first inversion operation S321, a second encoding-required determination operation S401, a second encoding operation S411, and a second inversion operation S421.

[0089] The data reception operation S101 may include an operation of receiving 4-bit original data including bits LSB, CSB, MSB, and QSB among 5-bit original data including bits LSB, CSB, MSB, PSB, and QSB.

[0090] The 5-bit conversion data generation operation S201 may include an operation of generating 5-bit conversion data including bits LSB, CSB_0, MSB, CSB_1, and QSB. In an embodiment, bits CSB_0 and CSB_1 of 5-bit conversion data may be generated by copying the bit CSB, among the 4-bit original data. In an embodiment, the 5-bit conversion data may include bits LSB, CSB_0, MSB, CSB_1, and QSB. The bits LSB, MSB, and QSB of the 5-bit conversion data may correspond to the LSB, MSB, and QSB of the 4-bit original data, respectively. The bits CSB_0 and CSB_1 of the 5-bit conversion data may correspond to the bit CSB of the 4-bit original data.

[0091] The first encoding-required determination operation S301 may include an operation of determining whether the data including the bits CSB_1 and QSB of the 5-bit conversion data need to be encoded. For example, the first encoding-required determination operation S301 may include an operation of determining whether the bits CSB_1 and

QSB of the 5-bit conversion data correspond to a program inhibition data pattern (0, 0).

[0092] If it is determined that the data including the bits CSB_1 and QSB need to be encoded (Y) in the first encoding-required determination operation S301, the first encoding operation S311 may be performed. If it is determined that the data including the bits CSB_1 and QSB do not need to be encoded (N) in the first encoding-required determination operation S301, the second encoding-required determination operation S401 may be performed.

[0093] The first encoding operation S311 may include an operation of encoding the data including the bits MSB and QSB, among the 5-bit conversion data. For example, the first encoding operation S311 may include an operation of inverting the bits MSB and QSB of the 5-bit conversion data.

[0094] The first inversion operation S321 may include an operation of inverting the bit CSB_0 of the 5-bit conversion data. Through the first inversion operation S321, information indicating that the data including the bits CSB_1 and QSB to be programmed into the first memory cell (i.e., the odd plug cell) have been encoded may be included in the data including the bit CSB_0 to be stored in the second memory cell (i.e., the even plug cell).

[0095] The second encoding-required determination operation S401 may include an operation of determining whether the data including the bits CSB_0 and MSB, among the 5-bit conversion data, need to be

encoded. For example, the second encoding-required determination operation S401 may include an operation of determining whether the bits CSB_0 and MSB of the 5-bit conversion data correspond to the program inhibition data pattern (0, 0).

- 5 **[0096]** If it is determined that the data including the bits CSB_0 and MSB, among the 5-bit conversion data, need to be encoded (Y) in the second encoding-required determination operation S401, the second encoding operation S411 may be performed.

10 **[0097]** The second encoding operation S411 may include an operation of encoding the data including the bits MSB and QSB of the 5-bit conversion data. For example, the second encoding operation S411 may include an operation of inverting the bits MSB and QSB of the 5-bit conversion data.

15 **[0098]** The second inversion operation S421 may include an operation of inverting the bit CSB_1 of the 5-bit conversion data. Through the second inversion operation S421, information indicating that the data including the bits CSB_0 and MSB to be programmed into the second memory cell (i.e., the even plug cell) have been encoded may be included in the bit CSB_1 to be stored in the first memory cell (i.e., the
20 odd plug cell).

[0099] FIG. 11 is a block diagram of a semiconductor device 100 according to an embodiment of the present disclosure.

[00100] Referring to FIG. 11, the semiconductor device 100 may include the control circuit 110, a page buffer group 120, a voltage generation

circuit 130, a line driving circuit 140, and a memory cell array 150.

[00101] The control circuit 110 may program 5-bit data that are received from the outside into the pair of memory cells that is included in the memory cell array 150 by distributing the 5-bit data, through control of
5 the page buffer group 120, the voltage generation circuit 130, and the line driving circuit 140.

[00102] The control circuit 110 may generate a page buffer control signal PB_ctrl, based on a command signal CMD and an address signal ADD that are received from the outside (e.g., a host), and may provide
10 the page buffer control signal PB_ctrl to the page buffer group 120. Furthermore, the control circuit 110 may generate the page buffer control signal PB_ctrl, based on 2-bit data that are provided by page buffers PB1, PB2 to PBm, and may provide the page buffer control signal PB_ctrl to the page buffer group 120.

15 **[00103]** The control circuit 110 may generate a voltage control signal V_ctrl based on the command signal CMD, and may provide the voltage control signal V_ctrl to the voltage generation circuit 130.

[00104] The control circuit 110 may generate a driving address signal ADD_d based on the command signal CMD and the address signal ADD,
20 and may provide the driving address signal ADD_d to the line driving circuit 140.

[00105] The page buffer group 120 may include the plurality of page buffers PB1, PB2 to PBm. The plurality of page buffers PB1, PB2 to PBm may be connected to a plurality of bit lines BL1, BL2 to BLm,

respectively, where m is a natural number. Each of the plurality of bit lines BL, BL2 to BL m may be connected to at least a pair of memory cells. Each of the plurality of page buffers PB1, PB2 to PB m may include a plurality of latches. Each of the plurality of page buffers PB1, PB2 to PB m may store data in the plurality of latches based on the page buffer control signal PB_ctrl, and may maintain or invert the stored data. Furthermore, each of the plurality of page buffers PB1, PB2 to PB m may program, into the pair of memory cells, the data that have been stored in the plurality of latches through the bit line BL.

Furthermore, each of the plurality of page buffers PB1, PB2 to PB m may sense the data that have been programmed into the pair of memory cells, may store the sensed data, and may output the stored sensed data. Accordingly, each of the plurality of page buffers PB1, PB2 to PB m may store data that has been received from the outside, may encode the stored data by inverting at least one bit data of the stored data based on the page buffer control signal PB_ctrl, and may program the data into the pair of memory cells by distributing the data, under the control of the control circuit 110. Furthermore, each of the plurality of page buffers PB1, PB2 to PB m may sense the data that have been stored in the pair of memory cells, may store the sensed data, may decode the stored sensed data by inverting at least one bit data of the stored sensed data based on the page control signal PB_ctrl, and may output the decoded data, under the control of the control circuit 110.

[00106] The voltage generation circuit 130 may generate internal voltages V_{int} having various voltage levels, based on the voltage control signal V_{ctrl}, and may provide the internal voltages V_{int} to the line driving circuit 140.

- 5 **[00107]** The line driving circuit 140 may drive first drain selection lines DSL_{Odd}, second drain selection line DSL_{Even}, word lines WL, and source selection lines SSL to the voltage levels of the internal voltages V_{int}, based on the driving address signal ADD_d.

- [00108]** The memory cell array 150 may include a plurality of memory
10 blocks BK1, BK2 to BK_n, where n is a natural number. Each of the plurality of memory blocks BK1, BK2 to BK_n may be selected by the word lines WL. The memory strings of the selected memory block may be connected to the plurality of page buffers PB1, PB2 to PB_m through the bit lines BL1, BL2 to BL_m. Furthermore, each of the plurality of
15 memory blocks BK1, BK2 to BK_n may include a plurality of memory strings to which a pair of memory cells has been connected in series. Each of the plurality of memory strings may include a drain selection transistor, a source transistor, and a dummy cell, in addition to a pair of memory cells that is connected in series to each string. The drain
20 selection transistor may include first drain selection transistors to which the first drain selection lines DSL_{Odd} are connected and second drain selection transistors to which the second drain selection lines DSL_{Even} are connected. Connection of the first drain selection lines DSL_{Odd} and the first drain selection transistors may select a first memory cell

(i.e., the odd plug cell), among the pair of memory cells (i.e., the odd plug cell and the even plug cell). Connection of the second drain selection lines DSL_Even and the second drain selection transistors may select a second memory cell (i.e., the even plug cell), among the pair of memory cells (i.e., the odd plug cell and the even plug cell).

[00109] The semiconductor device according to an embodiment of the present disclosure, which has been configured as described above, may store 4-bit original data, among 5-bit original data that are received from the outside, in the page buffer PB. The page buffer PB may convert, into 5-bit conversion data, the 4-bit original data that have been stored in the page buffer PB under the control of the control circuit 110. The page buffer PB may provide the control circuit 110 with 2-bit data, among the 5-bit conversion data. The control circuit 110 may generate the page buffer control signal PB_ctrl for the encoding of the 5-bit conversion data, based on the 2-bit data that are provided by the page buffer PB. The page buffer PB may encode the 5-bit conversion data based on the page buffer control signal PB_ctrl. The page buffer PB may program 3-bit data, among the 5-bit conversion data on which the encoding has been completed, into one of the pair of memory cells. Furthermore, the page buffer PB may store the remaining 1-bit original data, among the 5-bit original data, and may program the remaining 2-bit data, among the 5-bit conversion data on which the encoding has been completed, and the original 1-bit data into the other of the pair of memory cells.

[00110] Although embodiments according to the technical spirit of the present disclosure have been described above with reference to the accompanying drawings, the embodiments have been provided to merely describe embodiments according to the concept of the present disclosure, and the present disclosure is not limited to the 5 embodiments. A person having ordinary knowledge in the art to which the present disclosure pertains may substitute, modify, and change the embodiments in various ways without departing from the technical spirit of the present disclosure written in the following claims. Such 10 substitutions, modifications, and changes may be said to belong to the scope of the present disclosure. Furthermore, the embodiments may be combined to form additional embodiments.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

5 a page buffer comprising first to fifth latches, wherein the first to third latches and the fifth latch are configured to store 4-bit original data, among 5-bit original data, respectively, and the fourth latch is configured to store data identical with the data that has been stored in the second latch; and

10 a control circuit configured to determine a program inhibition pattern based on data that have been stored in two of the first to fifth latches and control the page buffer so that data that has been stored in at least one of the first to fifth latches is inverted based on the program inhibition pattern.

15 2. The semiconductor device of claim 1, wherein:

the 5-bit original data comprise first to fifth bits, and

the 4-bit original data comprise the first bit and the third to fifth bits.

20 3. The semiconductor device of claim 2, wherein:

the first latch stores the first bit of the 5-bit original data,

the second and fourth latches store the fourth bit of the 5-bit original data,

the third latch stores the third bit of the 5-bit original data, and

the fifth latch stores the fifth bit of the 5-bit original data.

4. The semiconductor device of claim 1, wherein the control circuit inverts or maintains the data that have been stored in the second latch, the third latch, and the fifth latch by determining whether the data that have been stored in the fourth latch and the fifth latch correspond to the program inhibition pattern.

5. The semiconductor device of claim 4, wherein the control circuit inverts the data that have been stored in the second latch, the third latch, and the fifth latch when it is determined that the data that have been stored in the fourth latch and the fifth latch correspond to the program inhibition pattern.

6. The semiconductor device of claim 4, wherein the control circuit maintains the data that have been stored in the second latch, the third latch, and the fifth latch when it is determined that the data that have been stored in the fourth latch and the fifth latch do not correspond to the program inhibition pattern.

7. The semiconductor device of claim 4, wherein the control circuit programs, into one of a pair of memory cells, the data that have been stored in the first to third latches.

8. The semiconductor device of claim 1, wherein the control circuit inverts or maintains the data that have been stored in the third to fifth latches by determining whether the data that have been stored in the second latch and the third latch correspond to the program inhibition pattern.

9. The semiconductor device of claim 8, wherein the control circuit inverts the data that have been stored in the third to fifth latches when it is determined that the data that have been stored in the second latch and the third latch correspond to the program inhibition pattern.

10. The semiconductor device of claim 9, wherein the control circuit maintains the data that have been stored in the third to fifth latches when it is determined that the data that have been stored in the second latch and the third latch do not correspond to the program inhibition pattern.

11. The semiconductor device of claim 8, wherein the control circuit programs, into one of a pair of memory cells, the data that have been stored in the first to third latches, and then stores, in the third latch, remaining 1-bit original data except for the 4-bit original data, among the 5-bit original data.

12. The semiconductor device of claim 11, wherein the control

circuit programs, into the other of the pair of memory cells, the data that have been stored in the third to fifth latches.

13. An operating method of a semiconductor device,
5 comprising:

receiving 4-bit original data, among 5-bit original data;

encoding the 4-bit original data into 5-bit conversion data;

programming 3-bit conversion data, among the 5-bit conversion data, into a first memory cell;

10 receiving remaining 1-bit original data, among the 5-bit original data; and

programming remaining 2-bit conversion data among the 5-bit conversion data and the remaining 1-bit original data, into a second memory cell.

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14. The method of claim 13, wherein the encoding of the 4-bit original data into the 5-bit conversion data comprises:

converting the 4-bit original data into the 5-bit conversion data,
and

20 encoding the 5-bit conversion data.

15. The method of claim 14, wherein the encoding of the 4-bit original data into the 5-bit conversion data further comprises generating the 5-bit conversion data including the 4-bit original data

and 1-bit additional data, and

Wherein the 1-bit additional data is the same data as a specific bit of the 4-bit original data.

5 16. An operating method of a semiconductor device, comprising:

 receiving 4-bit original data, among 5-bit original data;

 converting the 4-bit original data into 5-bit conversion data including 2-bit conversion data and remaining 3-bit conversion data;

10 determining whether the remaining 3-bit conversion data have been encoded based on the 2-bit conversion data; and

 determining whether the 2-bit conversion data have been encoded based on 2-bit data, among the remaining 3-bit conversion data.

15

 17. The method of claim 16, wherein:

 the 5-bit original data comprise first to fifth bits, and

 the 4-bit original data comprises the first bit and third to fifth bits of the 5-bit original data.

20

 18. The method of claim 17, wherein the converting of the 4-bit original data into the 5-bit conversion data comprises generating the second bit and fourth bit of the 5-bit conversion data which have the same value as the fourth bit of the 5-bit original data.

19. The method of claim 16, wherein:

the 5-bit conversion data comprise first to fifth bits, and

the determining of whether the remaining 3-bit conversion data

5 have been encoded based on the 2-bit conversion data comprises:

determining whether the first bit and second bit of the 5-bit
conversion data correspond to a program inhibition pattern,

encoding the first bit and third bit of the 5-bit conversion data
when it is determined that the first bit and second bit of the 5-bit

10 conversion data correspond to the program inhibition pattern, and

inverting the fourth bit of the 5-bit conversion data when it is
determined that the first bit and second bit of the 5-bit conversion data
correspond to the program inhibition pattern.

15 20. The method of claim 19, further comprising programming
the first to third bits, among the 5-bit conversion data, into one of a
pair of memory cells.

21. The method of claim 16, wherein:

20 the 5-bit conversion data comprise first to fifth bits, and

the determining of whether the 2-bit conversion data have been
encoded based on the 2-bit data comprises:

determining whether the third bit and fourth bit of the 5-bit
conversion data correspond to a program inhibition pattern,

encoding the first bit and third bit of the 5-bit conversion data when it is determined that the third bit and fourth bit of the 5-bit conversion data correspond to the program inhibition pattern, and

inverting the second bit of the 5-bit conversion data when it is
5 determined that the third bit and fourth bit of the 5-bit conversion data correspond to the program inhibition pattern.

22. The method of claim 21, further comprising programming the fourth and fifth bits, among the 5-bit conversion data, and
10 remaining 1-bit original data except for the 4-bit original data, among the 5-bit original data, in one of a pair of memory cells.