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"A Reference Voltage Generator".

The present invention relates to a reference voltage generator which is constructed of MISFETs (insulated gate type field effect transistors).

Two MISFETs whose gate electrodes are made of materials having work functions different from each other exhibit threshold voltages different from each other. The difference between the threshold voltages of the two MISFETs becomes equal to the difference of the work functions of the gate electrodes in the respective MISFETs. The threshold voltage difference can be utilized as a reference voltage. Since the reference voltage thus obtained has its value determined by the work function difference of the two gate electrodes, it is less liable to be influenced by bad effects attributed to dispersions in the characteristics of the circuit elements.

Accordingly, when fabricated in the form of an integrated circuit, a reference voltage generator

utilizing the work function difference produces a reference voltage of comparatively precise value in spite of comparatively great dispersions in the characteristics of various circuit elements in the integrated circuit.

As a result of research, we have discovered that the reference voltage exhibits a temperature dependence and a supply voltage dependence which are not negligible.

It is accordingly an object of this invention to provide a reference voltage generator which produces a reference voltage of stable level irrespective of temperature fluctuations.

According to the present invention there is provided a reference voltage generator including:

- (a) an output terminal;
- (b) a first MISFET which is supplied across its gate and source with a voltage between said output terminal and a reference point and which produces a drain - source current of a level corresponding to the voltage supplied across said gate and source;
- (c) a bias circuit generating first and second bias currents which have levels proportional to the drain - source current of said first MISFET;
- (d) a second MISFET which has a drain - source path coupled between a first node and said reference point, and a gate coupled to a drain thereof; the drain - source path being supplied with said first bias

current; and

(e) a third MISFET which has a gate coupled to said first node, a source coupled to said output terminal, and a drain, whose threshold voltage is made
5 a value smaller than that of said second MISFET and whose drain - source path is supplied with said second bias current;

whereby a voltage which corresponds to a difference between a threshold voltage of said second
10 MISFET and that of said third MISFET is supplied from said third MISFET to said output terminal.

The present invention will now be described in greater detail by way of examples with reference to the accompanying drawings, wherein:-

15 Figure 1 is a circuit diagram of a known reference voltage generator;

Figure 2 is a diagram showing the energy gap E_g of silicon and the temperature dependence thereof;

Figure 3 is a diagram showing the temperature
20 characteristics of the Fermi levels of n-type silicon and p-type silicon with impurity densities as parameters;

Figure 4 is a circuit diagram of a first preferred form of a reference voltage generator;

Figures 5A and 5B are sectional views of a
25 fraction of a CMOS IC;

Figures 6, 7 and 8 are circuit diagrams each showing second, third and fourth embodiments of

a reference voltage generator;

Figure 9 is a graph showing the characteristic curves of the circuits in Figure 1 and Figure 4;

Figures 10A, 10B and 10C are circuit diagrams each showing a current mirror circuit;

Figure 11 is a circuit diagram of a battery checker;

Figure 12 is an operating waveform diagram of the circuit in Figure 11; and

Figure 13 is a circuit diagram of a fifth embodiment of a reference voltage generator.

Our previously known reference voltage generator is shown in Figure 1.

The reference voltage generator comprises a circuit B which delivers a reference voltage V_{ref2} , and a circuit A which delivers a bias voltage V_{ref1} to be supplied to the circuit B.

In the circuit B, a pair of p-channel type MISFETs Q_{14}' and Q_{15}' have their gate electrodes made of polycrystalline silicon layers of conductivity type opposite to each other. That is, the MISFET Q_{14}' has its gate electrode made of an n-type polycrystalline silicon layer, whilst the MISFET Q_{15}' has its gate electrode made of a p-type polycrystalline silicon layer.

The reference voltage V_{ref2} to be delivered from the circuit B has a value which is close to the

difference ($V_{th1} - V_{th2}$) between the threshold voltage V_{th1} of the MISFET Q_{14} ' and the threshold voltage V_{th2} of the MISFET Q_{15} '. Since the threshold voltage difference ($V_{th1} - V_{th2}$) becomes equal to the difference between the Fermi level of the n-type polycrystalline silicon layer and that of the p-type polycrystalline silicon layer, the reference voltage V_{ref2} is at a value close to the Fermi level difference between the n-type polycrystalline silicon layer and the p-type polycrystalline silicon layer. In the case where a conductivity type-determining impurity in each of the n-type polycrystalline silicon layer and the p-type polycrystalline silicon layer is at a high density of, for example, 10^{18} atoms/cm³ or above, the Fermi level difference becomes a value close to the band gap of silicon. In this case the difference voltage V_{ref2} accordingly is at a value close to the band gap of silicon.

The output voltage V_{ref2} is stabilized irrespective of temperature fluctuations and supply voltage fluctuations as will be explained below.

The band gap of silicon has a temperature dependence. The physics of semiconductors is well known from the large quantity of publications available, one of the most important of which is "Physics of Semiconductor Devices" by S.M. SZE, published by John Wiley & Sons in 1969, especially

Chapter 2 "Physics and Properties of Semiconductors",
pp 11 - 65.

Page 24 of the above publication indicates
the relationships of several semiconductors between the
5 band gap E_g and the temperature, and Figure 2 of the
accompanying drawings reproduces the relationship of
silicon therefrom.

Likewise, the Fermi level of n-type silicon and
that of p-type silicon have temperature dependences.
10 Figure 3 illustrates the relationships between the Fermi
level and the temperature, of n-type and p-type silicon
materials at various impurity densities.

As will be understood by referring to Figure 2
and 3, the threshold voltage difference ($V_{th1} - V_{th2}$)
15 between the MISFETs Q_{14}' and Q_{15}' shown in Figure 1
involves the temperature dependence, and its value
decreases with a rise in temperature.

In the voltage generator of Figure 1,
therefore, the operating current of the MISFET Q_{14}' and
20 that of the MISFET Q_{15}' are deliberately unbalanced in
order that a substantial temperature compensation
voltage may be generated by the MISFETs Q_{14}' and Q_{15}' .
The current ratio between the operating current of
the MISFET Q_{14}' and that of the MISFET Q_{15}' is set at
25 an appropriate value by fixing the sizes of
MISFETs $Q_{11}' - Q_{13}'$ constituting a current mirror
circuit and by fixing the sizes of MISFETs Q_{16}' and
 Q_{17}' constituting another current mirror circuit.

The reference voltage generator shown in Figure 1 is also provided with a circuit similar to the circuit B, that is, the circuit A comprising MISFETs $Q_{10} - Q_{17}$, in order to reduce the supply voltage dependences of the input currents of the current mirror circuits comprising the MISFETs Q_{11}' , Q_{12}' . In the circuit A, the operating currents of the MISFETs Q_{14} and Q_{15} are equalized. Since the operating currents of the p-channel type MISFET Q_{14} with a gate electrode made of an n-type polycrystalline silicon layer and the p-channel type MISFET Q_{15} with a gate electrode made of a p-type polycrystalline silicon layer are made equal to each other, the output voltage V_{ref1} of the circuit A consequently becomes a constant value unaffected by fluctuations in bias currents even when the bias currents which are delivered from the MISFETs Q_{12} and Q_{13} in the circuit A have fluctuated due to fluctuations in the supply voltage V_{DD} . That is, the output voltage V_{ref1} is fixed at a value equal to the difference between the Fermi levels of n-type silicon and p-type silicon. Since an n-channel type MISFET Q_{10}' in the circuit B is supplied with the constant bias voltage V_{ref1} across the gate and source thereof, it produces a constant drain current which is not affected by the fluctuation of the supply voltage V_{DD} . It was conjectured that bias currents to be delivered from the drains of the MISFETs Q_{12}' and

Q_{13}' in response to the above referred to drain current would have no supply voltage dependence. It was consequently conjectured that the voltage V_{ref2} to be delivered from the circuit B would have no supply voltage dependence.

However, the reference voltage generator shown in Figure 1, requires a large number of circuit constituent elements because it is constructed of the two circuits having arrangements similar to each other, i.e., the circuit A for stabilizing the bias currents irrespective of the supply voltage fluctuations and the circuit B for determining the output voltage V_{ref2} and effecting the temperature compensation thereof. Moreover, we have discovered that, in spite of the temperature compensation, the output voltage - versus - temperature characteristic of the reference voltage generator is somewhat curved upwardly as indicated by a characteristic curve L_1 in Figure 9 by way of example. In other words, it was difficult to satisfactorily temperature-compensate the output voltage V_{ref2} over a wide temperature range.

In accordance with the present invention, the first one of a pair of MISFETs endowed with threshold voltages different from each other is diode-connected. The second one of the pair of MISFETs constitutes a source follower circuit which receives the drain voltage of the first MISFET. The

source of the second MISFET accordingly delivers a voltage of a level corresponding to the threshold voltage difference between the first MISFET and the second MISFET. A proper bias circuit for applying bias currents to the first and second MISFETs is prepared. The bias circuit includes a MISFET which receives across its gate and source electrodes, the voltage delivered from the source of the second MISFET. The bias currents to be supplied to the first and second MISFETs are determined by the MISFET in the bias circuit. Since the MISFET in the bias circuit has an appropriate threshold voltage - versus - temperature characteristic, the threshold voltage difference between the first and second MISFETs or the voltage to be delivered from the source of the second MISFET is temperature-compensated.

Referring now to the first embodiment shown in Figure 4, it will be seen that p-channel MISFETs and n-channel MISFETs constitute complementary circuits, and they are formed on a single silicon chip by the known CMOS IC technology which is employed in the polycrystalline silicon self-alignment technique.

A polycrystalline silicon layer which serves as the gate electrode of an n-channel MISFET Q_1 has its major part made the p^+ -conductivity type. A polycrystalline silicon layer which serves as the gate

electrodes of n-channel MISFETs Q_2 and Q_3 is made of the n^+ -conductivity type similar to the gate electrode of an ordinary n-channel MISFET which is manufactured by the known polycrystalline silicon self-alignment technique. The gate electrodes of p-channel MISFETs Q_4 and Q_5 are made of a polycrystalline silicon layer of the p^+ -conductivity type.

The MISFET, such as MISFET Q_1 , the gate electrode of which is made the opposite conductivity type to the channel conductivity type thereof is enclosed with a circle. Since the other usual MISFETs are not enclosed with circles, they are distinguished from the above-stated MISFET such as MISFET Q_1 . The same notation is adopted in the circuit diagrams of the other embodiments to be described later.

Figures 5A and 5B show sections of the MISFETs.

The major surface of an n-type single crystal silicon substrate 1 which is parallel to the (100) crystal plane is formed with a thick field oxide film 2 having a thickness of, e.g., about 1 μ m by the known local oxidation technique. Those parts of the substrate 1 which are not covered with the field oxide film 2 are used as active regions for forming the circuit elements.

The p-channel MISFET Q_4 comprises a p^+ -type

source region 4a and drain region 4b which are formed in the surface of the substrate 1, and a p^+ -type polycrystalline silicon layer 7a which is formed on the surface of the substrate 1 through a gate insulating film 6a. The p^+ -type polycrystalline silicon layer 7a forms the gate electrode of the MISFET Q_4 .

In the surface of the substrate 1, there are formed p-type well regions 3a and 3b for forming the n-channel MISFETs Q_1 and Q_2 .

The MISFET Q_1 comprises an n^+ -type source region 5a and drain region 5b which are formed in the surface of the p-type well region 3a, and a polycrystalline silicon layer 7b which is formed on the surface of the p-type well region 3a through a gate insulating film 6b. The polycrystalline silicon layer 7b has its central part G_2 formed by p^+ -type silicon. The polycrystalline silicon layer 7b has both its end parts G_1 and G_2 formed by n^+ -type silicon.

The MISFET Q_2 comprises an n^+ -type source region 5c and drain region 5d which are formed in the surface of the p-type well region 3b, and an n^+ -type polycrystalline silicon layer 7c which is formed on the surface of the p-type well region 3b through a gate insulating film 6c.

The surface of the p-type well region 3a is

formed with a p^+ -type contact region 4c as shown in Figure 5B.

An insulating film 8 made of, e.g., phosphosilicate glass is formed on the field oxide film 2 and the surfaces of the parts of the substrate 1 formed with the MISFETs. Wiring layers 9a to 9g are formed on the surface of the insulating film 8. These wiring layers 9a to 9g made of e.g. evaporated aluminium, and are held in ohmic contact with the various regions of the MISFETs. In order to enhance the gate - drain breakdown voltages of the respective MISFETs and also to prevent undesired impurities from being introduced into the polycrystalline silicon layers 7a to 7c, the surfaces of the polycrystalline silicon layers 7a to 7c are formed with thin oxide films by thermal oxidation before the insulating film 8 is formed. However, in Figure 5A, such thin oxide films are omitted for the sake of clarity.

The IC as shown in Figures 5A and 5B can be manufactured by the use of the CMOS IC production technology and without adding any special step of manufacture.

By way of example, after the p-type well regions 3a and 3b, the field oxide film 2 and the gate insulating films 6a to 6c have been formed, a polycrystalline silicon layer is formed on the whole

area of the surface of the substrate 1 by the known CVD (chemical vapour deposition) process. By selectively etching this polycrystalline silicon layer, the polycrystalline silicon layers 7a to 7c are formed.

Subsequently, a first silicon oxide film to be used as an impurity introducing mask is formed on the surface of the substrate 1 by the CVD process.

The selective etching is performed to remove those parts of the first silicon oxide film which overlie the parts to form the p-channel MISFETs therein, the part G_2 of the polycrystalline silicon layer 7b and the part to form the contact region 4c therein.

Subsequently, a p-type impurity such as boron is introduced by the impurity diffusion process into the polycrystalline silicon layers and the surface parts of the substrate 1 which are not covered with the first silicon oxide film. Thus, the p^+ -type semiconductor regions 4a to 4c are formed. In addition,

the entire polycrystalline silicon layer 7a and the central part G_2 of the polycrystalline silicon layer 7b are formed by p^+ -type silicon.

Next, the first silicon oxide film is removed, whereupon a second silicon oxide film to be used as an impurity introducing mask is formed on the substrate 1. The second silicon oxide film is removed in those parts which overlie the parts to form

the source and drain regions of the MISFET Q_1 therein, the end parts G_1 and G_3 of the polycrystalline silicon layer $7b$ and the part to form the MISFET Q_2 therein.

Next, an n-type impurity such as phosphorus is introduced into the polycrystalline silicon layers and the surface parts of the p-type well regions $3a$ and $3b$ which are exposed. As a result, the n^+ -type semiconductor regions $5a$ to $5d$ are formed. In addition, the end parts G_1 and G_3 of the polycrystalline silicon layer $7b$ and the entire polycrystalline silicon layer $7c$ are made the n^+ -type. The end parts G_1 and G_3 of the polycrystalline silicon layer $7b$ have the n-type impurity introduced thereinto, respectively, in order that the positions of the end parts of the n^+ -type source and drain regions $5a$ and $5b$ of the MISFET Q_1 may be determined by the polycrystalline silicon layer $7b$, in other words, that the regions $5a$ and $5b$ may be formed by the self-alignment technique. The widths of the end parts G_1 and G_3 are determined by a mask alignment precision.

The n-channel MISFET Q_1 has a threshold voltage V_{th1} of comparatively great magnitude because the part G_2 of its gate electrode is made of the p^+ -type polycrystalline silicon layer. The n-channel MISFET Q_2 has a comparatively small threshold voltage V_{th2} because its gate electrode

is made of the n^+ -type polycrystalline silicon layer.

The p-type well regions 3a and 3b in which the channels of the respective MISFETs Q_1 and Q_2 are formed are simultaneously formed by the IC production technology, so that they contain the conductivity type-determining impurity at densities equal to each other. Since the gate insulating films 6b and 6c are simultaneously formed, they are made of the same material and to equal thicknesses.

Since the channel regions of the MISFETs Q_1 and Q_2 have equal characteristics and the gate insulating films 6b and 6c are made of the same material and have the equal thicknesses, the difference between the threshold voltages V_{th1} and V_{th2} becomes equal to the difference between the Fermi level of p^+ -type polycrystalline silicon and that of n^+ -type polycrystalline silicon. The n^+ -type polycrystalline silicon which contains the conductivity type-determining impurity at a high density of, e.g. 10^{18} atoms/cm³ has the Fermi level close to the bottom of the conduction band thereof. Likewise, the p^+ -type polycrystalline silicon has the Fermi level close to the top of the valence band thereof. Therefore, the threshold voltage difference ($V_{th1} - V_{th2}$) becomes a value which is close to the band gap of silicon.

In Figure 4, the MISFET Q_1 is connected

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in diode configuration, that is, it has its drain and gate electrodes connected together in common. The drain of the MISFET Q_1 is connected to the gate of the MISFET Q_2 to be paired with the former MISFET. The MISFET Q_2 constitutes a source follower circuit along with the MISFET Q_3 . A bias current which flows between the drain and source of the MISFET Q_2 is determined by the MISFET Q_3 . This MISFET Q_3 has its drain and gate electrodes inter-connected in order that the bias current may be determined by an output voltage V_{ref} which is delivered from the source of the MISFET Q_2 , i.e. the MISFET Q_3 is connected in diode configuration. In order to supply a bias current to the MISFET Q_1 , there is provided a current mirror circuit CM_1 comprising the p-channel MISFETs Q_4 and Q_5 . The current mirror circuit CM_1 constitutes a constant current source. The input bias current of the current mirror type constant current source is produced from the drain of the MISFET Q_2 . Accordingly, a bias current which flows through the MISFET Q_1 is in accurate proportion to the bias current flowing through the MISFET Q_2 .

In Figure 4, the p-channel MISFETs Q_4 and Q_5 have their respective substrate gates (that is, the n-type silicon substrate 1 as shown in Figure 5A) connected to a power supply terminal V_{DD} along with

their respective sources. However, connections between the substrate gates of the MISFETs Q_4 and Q_5 and the power supply terminal have been omitted for the sake of clarity. Similarly, the connections of p-channel MISFETs to substrate gates have been omitted from the circuit diagrams of the other embodiments to be described later.

The n-channel MISFETs Q_1 and Q_3 have their respective substrate gates connected, along with their respective sources, to a reference potential terminal GND which is held at earth potential.

In this embodiment, it is desirable that the threshold voltage difference ($V_{th1} - V_{th2}$) between the MISFETs Q_1 and Q_2 is not affected by any other factor than the difference between the Fermi levels of the p^+ -type polycrystalline silicon and the n^+ -type polycrystalline silicon. If the substrate gate of the MISFET Q_2 is connected to the reference potential terminal GND, a voltage equal to the output voltage V_{ref} will be applied across the source and the substrate gate of the MISFET Q_2 . As a result, the threshold voltage V_{th2} will be increased by the substrate bias effect. The magnitude of the increment of the threshold voltage which is caused by the substrate bias effect is effected by the Fermi level of a semiconductor.

In contrast, the threshold voltage V_{th1} is not affected by the substrate bias effect because the source and the substrate gate of the MISFET Q_1 are held equipotential. Therefore, the threshold voltage different ($V_{th1} - V_{th2}$) becomes a value smaller than the Fermi level difference.

In this embodiment, the MISFET Q_2 has its substrate gate connected to its source similarly to the pairing MISFET Q_1 in order to prevent the undesirable decrease of the threshold voltage difference ($V_{th1} - V_{th2}$).

Now, the electrical characteristics of the circuit shown in Figure 4 will be described.

Letting m denote a current multiplication factor in the current mirror circuit CM_1 comprising the MISFETs Q_4 and Q_5 and I_0 denote the bias current of the MISFET Q_2 , the bias current which is supplied to the drain of the MISFET Q_1 becomes ($m \times I_0$). Letting $\beta_0 (W_1/L_1)$, $\beta_0 (W_2/L_2)$ and $\beta_0 (W_3/L_3)$ (where β_0 indicates a constant, W a channel width and L a channel length) denote the transconductances of the respective MISFETs Q_1 , Q_2 and Q_3 ; letting V_{th1} and V_{th2} denote the threshold voltages of the respective MISFETs Q_1 and Q_2 as described before; and letting V_{th3} denote the threshold voltage of the MISFET Q_3 ; the output voltage V_{ref} is then satisfied by the following

equation (1):

$$V_{\text{ref}} = (V_{\text{th1}} - V_{\text{th2}}) + \sqrt{\frac{2 I_o}{\mu_o (\frac{W_1}{L_1})}} \left\{ \sqrt{m} - \sqrt{\frac{(\frac{W_1}{L_1})}{(\frac{W_2}{L_2})}} \right\} \dots (1)$$

Here, the bias current I_o is determined by the MISFET Q_3 and which is satisfied by the following equation (2):

$$I_o = \frac{1}{2} \mu_o \left(\frac{W_3}{L_3}\right) (V_{\text{ref}} - V_{\text{th3}})^2 \dots (2)$$

5 From equations (1) and (2), accordingly, the output voltage V_{ref} is given by the following equation (3):

$$V_{\text{ref}} = \{ (V_{\text{th1}} - V_{\text{th2}}) - A V_{\text{th3}} \} / (1 - A) \dots (3)$$

10 where the term A is a constant which is denoted by the following equation (4):

$$A = \sqrt{\frac{(\frac{W_3}{L_3})}{(\frac{W_1}{L_1})}} \left\{ \sqrt{m} - \sqrt{\frac{(\frac{W_1}{L_1})}{(\frac{W_2}{L_2})}} \right\} \dots (4)$$

As will be apparent from equations (3) and (4), the output voltage V_{ref} assumes a value determined

by only the sizes and threshold voltages of the respective MISFETs, and it does not depend upon the supply voltage V_{DD} .

As can be seen from equation (4), the value of the constant A is made zero by setting the current multiplication factor $\underline{m}$ and the size ratio of the MISFETs Q_1 and Q_2 at certain predetermined values. By way of example, when the current multiplication factor $\underline{m}$ is made equal to unity and the sizes of the MISFETs Q_1 and Q_2 are made equal to each other, the constant A becomes zero. At this time, the output voltage V_{ref} becomes equal to the threshold voltage difference ($V_{th1} - V_{th2}$), i.e. the Fermi level difference between the p^+ -type polycrystalline silicon and the n^+ -type polycrystalline silicon as seen from Equation (3).

However, care needs to be taken of the fact that the band gap of silicon has the temperature dependence as shown in Figure 2 and the fact that the Fermi levels of the p-type and n-type silicon materials have temperature dependences as shown in Figure 3.

In the case where the gate electrodes of the MISFETs Q_1 and Q_2 are made of the polycrystalline silicon as described above, the threshold voltage difference ($V_{th1} - V_{th2}$) has some temperature characteristic in accordance with such

temperature dependences of the Fermi levels of the polycrystalline silicon materials. By way of example, in the case where the polycrystalline silicon layers to form the gate electrodes of the MISFETs Q_1 and Q_2 were respectively diffused with boron and phosphorus at high densities substantially equal to saturation densities with a view to attaining a threshold voltage difference ($V_{th1} - V_{th2}$) of about 1.2 volt, the measured temperature coefficient of the threshold voltage ($V_{th1} - V_{th2}$) was about -0.3 -0.5 mV/°C.

In this embodiment, the temperature dependence of the threshold voltage difference ($V_{th1} - V_{th2}$) and that of the threshold voltage V_{th3} are noted.

When the right-hand side of equation (3) is differentiated by the temperature T , the following equation (5) indicative of the temperature dependence of the output voltage V_{ref} can be obtained:

$$\frac{\partial V_{ref}}{\partial T} = \left\{ \frac{\partial (V_{th1} - V_{th2})}{\partial T} - A \frac{\partial V_{th3}}{\partial T} \right\} / (1 - A) \quad \dots (5)$$

In order to make the temperature dependence of the output voltage V_{ref} zero, the constant A may be set in consideration of the temperature dependence of the threshold voltage difference ($V_{th1} - V_{th2}$) and that of the threshold voltage V_{th3} so as to make the

numerator terms of the right-hand side of equation (4) equal to zero. As will be apparent from equation (4), the constant A is determined by the size ratios of the respective MISFETs and the current multiplication factor. As will be understood from Figures 2 and 3, the temperature characteristic curve of the threshold voltage difference ($V_{th1} - V_{th2}$) is somewhat convex. Although not illustrated, the temperature characteristic curve of the threshold voltage V_{th3} of the MISFET Q_3 is somewhat convex likewise to that of the threshold voltage difference ($V_{th1} - V_{th2}$).

In the foregoing case of the prior art circuit shown in Figure 1, the temperature compensation voltage which is formed substantially by the MISFETs Q_{14}' and Q_{15}' with their operating currents unbalanced can correct the threshold voltage difference in only a comparatively narrow temperature range. As a result, the output voltage V_{ref2} of the circuit of Figure 1 takes the form of the curve L_1 in Figure 9 referred to before.

In contrast, in the case of the circuit of the first embodiment shown in Figure 4, the threshold voltage V_{th3} has the temperature dependence similar to that of the threshold voltage difference ($V_{th1} - V_{th2}$), so that the temperature dependence of the threshold voltage difference ($V_{th1} - V_{th2}$) can be

satisfactorily compensated over a wide temperature range.

A curve L_2 in Figure 9 indicates the measured result of the output voltage V_{ref} at the time when the sizes of the MISFETs Q_1 to Q_3 were made equal to one another and when the current multiplication factor m of the current mirror circuit CM_1 comprising the MISFETs Q_4 and Q_5 was made equal to 1.5, that is, when the constant A was made equal to 0.22.

As will be apparent from Figure 9, the temperature coefficient can be made substantially zero by appropriately fixing the constant A.

Figure 6 shows the circuit of a second embodiment. In this circuit, a current mirror circuit CM_2 comprises MISFETs Q_3 and Q_6 , whilst another current mirror circuit CM_3 comprises MISFETs Q_5 and Q_4 . The drain current of the MISFET Q_4 is supplied to an n-channel MISFET Q_1 having a p^+ -type polycrystalline silicon electrode.

Since the MISFETs Q_3 and Q_6 are set at appropriate sizes, the current ratio between the MISFETs Q_3 and Q_6 is properly set. As a result, the current ratio between the MISFETs Q_1 and Q_2 is properly set.

Since the current ratio of bias currents to flow through the MISFETs Q_1 and Q_2 and the sizes

of the MISFETs Q_1 , Q_2 and Q_3 are properly set, a desirable output voltage V_{ref} which is stable against temperature fluctuations and power supply fluctuations can be obtained as in the first embodiment shown in Figure 4.

In the circuit of Figure 6, the current ratio of the bias currents which flow through the MISFETs Q_1 and Q_2 can also be properly set by appropriately setting the size ratio between the MISFETs Q_5 and Q_4 constituting the current mirror circuit CM_3 , instead of changing the size ratio between the MISFETs Q_3 and Q_6 .

In accordance with the circuit of Figure 6, the drain of the MISFET Q_2 is maintained at a high voltage because it is connected to a power supply terminal V_{DD} . Accordingly, the circuit of Figure 6 operates satisfactorily even with a supply voltage of a value smaller than the operating lower-limit voltage of the circuit in Figure 4.

Figure 7 shows the circuit of a third embodiment. In this circuit of Figure 7, the drain current of a MISFET Q_3 is supplied to a current mirror circuit CM_4 which comprises MISFETs Q_7 , Q_6 and Q_4 .

One output current of the current mirror circuit CM_4 is supplied to a diode-connected MISFET Q_1 , whilst the remaining output current is

supplied to a current mirror circuit CM_5 which comprises MISFETs Q_8 and Q_5 .

A bias current is caused to flow through a MISFET Q_2 by the current mirror circuit CM_5 .

5 The MISFETs Q_1 , Q_2 and Q_3 are made MISFETs having structures similar to those of the MISFETs Q_1 , Q_2 and Q_3 in Figures 4 and 6.

10 Since the MISFETs Q_1 , Q_2 and Q_3 are connected as shown in Figure 7, a constant voltage V_{ref} can be derived from the gate of the MISFET Q_3 .

The bias currents which flow through the MISFETs Q_1 and Q_2 are set at an appropriate ratio by altering the current multiplication factor of at least one of the current mirror circuits CM_4 and CM_5 .

15 The circuit of the embodiment shown in Figure 7 has the merit that its output voltage V_{ref} is not readily affected by fluctuations in the supply voltage as described below.

20 The source - drain voltage of the MISFET Q_4 is varied due to the fluctuation of the supply voltage. When the source - drain voltage has been varied in this manner, the drain current of the MISFET Q_4 has its magnitude varied by the known channel length modulation effect. As a
25 result, the magnitude of the bias current of the MISFET Q_1 is varied.

However, in this embodiment, the drain

current of the MISFET Q_6 is varied simultaneously the drain current of the MISFET Q_4 by the channel length modulation effect. As a result, the ratio between the drain current of the MISFET Q_4 and that of the MISFET Q_6 is made a substantially constant value corresponding to the size ratio between these MISFETs Q_4 and Q_6 , irrespective of the fluctuation of the supply voltage. The MISFET Q_5 constituting the current mirror circuit CM_5 has its drain - source voltage held constant by the MISFET Q_2 . Therefore, the current multiplication factor of the current mirror circuit CM_5 is maintained at a constant value irrespective of the fluctuation of the supply voltage.

As a result, the ratio between the bias currents which flow through the MISFETs Q_1 and Q_2 is maintained at a substantially constant value irrespective of the fluctuations in the supply voltage. Since, in this manner, the ratio of the bias currents of the two MISFETs Q_1 and Q_2 is maintained at a good value, the variation which is imposed on the output voltage V_{ref} at the fluctuation of the supply voltage becomes sufficiently small.

Referring now to the fourth embodiment shown in Figure 8, the circuit is designed such that the supply voltage dependence of an output voltage

V_{ref} is improved more satisfactorily. In a MISFET which is operated in its saturation region, even when a constant bias voltage is applied across the gate and source thereof, the source - drain current thereof is changed by the known channel length modulation effect as above described due to a change in the source - drain voltage thereof.

In the case of the circuit as shown in Figure 4, one MISFET Q_5 constituting the current mirror circuit CM_1 has its gate and drain connected in common and therefore has its source - drain voltage maintained at a value substantially equal to its threshold voltage. Accordingly, the source - drain voltage of the MISFET Q_5 is maintained at a substantially constant value irrespective of the fluctuation of the supply voltage V_{DD} . In contrast, the source - drain voltage of the diode-connected MISFET Q_1 is made a substantially constant value, so that the source - drain voltage of the other MISFET Q_4 constituting the current mirror circuit CM_1 varies in accordance with the fluctuations of the supply voltage V_{DD} . The drain current of the MISFET Q_4 is accordingly varied comparatively greatly in accordance with the fluctuations of the supply voltage V_{DD} . Since the drain current of the MISFET Q_4 is changed, the current multiplication factor $\underline{m}$ of the current mirror circuit CM_1 is

changed in accordance with the fluctuations of the supply voltage V_{DD} . For this reason, the voltage V_{ref} which is delivered from the circuit shown in Figure 4 comes to have some supply voltage dependence.

5 In the circuit shown in Figure 8, a current mirror circuit CM_1 comprises p-channel MISFETs Q_5 and Q_4 . In addition, a differential amplifier D-AMP comprises p-channel MISFETs Q_7 and Q_8 for amplification and n-channel MISFETs Q_9 and Q_{10} in the current mirror connection. A p-channel MISFET Q_6 is interposed between the drain of the output MISFET Q_4 in the current mirror circuit CM_1 and the gate and drain of a diode-connected MISFET Q_1 . The gate of the MISFET Q_6 is supplied with the output of the differential amplifier D-AMP.

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The drain voltages of the MISFETs Q_4 and Q_5 are supplied to the differential amplifier D-AMP. The output of the differential amplifier D-AMP is negatively fed back to the gate of the MISFET Q_6 . As the result of the negative feedback operation, the drain voltage of the MISFET Q_4 becomes a value equal to that of the MISFET Q_5 .

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As a result of the source - drain voltages of the MISFETs Q_4 and Q_5 being equalized to each other, the relative variations of the source - drain currents of the MISFETs Q_4 and Q_5 as based on the respective channel length modulation effects thereof

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become equal to each other. As a result, the current multiplication factor $\underline{m}$ of the current mirror circuit CM_1 is held constant irrespective of the fluctuation of the supply voltage V_{DD} .

5 Since the multiplication factor $\underline{m}$ is held constant, a voltage V_{ref} which is delivered from the circuit shown in Figure 8 has substantially no dependence on the supply voltage.

10 Each of Figures 10A to 10C shows the arrangement of a current mirror circuit CM_1 whose current multiplication factor $\underline{m}$ fluctuates little due to the channel length modulation effect.

15 Each of the circuits in Figures 10A to 10C can be replaced with the current mirror circuit CM_1 shown in Figure 4, or with the current mirror circuit CM_1 or the differential amplifier D-AMP and the MISFET Q_6 shown in Figure 8. The circuit shown in Figure 10A is constructed of the smallest number of MISFETs. When, in the circuit of Figure 10B or 20 Figure 10C, at least MISFETs Q_{23} and Q_{24} have equal threshold voltages, the source - drain voltages of MISFETs Q_4 and Q_5 can be substantially equalized to each other. In order to equalize the drain voltages of the MISFETs Q_4 and Q_5 irrespective of the current 25 multiplication factor $\underline{m}$, the ratio between the sizes of the MISFETs Q_{23} and Q_{24} may be equalized to the ratio between the sizes of the MISFETs Q_4 and Q_5 .

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The above described embodiments can be extensively utilized as reference voltage generators.

For example, it is required to form the reference voltage of a battery checker as shown in Figure 11 which gives an alarm when there is a decrease in the voltage of a battery and which is utilized in an electronic desk calculator. The reason is that it includes a small number of elements used and can be readily put into the form of a 1-chip MIS IC.

This circuit operates as follows. First, there is provided a reset signal generator (not shown) and a reset signal is produced therefrom at the time of closure of a power supply. A flip-flop circuit FF is accordingly reset by the signal supplied to its reset terminal at the closure of the power supply. A divided voltage $(R_2 E_0)/(R_1 + R_2)$ which is delivered from a voltage divider constructed of resistance elements R_1 and R_2 is changed with a battery voltage E_0 . This divider voltage and the reference voltage delivered from the reference voltage generator are compared by a comparator CMP.

In the case where the battery voltage E_0 is greater than a predetermined value, the output of the comparator CMP is made a low level which is substantially equal to earth potential.

In the case where the battery voltage E_0

has become lower than the predetermined value, the output of the comparator CMP is at a high level which is substantially equal to the level of the battery voltage E_0 .

5 The flip-flop FF is accordingly brought into its set status. A display device (not shown) is driven by the set output of the flip-flop FF. That is, the display of the alarm to indicate a run down battery is effected. Operating waveforms are
10 shown in Figure 12.

 In a modified form, in place of the construction wherein with a view to making the threshold voltages of the respective MISFETs unequal, the conductivity types of the polycrystalline
15 silicon layers as the gate electrodes are made different as described before there can be adopted a construction wherein various factors influential on the threshold voltages are made different. For example, in case of utilizing the difference
20 between the work functions of gate electrodes, the gate electrode of one of a pair of MISFETs can be made of polycrystalline silicon, and that of the other MISFET can be made of aluminium or molybdenum. It is also possible to change the density of a
25 conductivity type-determining impurity in a part to be used as the channel region of one MISFET, with an ion implantation technique. The MISFETs, such

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as those Q_3 shown in Figures 4, 6 and 8, which are diode-connected in order to determine bias current levels may well be of p-channel type instead of n-channel type. In the case where a comparatively
5 high reference voltage is required, the circuit as shown in Figure 4, for example, may be combined with a linear amplifier having an appropriate gain.

Alternatively, a circuit of an arrangement as shown in Figure 13 may be used instead, in order
10 to obtain a voltage equal to $2V_{\text{ref}}$ at the output terminal T_O . As shown each of the MISFETs Q_1 , Q_2 and Q_3 is associated with a corresponding identical MISFET Q_{1a} , Q_{2a} and Q_{3a} respectively, said additional MISFETs being in series with the associated
15 respective original MISFETs Q_1 , Q_2 and Q_3 of the circuit shown in Figure 4.



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CLAIMS.

1. A reference voltage generator including:
 - (a) an output terminal;
 - (b) a first MISFET which is supplied across its gate and source with a voltage between said
5 output terminal and a reference point and which produces a drain - source current of a level corresponding to the voltage supplied across said gate and source;
 - (c) a bias circuit generating first and
10 second bias currents which have levels proportional to the drain - source current of said first MISFET;
 - (d) a second MISFET which has a drain - source path coupled between a first node and said reference point, and a gate coupled to a drain
15 thereof; the drain - source path being supplied with said first bias current; and
 - (e) a third MISFET which has a gate coupled to said first node, a source coupled to said output terminal, and a drain, whose threshold voltage is
20 made a value smaller than that of said second MISFET and whose drain - source path is supplied with said second bias current;
- whereby a voltage which corresponds to a difference between a threshold voltage of said second
25 MISFET and that of said third MISFET is supplied from said third MISFET to said output terminal.



2. A reference voltage generator according to Claim 1, wherein a potential difference which is applied across the substrate gate and source of said third MISFET is equalized to a potential difference which is applied across the substrate gate and source of said second MISFET.

3. A reference voltage generator according to Claim 1, wherein said second MISFET and said third MISFET have channel lengths and channel widths equal to each other, and said first bias current has a value greater than said second bias current.

4. A reference voltage generator according to Claim 1, wherein said first MISFET has its drain - source path coupled between said output terminal and said reference point, and has its gate coupled to its drain.

5. A reference voltage generator according to Claim 4, wherein said bias circuit includes a current mirror circuit which is supplied with a drain current of said third MISFET thereby to generate said first bias current.

6. A reference voltage generator according to Claim 5, wherein said current mirror circuit comprises a fourth MISFET whose gate and drain are inter-connected and which has a conductivity type opposite to that of said third MISFET, and a fifth MISFET whose gate is coupled to the gate of said



fourth MISFET, whose source is coupled to a source of said fourth MISFET and which has the same conductivity type as that of said fourth MISFET.

5 7. A reference voltage generator according to Claim 6, further including an additional circuit which makes the source - drain voltage of said fifth MISFET substantially equal to that of said fourth MISFET.

10 8. A reference voltage generator according to Claim 7, wherein said additional circuit comprises a sixth MISFET which has a source - drain path connected between the drain of said fifth MISFET and that of said second MISFET and which has the same conductivity type as that of said fifth MISFET, and
15 a differential amplifier which has a non-inverting input terminal which is supplied with the drain voltage of said fourth MISFET, an inverting input terminal which is supplied with the drain voltage of said fifth MISFET and an output terminal which
20 delivers a voltage to be supplied to the gate of said sixth MISFET.

 9. A reference voltage generator according to Claim 4, wherein said bias circuit includes a fourth MISFET whose gate and source are respectively
25 connected to the gate and source of said first MISFET in common, and a current mirror circuit which is supplied with a drain current of said fourth



MISFET in order to generate said first bias current.

10. A reference voltage generator according to Claim 1, wherein said bias circuit includes a current mirror circuit which is supplied with a drain current of said first MISFET in order to generate said first and second bias currents.

11. A reference voltage generator according to Claim 10, wherein said current mirror circuit comprises a fourth MISFET which has a gate and a drain connected to the drain of said first MISFET in common and which has a conductivity type opposite to that of said first MISFET, and fifth and sixth MISFETs whose gates and sources are respectively connected to the gate and source of said fourth MISFET and which have the same conductivity type as that of said fourth MISFET, whereby said first bias current is delivered from the drain of said sixth MISFET, and said second bias current is delivered from the drain of said fifth MISFET.

12. A reference voltage generator according to Claim 11, wherein said current mirror circuit further includes a seventh MISFET which has a gate and a drain connected to the drain of said fifth MISFET in common and which has the same conductivity type as that of said first MISFET, and an eighth MISFET which has a gate and a source respectively connected to the gate and a source of said seventh



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MISFET in common and which has the same conductivity type as that of said first MISFET, whereby said second bias current is generated at the drain of said eighth MISFET.

5 13. A reference voltage generator according to Claim 1, wherein said first to third MISFETs are formed on a semiconductor substrate which is formed as a CMOS IC.

10 14. A reference voltage generator according to Claim 12, wherein the gate of said second MISFET and that of said third MISFET are made of materials having work functions different from each other.

15 15. A reference voltage generator according to Claim 14, wherein the gates of said second and third MISFETs are made of silicon.

16. A reference voltage generator according to Claim 15, wherein said second and third MISFETs are of the n-channel type.

20 17. A reference voltage generator according to Claim 16, wherein the gate of said second MISFET is of the p-type, whilst the gate of said third MISFET is of the n-type.

25 18. A reference voltage generator according to Claim 17, wherein said second and third MISFETs are formed on p-type well regions which are formed in a surface of said semiconductor substrate electrically independently of each other.



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19. A reference voltage generator constructed substantially as herein described with reference to and as illustrated in Figure 4, or Figure 6, or Figure 7, or Figure 8, or Figure 13 of the accompanying drawings.
