GATE PROTECTION ARRANGEMENT FOR A SEMICONDUCTOR DEVICE

The present invention relates generally to a semiconductor device provided with a gate-protecting circuit.

In many semiconductor integrated circuits, a gate-protecting circuit is provided in the vicinity of the input portion, particularly in the vicinity of an input pad (bonding pad), in order to protect the internal circuit elements from excessively large input signals from external units. Fig. 1 of the accompanying drawings shows an example of a known integrated circuit in which a gate-protecting circuit 1 consisting of an input resistor 2 and a clamping diode 3 is inserted between an input pad 4 and internal circuitry 5 having elements that must be protected.

In this gate-protecting circuit, the input resistor may be a diffused semiconductor layer (or region) that is obtained by doping the main surface of a semiconductor substrate with impurities. Alternatively, the input resistor may be a polycrystalline silicon layer that is formed on the main surface of the semiconductor susbtrate. Fig. 2 of the accompanying drawings shows a resistor in which the main surface of a semiconductor substrate 6 is doped with impurities to form a shallow diffused semiconductor layer 8 between field oxide films 7. In Fig. 2 an input pad 9 in the form of an aluminium layer is connected to one end of the semiconductor layer 8, and

(15)

wiring 10 of the internal circuitry is connected to the other end of the semiconductor layer 8. Fig. 3 of the accompanying drawings shows a resistor in which a polycrystalline silicon layer 13 (which has a high resistance but a low impurity concentration) is formed by e.g. chemical vapour deposition (CVD) on a field oxide film 12 of a semiconductor substrate 11. As shown in Fig. 3, an input pad 14 is connected to one end of the polycrystalline silicon layer 13, and wiring 15 for the internal circuitry (e.g. circuitry 5 from Fig. 1) is connected to the other end of the polycrystalline silicon layer 13, over an insulating film 16 (e.g. see "Nikkei Electronics", January 31, 1983, p. 138, etc.).

With the above two constructions, however, the inventor has discovered that the input resistor and the input pad are laid out separately on the main surface of the semiconductor substrate, so that the area occupied by the gate-protecting circuit is increased, making it difficult to accomplish a high degree of integration. In devices which operate at high speed, in particular, the resistances of the semiconductor layer 8 and polycrystalline silicon layer 13 have been reduced by a silicide technique without increasing the steps of fabrication. Therefore, in order for the semiconductor layer and the polycrystalline silicon layer to retain a predetermined resistance, their areas must be increased, which makes it difficult to fabricate a device in a highly integrated form.

To overcome the problem, the present invention proposes, in a first aspect, a semiconductor device having a gate-protecting circuit between an input pad and internal circuit elements including MOS transistors, comprising:

a diffused semiconductor well region of a second conductivity type within a semiconductor substrate of a first conductivity type, the diffused semiconductor well region acting as an input resistor of the gate protecting circuit;

two silicide films at spaced-apart positions on the diffused semiconductor well region, one silicide film coupling the input pad to the well region and the other coupling the well region to the MOS transistors of the internal circuit element;

a field oxide film over the well region; and

further silicide films covering the source and drain regions of the MOS transistors.

This makes possible a reduction in the total area of the device and hence permits the device to have a highly integrated form.

In a second aspect the present invention provides a method of fabricating a semiconductor device having a gate protecting circuit and internal circuit elements including MOS transistors, the method comprising:

forming a diffused semiconductor well region of a second conductivity type within a semiconductor substrate of a first conductivity type;

forming two silicide films at spaced apart locations on the diffused semiconductor well region;

forming a field oxide film over the well region; and

forming further silicide films covering the source and drain regions of the MOS transistors;

thereby to form a device in which the diffused semiconductor well region acts as an input resistor of the gate protecting circuit, one of the silicide films couples the input pad to the well region, and the other silicide film coupling the well region to the MOS transistors of the internal circuit.

An embodiment of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a diagram of a gate-protecting circuit and has already been described;

Figs. 2 and 3 are sections through conventional resistor constructions and have already been described;

Fig. 4 is a plan view of major portions of a semiconductor device helpful in understanding the present invention;

Fig. 5 is a section taken along line X-X through Fig. 4; and

Figs. 6(A) to 6(F) are sections showing the manufacturing steps thereof.

Fig. 7 is a sectional view of an embodiment of the present invention.

As shown in Figs. 4 and 5, a diffused semiconductor layer 21 consisting of p-type impurities such as boron ions is formed in an oblong shape in a portion of the surface

of an n-type silicon substrate 20 which contains impurities such as phosphorous ions. The semiconductor layer 21 is between 0.5 to 10 μm deep and has a sheet resistivity of 1 to 50 kΩ/□. Semiconductor region 21A is formed in a separate portion as a p-type well in which an NMOS transistor Q_N of a CMOS circuit will be formed, as described later and has a similar depth and sheet resistivity to the layer 21.

An oxide film which is between 0.5 to 2.0 μm thick, and which acts as a field oxide film 22, is formed on top of the semiconductor layer 21, and a pair of contact portions 23, 24 are formed in the oxide film 22 at each end of the semiconductor layer 21. A p-type semiconductor layer 25 or an n-type semiconductor layer 26 that acts as a channel stopper can be formed, if desired, under the oxide film 22, and p-type high-concentration semiconductor layers ($1 \times 10^{20}/cm^3$) 27, 28 having a depth of 0.35 μm are formed under the contact portions 23, 24. The semiconductor layer ($5 \times 10^{16}/cm^3$) 25 having a depth of 1 μm formed over the semiconductor layer 21 (and having a higher impurity concentration than region 21) also serves as a part of the input resistor so that the input resistance is effectively defined by the regions 21 and 25. It should be noted that the layers 25 and 26 are optional, but can be useful in obtaining optimum performance. An SiO_2 film 29 that acts as an intermediate insulating layer is then formed, and contact holes are formed therein at the contact

portions 23, 24.

A PMOS transistor Q_P consisting of a gate electrode 30 and p-type semiconductor layers ($1 \times 10^{20}/cm^3$) 31 having a depth of 0.35 μm is formed in another portion of the silicon substrate 20, and an NMOS transistor Q_N consisting of a gate 32 and n-type semiconductor layer ($1 \times 10^{20}/cm^3$) 33 is formed in the other semiconductor layer 21A. These transistors Q_P and Q_N form part of the internal circuitry of the MOS circuit that is to be protected.

Aluminium layers 34, 35 and 36 are formed over the SiO_2 film 29 to connect the transistors Q_P, Q_N, and aluminium layers 37, 38 are connected to the semiconductor layers (the high-concentration impurity layers 27, 28) through contact holes. Of these, the aluminium layer 37 is connected to the internal circuitry (such as the CMOS circuit), and the aluminium layer 38 that acts as an input pad is formed in approximately square configuration on the oxide film 22 or, in other words, over the semiconductor layer 21.

The steps of manufacturing this semiconductor device will be described below in conjunction with Figs. 6(A) to 6(F).

First, the main surface of an n-type silicon substrate 20 is completely oxidized to form an oxide film 40, as shown in Fig. 6(A), and then windows 41 are formed in the oxide film 40 by a photolithographic technique, as shown in

Fig. 6(B). Using the oxide film as a mask, boron ions are implanted and are diffused by a high-temperature treatment, to form the p-type diffused semiconductor layers 21, 21A, as shown in Fig. 6(C). The oxide film 40 is then removed by etching.

An SiO_2 film 42 is then formed over the whole surface, as shown n Fig. 6(D), and an Si_2N_3 film 43 of a required pattern is formed thereon. The Si_2N_3 film 43 is then selectively oxidized to form thick oxide films that act as the field oxide films 22 as shown in Fig. 6(E). If it is desired to include a region 25 and 26 for channel stopping and, in the case of region 25, for serving as part of the input resistor, the following steps (not shown) can be used. After the step of Fig 6(D), first and second ion implantations through a SiO_2 film 42 are carried out using an Si_3N_4 film 43 and two photoresist films (not shown) as masks. One of the photoresist films covers the surface of n-type substrate for implanting p-type impurities which will be used to form region 25, and the other covers the surface of p-type well for implanting n-type impurities which will be used to form the region 26. In the step of Fig. 6(E), the channel stoppers 25 and 26 and a field oxide film 22 can then be formed simultaneously by a conventional heat treatment method.

The NMOS transistor Q_N and the PMOS transistor Q_P are thereafter formed in a customary manner, the high-concentration impurity layers 27, 28 are formed

simultaneously with the semiconductor layers 31 of the PMOS transistor Q_p, and a wiring layer 37 and an input pad 38 are formed simultaneously with the formation and contact of the aluminum layers 34,35 and 36, and are connected together. This completes the semiconductor device shown in Fig. 6(F) and Fig. 4. The same reference numerals as those used in Fig. 4 are used for the device of Fig. 6(F).

According to the thus-constructed semiconductor device, the input pad 38 is formed on the semiconductor layer 21 that acts as an input resistor. Therefore, the total area of the input pad 38 and the semiconductor layer 21 can be reduced by the quantity by which they are superposed, and the device can be efficiently integrated. The input pad 38 is formed flat on the field oxide film 22, so that a good bonding can be effected.

The semiconductor device discussed above with reference to Figs. 4 to 6 is not an embodiment of the invention. However, it is helpful in understanding the embodiment of the present invention, which will now be described.

Fig. 7 shows an embodiment of the present invention which utilizes platinum silicide layers 50 which are formed on the resistor contact layers 27, 28, platinum silicide layers 52 which are formed on the source and drain regions 31 of the transistors Q_p and platinum silicide layers 54 which are formed on the source and drain regions 33 of the transistor Q_N. Numerals in Fig. 7 which

correspond to numerals used in Fig. 5 identify like elements. The silicide layers 50, 52 and 54 having a sheet resistivity of 4 Ω/□ and 500 Å thick can be formed in a self-aligned manner similar to that described on pages 164 and 165 of an article by T. Shibata et al., "An Optimally Designed Process for Submicrometer MOSFET's", IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 2, April, 1982, pp. 161-165, which article is herein incorporated by reference. As noted in that article, the advantages of this silicide technique is that it permits lowering the resistance of the source and drain regions so that a shallow diffused source and drain can be used without increasing the resistance of the source and drain to the point that it degrades the circuit performance. Other various metals can be used for forming the silicide, including Mo, W, Ta, or Ti.

By virtue of the structure of Fig. 7, the silicide can be added at the location shown without being plated over the resistor 21. This prevent the silicide from undesirably reducing the resistance value of the resistor 21 (which would correspondingly require increasing the area of the resistor). At the same time, the resistance of the source, drain and resistor contacts is reduced to maximise speed.

An added feature of the Fig. 7 arrangement is the formation of a SiO_2 film 56 over the gate of electrodes of the respective transistors Q_P and Q_N. This serves as a

side wall for the silicide step, and can be accomplished in a manner similar to that shown in Fig. 2 of the article by P.J. Tsang et al., "Fabrication of High-Performance LDDFET's With Oxide Sidewall-Spacer Technology", IEEE Transactions on Electronic Devices, Vol. ED-29, No. 4, April, 1982, pp. 590-596, which article is also herein incorporated by reference. It should be noted that, if desired, the silicide could be formed over the gate electrode by etching the SiO_2 film to expose the gate electrode prior to the silicidation.

Some advantages of the embodiment described above are as follows:

(1) the input resistor of a gate-protecting circuit is formed by an impurity diffused semiconductor layer, and an input pad may be formed on the input resistor. Therefore, the total layout area can be reduced to less than that when the input resistor and the input pad are arranged separately, and the semiconductor device can be realized in an extremely highly-integrated form.

(2) An input pad may be formed on a thick field oxide film on an impurity diffused semiconductor layer, so that the input pad is flat, enabling a good bonding of a wire or the like.

(3) An impurity diffused semiconductor layer and an input pad can be formed by utilizing standard steps for fabricating MOS transistors, and can hence be formed easily without complicating the manufacturing process thereof.

The invention has been described in detail above by way of an embodiment thereof. However, the invention should not be limited to this embodiment alone, and can be variously modified within a scope that does not depart from the gist thereof. For instance, the device may be of a construction in which an n-type well is formed in a p-type silicon substrate, or it may be of the SOS (silicon on sapphire) construction, or the SOI (silicon on insulating film) construction. In addition to boron and phosphorous ions, furthermore, the impurities may be any of those in groups III or V, such as arsenic or antimony ions.

Normally, the silicide films 50 which couple the resistor 21 to the input pad 38 and the wiring layer 37 and the silicide films 52,54 which cover the source and drain regions 31,33 of the MOS transistors Q_P, Q_N are formed simultaneously, but this is not essential.

CLAIMS:

1. A semiconductor device having a gate-protecting circuit between an input pad and internal circuit elements including MOS transistors, comprising:

a diffused semiconductor well region of a second conductivity type within a semiconductor substrate of a first conductivity type, the diffused semiconductor well region acting as an input resistor of the gate protecting circuit;

two silicide films at spaced-apart positions on the diffused semiconductor well region, one silicide film coupling the input pad to the well region and the other coupling the well region to the MOS transistors of the internal circuit element;

a field oxide film over the well region; and

further silicide films covering the source and drain regions of the MOS transistors.

2. A device according to claim 1, wherein at least one of the MOS transistors is formed in a further diffused well region of the second conductivity type in the semiconductor substrate.

3. A device according to claim 2 having at least one MOS transistor with source and drain regions of the first conductivity type in the further diffused well region, and at least one MOS transistor with source and drain regions of the second conductivity type in the substrate.

4. A device according to claim 2 or claim 3, wherein

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the further diffused well region is formed simultaneously with the well region acting as an input resistor.

5. A device according to any one of claims 1 to 4, wherein the silicide films over the well region and the further silicide films over the source and drain regions of the MOS transistors are formed in a self-aligned manner with the field oxide film.

6. A device according to any one of the preceding claims, wherein the silicide films and the further silicide films are formed simultaneously.

7. A device according to any one of the preceding claims having semiconductor regions between the silicide films and the well region which have the same conductivity type as but a higher impurity concentration than the well region.

8. A device according to any one of the preceding claims having a further semiconductor region between the well region and the field oxide film which has the same conductivity type as but a higher impurity concentration than the well region.

9. A device according to any one of the preceding claims, having channel stopper regions adjacent the source and drain regions of the MOS transistors, the channel stopper regions being of a conductivity type opposite to the adjacent source or drain region.

10. A device according to claim 9 as dependant on claim 8, wherein the channel stopper regions are formed

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simultaneously with the further semiconductor region.

11. A semiconductor device substantially as herein described with reference to and as illustrated in Fig. 7 of the accompanying drawings.

12. A method of fabricating a semiconductor device having a gate protecting circuit and internal circuit elements including MOS transistors, the method comprising:

forming a diffused semiconductor well region of a second conductivity type within a semiconductor substrate of a first conductivity type;

forming two silicide films at spaced apart locations on the diffused semiconductor well region;

forming a field oxide film over the well region; and

forming further silicide films covering the source and drain regions of the MOS transistors;

thereby to form a device in which the diffused semiconductor well region acts as an input resistor of the gate protecting circuit, one of the silicide films couples the input pad to the well region, and the other silicide film coupling the well region to the MOS transistors of the internal circuit.

13. A method according to claim 12, wherein a gate electrode of at least one of the MOS transistors is formed over a part of the substrate other than the part in which the diffused semiconductor well region is formed, and impurities of the second conductivity type are implanted into the substrate adjacent the or each gate electrode,

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thereby to form the source and drain regions of the at least one MOS transistor.

14. A method according to claim 12 or claim 13, wherein the diffused semiconductor well region is a first diffused semiconductor region and a further diffused semiconductor region of the second conductivity type is formed in the substrate, a gate electrode of at least one of the MOS transistors is formed over a part of the second diffused semiconductor well region, and impurities of the first conductivity type are implanted into the further diffused semiconductor region adjacent the or each gate electrode, thereby to form the source and drain regions of the at least one of the MOS transistors.

15. A method according to claim 14 wherein the first diffused semiconductor well region and the further diffused semiconductor well region are formed simultaneously.

16. A method according to any one of claims 12 to 15, further including:

forming a layer of insulating material over the field oxide film, and

forming an aluminium layer over the layer of insulating material.

17. A method according to any one of claims 12 to 16, wherein the silicide films and the further silicide films are formed simultaneously.

18. A method according to any one of claims 12 to 17, wherein the silicides film and the further silicide film

are formed in self-aligned manner with the field oxide film.

19. A method of fabricating a semiconductor device substantially as herein described with reference to Fig. 7.

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